

Novel Three-Phase Multi-Level Inverter with Reduced Components

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Abstract—A new multilevel converter topology is proposed in this paper. Low component count and compact design are the main features of the proposed topology. Furthermore, the proposed converter is a capacitor-, inductor-, and diode-free configuration, allowing reducing the converter footprint, increasing the lifetime and simplifying the control strategy. Further, a comparative study is carried out to highlight the merits of the proposed circuit as compared to existing multilevel topologies. Finally, simulation results for the three-level version using different modulation strategies are presented.

Index Terms— Fundamental frequency modulation, multilevel inverters, pulse width modulation

I. INTRODUCTION

Nowadays, renewable energy generators (REGs) are interconnected to the grid with a higher penetration for the purpose of meeting the increased demand for energy worldwide with keeping CO₂ emissions at low levels. Accordingly, notable improvements to energy conservation and a significant reduction of CO₂ emissions are achieved. Nevertheless, there are constant needs for proposing new technologies in order to increase system reliability and efficiency. Recent developments in those technologies have heightened the need for improving power electronics converters (PECs) that link the original energy source to the grid. PECs play an essential role in power systems containing renewable generators, as they take the responsibility of converting the generated primary power from REGs to be matched with the grid or load standards. Additionally, PECs are used for increasing the overall performance of generating systems because of their ability to integrate different storage technologies allowing doing several essential services such as energy arbitrage, peak shaving, load flowing, spinning reserve, voltage support, black start, and frequency regulation, etc. [1].

The main REGs are photovoltaic (PV), wind power (WP), and hydropower plants (HPPs). In these generating systems, various converter families already have been used for a long time, like traditional voltage source converters (VSCs), matrix converters (MCs), and cyclo-converters (CCVs). However, significant problems with these converters have limited power handling due to limited maximum power rating of available semiconductor devices, high total harmonics distortion (THD) in input and output sides, and negative influence on the power factor of the system by using none-fully-controlled converters such as CCV [2-5]. Several solutions have been presented for the purpose of overcoming the abovementioned

limitations, including using identical converters in parallel configurations for increasing the handled power, using complex, bulky and specially designed filters for improving the THD, and using compensation circuits for controlling the reactive power and improving the power factor in non-fully controlled converters. However, these solutions becoming unattractive today because they increase the weight, volume, complexity, and cost of PECs while decreasing efficiency, reliability and lifetime of the energy system [2, 3, 5]. These drawbacks prevent the use of these converters in high power applications. Unique features of modularity, low dv/dt , low THD, low switching frequency, low electromagnetic interferences, low filtering requirements, and low switching losses of multilevel converters (MLCs) allow them to be used intensively in modern medium- and high-power energy systems [6-8]. In other words, MLCs-based systems produce high-quality outputs with reasonable side effects.

Neutral point clamped converter (NPC) [9, 10], flying capacitors converter (FC) [11, 12], and cascaded H-bridge converter (CHB) [13] are three common topologies of MLCs. High component count, namely DC sources, electrolytic capacitors, transformers, switching devices, and power diodes, increasing the converter footprint, cost, conduction losses, control complexity and decreasing the lifetime is the main drawback of the mentioned topologies [6-8]. To tackle these drawbacks, several topologies were recently presented in [14-20], aiming to improve conventional configurations by proposing new circuits with reduced components count and simplified control algorithms. Towards this aim, a new multilevel converter topology is proposed in this paper. The proposed topology can produce the same number of voltage levels with low component count compared to the existing configurations. Further, the proposed topology has a compact design feature as it does not require either transformers or electrolytic capacitors for operation. This compact feature is important in portable solutions requiring a reduced size of the converter and low cooling system requirements. Besides, the losses in the proposed circuit will be decreased dramatically because of using only switching devices operating at low frequencies instead of using hybrid designs based on switches and diodes.

This paper is organized as follows. The operating principles of the proposed topology will be presented for three-level configuration in section II. In section III, a comparison between the proposed circuit and other MLC topologies for generating the same number of voltage levels will be provided. Then, the two applied switching schemes will be explained in section IV, while section V will introduce the simulation results for the two modulation schemes. Finally, conclusions will be withdrawn in section VI.

II. THE PROPOSED MULTI-LEVEL CONVERTER CONFIGURATION

Simplifying the converter structure is the main objective when designing the proposed MLC topology. By this way, a simple control system can be used, and an extra reliability degree can be obtained. To achieve this target, electrolytic capacitors, power transformer, and power diodes should not be used in the design of the proposed topology in order to avoid increasing the size, losses, and decreasing the lifetime of the converter. For wider applications, the input DC ports

should be decreased as well. Consequently, the number of required isolated DC sources will be reduced. One DC source is normally defined by an isolation transformer combined with a six-pulse rectifier. Therefore, saving one DC source means saving six power diodes and one isolation transformer. According to this perspective, the proposed topology is designed to have a fewer number of isolated DC sources while keeping reasonable switching device count. The proposed topology uses only two DC sources and twelve switching devices for producing three-level pole voltages, resulting in five-level line voltages. The two isolated DC sources can be realised for example by using two PV generators. Fig. 1 shows the power circuit and the resulting voltages of the proposed MLC. Although the proposed topology can be extended to N level, only the three-level configuration is studied in this paper.

Throughout this paper, the term -pole voltage- will refer to the voltage difference between point A or B or C and point 0. The pole voltages V_{A0} , V_{B0} , and V_{C0} , are used for synthesising both line and phase voltages. For this reason, both of the two switching strategies are designed for controlling the used switches in a way to produce three-level voltage waveforms having phase shifts of 120° . As a result, five-level line voltages can be produced as shown in Fig. 1(b), where the line voltage V_{AB} is constructed by subtracting V_{A0} from V_{B0} .

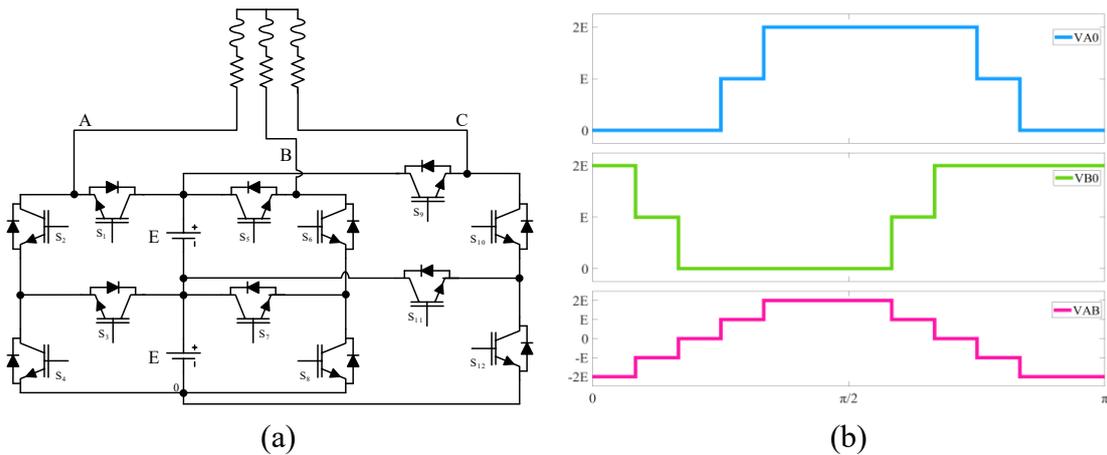


Fig. 1. The proposed three-phase multilevel topology. (a) The power circuit for the proposed topology. (b) Line voltage V_{AB} synthesization using pole voltages V_{A0} and V_{B0} .

III. COMPARISON OF THE PROPOSED TOPOLOGY WITH OTHER MLC TOPOLOGIES

Conventional multi-level converters, namely CHB, FC, and NPC have several shortcomings in both control and component count as mentioned in section I. To overcome these limitations, new and modified topologies have been reported in [14-20]. These topologies aim to decrease the component count while increasing efficiency and reliability. Although these configurations are widely used in industrial applications, some of them are still in investigation and improvement stages. Table I summarises the results of a comparative strategy regarding the required components for producing an equal number of voltage levels.

The comparative strategy is based on unified constraints as follows: producing three-level pole voltages for each topology, using only symmetrical DC sources, i.e. DC voltage source has a rating $2E$ was counted as two DC sources each has a rating of E , single-phase topology being converted to a three-phase version before comparison. Table I shows a comparison between the proposed topology and existing circuits in literature in term of the component count at the same voltage levels and the mentioned constraints. The proposed topology can produce the same output voltage levels while using a lower component count as compared to the other three-level configurations. The main advantages of the proposed topology are capacitor-, diode-, and inductor-free, allowing the proposed MLC to have a longer lifetime, lower switching losses, and compact design. The main characteristics and limitations of the compared topologies are highlighted and discussed in the following paragraphs.

TABLE I. COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND THREE-LEVEL MLC TOPOLOGIES

Topology	DC Sources	Switches	Diodes	Capacitors	Inductors	Total	CLF ^a
Modified T-type [19]	1	9	12	2	0	24	8.0
Fig. 8 in [16]	3	9	9	0	3	24	8.0
In [18]	1	18	0	3	0	22	7.3
Neutral point clamped (NPC)	1	12	6	2	0	21	7.0
Active T-type converter [14, 17]	1	18	0	2	0	21	7.0
In [20]	1	12	3	4	1	21	7.0
Cascaded half H-Bridge (CHHB)	6	12	0	0	0	18	6.0
Flying capacitors (FCs)	1	12	0	4	0	17	5.7
Cascaded full H-bridge (CHB)	3	12	0	0	0	15	5.0
T-type converter [14, 19]	1	12	0	2	0	15	5.0
Fig. 5 in [15]	3	9	3	0	0	15	5.0
The proposed topology	2	12	0	0	0	14	4.7

^a Components per level factor [22]

In [20], a three-level topology was presented, which is an extension of the two-level split-source inverter (SSI) in [21]. It can generate a high-quality three-level output voltage with a boosting feature, making a direct connection of low-voltage energy sources, e.g. photovoltaics (PV), more accessible. For generating three-level, it requires one DC source, twelve semiconductor switches, three power diodes, four capacitors, and only one inductor. Although having features like multi-level outputs, boosting capability, and operating with an only single source, this topology suffers from high current and voltage stresses on the used semiconductor components, limited power transfer capability, increasing the system footprint and control-complexity due to capacitors and inductors, besides decreasing the expected lifetime of the converter. Further, the quality of the output voltage is a function of the gain value, i.e. at low voltages values, the THD of the output voltages rises when increasing the input voltage. Additionally, it needs extra efforts in control algorithms for removing the low-frequency components from not only input current but also output voltage caused by oscillations of flying capacitors voltages. Moreover, during starting, special precautions for limiting the

switch voltage stress and controlling the rise up time, like using soft-start-up-resistors is mandatory for grid-connected mode while in stand-alone mode, those issues can be controlled by especially setting of control parameters in control algorithm.

Authors in [18] have highlighted a new MLC using two main switches to change the polarity of the output voltages, and several groups of anti-parallel switches for level-generator stages. For producing three-level three-phase voltage, this topology requires eighteen switches, three capacitors, and one DC source. The main limitations for this circuit are using electrolytic capacitors for splitting one DC source to three equal divisions, requiring a high number of switches and having high voltage stress across switches, which are used for changing the polarity, resulting in different losses and heat distribution inside the converter. As a result, the converter cost, size, losses, and control complexity are increased while decreasing the system lifetime.

A dual-DC-port asymmetrical MLI (DPAMLI) was designed and analyzed in [15]. It requires nine switches, three power diodes, and three DC sources (two having E and one with $2E$) in order to generate three-level voltage for three-phase applications. The neutral point clamped (NPC) and T-type three-level cells are used for derivation of the suggested topology. Although the DPMLI can allow a bidirectional power flow between input and output ports, only a unidirectional version was highlighted and validated in [15] for the purpose of reducing the components count. It is a single-stage converter, being able to connect two DC sources, having different ratings and producing multilevel AC output voltages. This makes the connection of different voltage sources to the same converter easier and efficient. It has two different operating modes, which are selected by the controller according to the relationship between the required output voltage and the actual applied voltage across the low DC port terminals. Although it does not have any problem regarding using electrolytic capacitors, it uses power diodes, increasing losses in the converter. Further, at least six switches have high voltage stresses equal to the voltage applied across the high voltage DC port terminals, limiting this topology to be only applicable in low and medium voltage.

For the purpose of decreasing switch count, authors in [19] have presented a modified three-level topology of well-known T-type MLI. The three bidirectional switches between the load points and the clamped neutral point were replaced by a cell consisting of one switch and four diodes. This topology needs two capacitors, one DC source, twelve power diodes, and nine switches for producing the same output voltage levels as a conventional T-type topology. However, using capacitors and a high number of semiconductor components make this topology unattractive for many applications that require high efficiency, reliability, and smaller size.

Most of the voltage source converters (VSCs) are suffering from the shoot-through problem, resulting in decreasing their reliability and adding complexity in both control stage and protection circuits. One of the most common solutions is adding a deadtime between the complementary switches either by using software or hardware solutions. However, this solution renders several drawbacks such as distortion of output waveforms and increasing the power losses, especially when

using body diodes with a poor performance [16, 23, 24]. The shoot-through problem is a critical problem in MLI topologies due to having a higher number of power switches in different configurations. In [16], another solution is presented in the form of new dual-buck multilevel topologies, allowing splitting one switching leg into two legs. Although these configurations enhance the reliability degree and the control simplicity, they require a high component count in the power circuit. For example, the presented topologies require two DC sources, nine switches, nine power diodes, and three inductors for generating only three voltage levels when feeding three-phase load.

IV. MODULATION SCHEMES FOR THE PROPOSED CIRCUIT

Modulation schemes for MLCs are classified according to the switching frequency into two groups: fundamental and low-frequency modulation. All of these switching schemes are used for producing a specified AC voltage waveform across the converter outputs, increasing the magnitude of the output voltage, decreasing the harmonics contents in both output currents and voltages, and performing others services such as balancing of capacitors voltages and common-mode voltage reductions [6].

In this paper, two switching schemes are applied. The first one is based on a fundamental switching frequency, i.e., staircase modulation (SCM), while the other belongs to low frequency modulation, i.e. level-shifted pulse width modulation (LSPWM). The applied modulation schemes are designed for controlling the proposed topology to produce three-level 0, E, and 2E across pole voltage V_{A0} , five-level 2E, E, 0, -E, and -2E across line voltage V_{AB} , and seven-level $4/3 E$, E, $2/3 E$, 0, $-2/3 E$, -E, and $-4/3 E$ across phase voltage V_{AN} .

Table II summarises the twelve switching states that are used in SCM. These switching states are selected in a way to minimise the number of active switches at any instant to reduce the converter losses. Furthermore, LSPWM is implemented

Table II. The switching states and the corresponding pole voltages (X : ON, - : OFF)

V_{A0}	E	2E	2E	2E	2E	2E	E	0	0	0	0	0
V_{B0}	0	0	0	0	E	2E	2E	2E	2E	2E	E	0
V_{C0}	2E	2E	E	0	0	0	0	0	E	2E	2E	2E
S_1	-	X	X	X	X	X	-	-	-	-	-	-
S_2	X	-	-	-	-	-	X	X	X	X	X	X
S_3	X	-	-	-	-	-	X	-	-	-	-	-
S_4	-	-	-	-	-	-	-	X	X	X	X	X
S_5	-	-	-	-	-	X	X	X	X	X	-	-
S_6	X	X	X	X	X	-	-	-	-	-	X	X
S_7	-	-	-	-	X	-	-	-	-	-	X	-
S_8	X	X	X	X	-	-	-	-	-	-	-	X
S_9	X	X	-	-	-	-	-	-	-	X	X	X
S_{10}	-	-	X	X	X	X	X	X	X	-	-	-
S_{11}	-	-	X	-	-	-	-	-	X	-	-	-
S_{12}	-	-	-	X	X	X	X	X	-	-	-	-

by using two symmetrical carrier signals C_{R1} and C_{R2} . These signals have the same magnitude of C_{RM} and phase while having a level shift of C_{RM} . The number of carrier signals N_{CR} is related to the output voltage levels across the pole terminals N by (1) [8].

$$N_{CR} = N - 1 \quad (1)$$

The LSPWM scheme uses three sinusoidal modulation signals, having a magnitude of C_{RM} and a phase-shift of 120° . These signals are compared with C_{R1} and C_{R2} for generating two Boolean signals X and Y . Then the switching signals are produced by executing logical operations on X and Y as described in the proposed equations (2)-(5).

$$S_1 = X \quad (2)$$

$$S_2 = \overline{X} \quad (3)$$

$$S_3 = Y \quad (4)$$

$$S_4 = \overline{Y} \quad (5)$$

Fig. 2 shows the LSPWM switching scheme for phase A, including the pole voltage for phase A - V_{A0} , two carrier signals C_{R1} , C_{R2} , one sinusoidal modulation signal S_M , two Boolean signals X , Y , and four switching signals for phase A, i.e., S_1 , S_2 , S_3 , and S_4 .

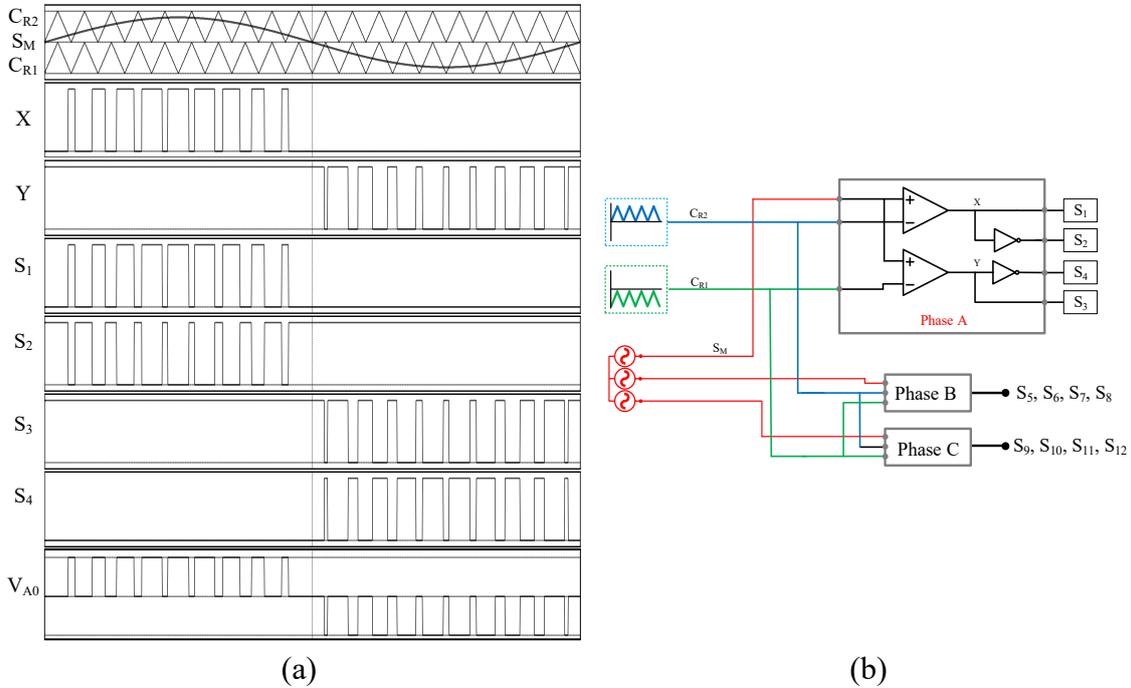


Fig. 2. The LSPWM switching scheme for the proposed converter. (a) Switching patterns for phase A. (b) Block diagrams for the Boolean operations.

V. SIMULATION RESULTS AND DISCUSSIONS

To illustrate the working principles of the proposed topology, a three-level model is designed and simulated not only for a fundamental frequency modulation but also for a pulse width modulation technique. The simulated model uses two symmetrical DC voltage sources and twelve switches (nine of E volt and three of $2E$ volt) to produce a three-level pole voltage. Table III provides the main simulation parameters, while the PSIM software has been used for obtaining the simulation results.

Fig. 3 shows the pole voltages V_{A0} , V_{B0} , and V_{C0} when the proposed converters are modulated by SCM and LSPWM switching schemes. By keeping the voltage across pole terminals have three steps and a phase shift of 120° , five-level balanced three-phase line voltages V_{AB} , V_{BC} , and V_{CA} will be generated at the load terminals as shown in Fig. 4. Fig. 5 shows the simulated results for the proposed topology when supplying power to a resistive-inductive load with a power factor of 0.9.

TABLE III. SIMULATION SYSTEM MAIN SPECIFICATIONS

System parameters	Value
DC voltage value E	100 V
Load value at 50 Hz	$R=50 \Omega$, $X_L=23.6 \Omega$
Switching Frequency F_s	2.5 kHz
Modulation index $M_i (= \sin_M / C_{RM})$	1

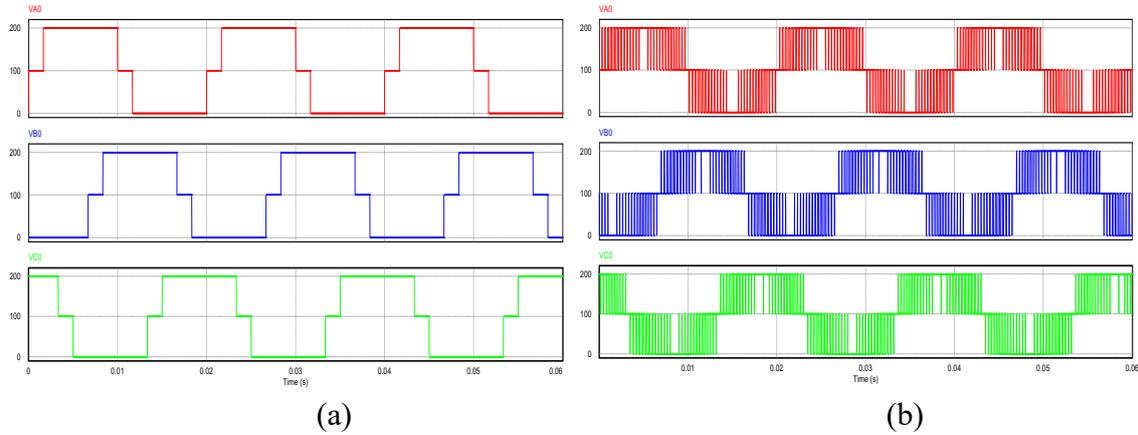


Fig. 3. The pole voltage waveforms: V_{A0} , V_{B0} , and V_{C0} . (a) staircases modulation. (b) Level-shifted PWM.

By comparing the two graphs for V_{AN} in Fig. 5 (a) and (b), it can be seen that the voltage level number is different consistent with the applied switching scheme. V_{AN} has seven levels of $-4/3 E$, $-E$, $-2/3 E$, 0 , $2/3 E$, E , $4/3 E$ for SCM and nine levels of $-4/3 E$, $-E$, $-2/3 E$, $-1/3 E$, 0 , $1/3 E$, $2/3 E$, E , $4/3 E$ for LSPWM. The two extra voltage levels in $V_{AN} \pm 1/3 E$ are generated because of two new voltage combinations in the pole voltages when using LSPWM switching scheme. Table IV and (6) [25] provide more clarification regarding the effect of switching schemes on the phase voltage level number.

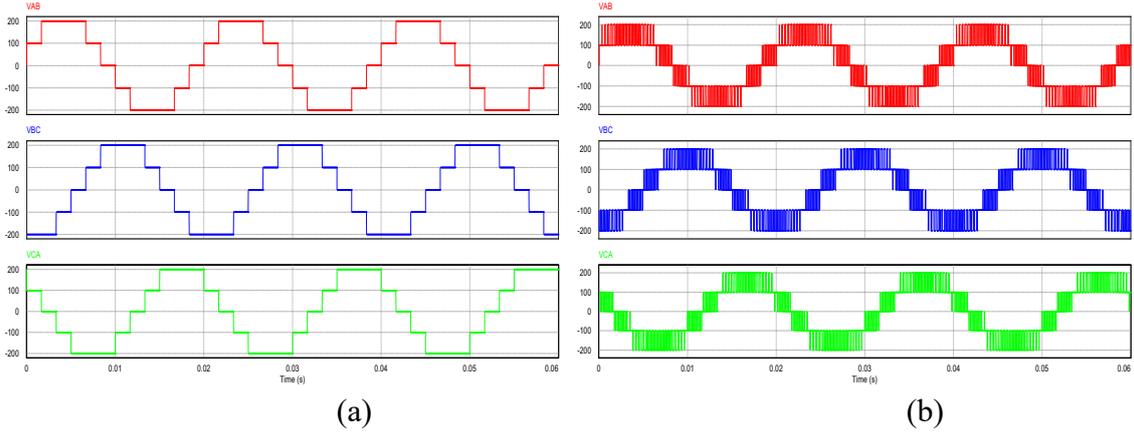


Fig. 4. The output line voltage waveforms: V_{AB} , V_{BC} , and V_{CA} . (a) Staircases modulation. (b) Level-shifted PWM.

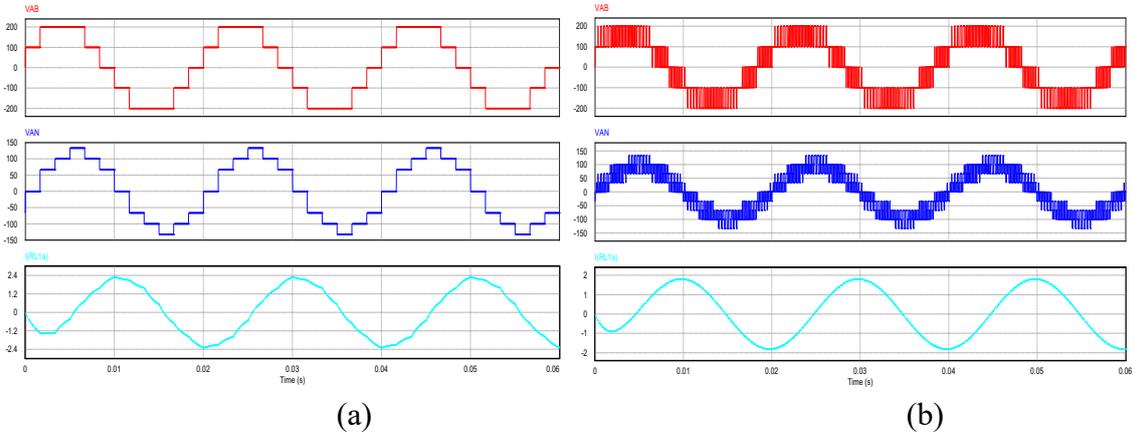


Fig. 5. The output waveforms under R-L load: V_{AB} , V_{An} , and I_{An} . (a) Staircases modulation. (b) Level-shifted PWM.

TABLE IV. THE SWITCHING MODULATION EFFECTS ON THE NUMBER OF LEVELS OF THE PHASE VOLTAGE V_{AN}

V_{A0}		V_{B0}		V_{C0}		V_{AN}	
SCM	LSPWM	SCM	LSPWM	SCM	LSPWM	SCM	LSPWM
2E	2E	0	0	0	0	4/3 E	4/3 E
2E	2E	E	E	0	0	E	E
2E	2E	2E	E	0	E	2/3 E	2/3 E
–	E	–	E	–	0	–	1/3 E
E	E	2E	2E	0	0	0	0
–	E	–	2E	–	E	–	-1/3 E
0	0	2E	2E	0	0	-2/3 E	-2/3 E
0	0	2E	2E	E	E	-E	-E
0	0	2E	2E	2E	2E	-4/3 E	-4/3 E

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \times \begin{bmatrix} V_{A0} \\ V_{B0} \\ V_{C0} \end{bmatrix} \quad (6)$$

VI. CONCLUSION

A new three-level multilevel inverter is proposed and analysed in this study. The proposed topology can generate a three-level pole voltage without using any passive component. Further, it requires a low component count as compared to other existing three-level topologies. Two modulation strategies based on fundamental frequency modulation and sinusoidal pulse width modulation are effectively applied for producing three balanced three-phase output voltages. The effectiveness of the proposed topology is verified via a simulation model of the circuit and resistive-inductive load. Moreover, a comparative study is carried out to highlight the advantage of the proposed circuit and provide a view on the design trade-off and selection of suitable multilevel converter topologies.

REFERENCES

- [1] M. Faisal, M. A. Hannan, P. J. Ker, A. Hussain, M. B. Mansor, and F. Blaabjerg, "Review of Energy Storage System Technologies in Microgrid Applications: Issues and Challenges," *IEEE Access*, vol. 6, pp. 35143-35164, 2018.
- [2] M. V. Pronin, O. B. Shonin, A. G. Vorontsov, and G. A. Gogolev, "Features of a drive system for pump-storage plant applications based on the use of double-fed induction machine with a multistage-multilevel frequency converter," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, pp. DS1b.7-1-DS1b.7-8.
- [3] J. Janning and A. Schwery, "Next generation variable speed pump-storage power stations," in *2009 13th European Conference on Power Electronics and Applications*, 2009, pp. 1-10.
- [4] M. Pronin, O. Shonin, A. Vorontsov, and G. Gogolev, "A pumped storage power plant with double-fed induction machine and cascaded frequency converter," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1-9.
- [5] A. Joseph and T. R. Chelliah, "A Review of Power Electronic Converters for Variable Speed Pumped Storage Plants: Configurations, Operational Challenges, and Future Scopes," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 103-119, 2018.
- [6] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631-1656, 2017.
- [7] H. Akagi, "Multilevel Converters: Fundamental Circuits and Systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2048-2065, 2017.
- [8] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37-53, 2015.
- [9] R. H. Baker, "Switching circuit," ed: Google Patents, 1980.
- [10] A. Nabae, I. Takahashi, and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518-523, 1981.

- [11] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 397-403 vol.1.
- [12] J.-P. Lavieville, P. Carrere, and T. Meynard, "Electronic circuit for converting electrical energy, and a power supply installation making use thereof," ed: Google Patents, 1997.
- [13] R. H. Baker and L. H. Bannister, "Electric power converter," ed: Google Patents, 1975.
- [14] Y. Wang, W. W. Shi, N. Xie, and C. M. Wang, "Diode-Free T-Type Three-Level Neutral-Point-Clamped Inverter for Low-Voltage Renewable Energy System," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 11, pp. 6168-6174, 2014.
- [15] H. Wu, L. Zhu, F. Yang, T. Mu, and H. Ge, "Dual-DC-Port Asymmetrical Multilevel Inverters With Reduced Conversion Stages and Enhanced Conversion Efficiency," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 2081-2091, 2017.
- [16] F. Yang, H. Ge, J. Yang, R. Dang, and H. Wu, "A Family of Dual-Buck Inverters With an Extended Low-Voltage DC-Input Port for Efficiency Improvement Based on Dual-Input Pulsating Voltage-Source Cells," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3115-3128, 2018.
- [17] R. Katebi, J. He, and N. Weise, "Investigation of Fault-Tolerant Capabilities in an Advanced Three-Level Active T-Type Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 1, pp. 446-457, 2019.
- [18] R. G. Ganesan, M. Bhaskar, and K. Narayanan, "Novel 11-level Multi-level Inverter," in *2018 IEEE Innovative Smart Grid Technologies - Asia (ISGT Asia)*, 2018, pp. 1050-1055.
- [19] C. L. Solanki, M. H. Ayalani, and S. N. Gohil, "Performance of Three Phase T-Type Multilevel Inverter with Reduced Switch Count," in *2018 International Conference on Current Trends towards Converging Technologies (ICCTCT)*, 2018, pp. 1-5.
- [20] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three-Phase Three-Level Flying Capacitors Split-Source Inverters: Analysis and Modulation," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4571-4580, 2017.
- [21] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three-Phase Split-Source Inverter (SSI): Analysis and Modulation," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7451-7461, 2016.
- [22] A. Salem, E. M. Ahmed, M. Orabi, and M. Ahmed, "New Three-Phase Symmetrical Multilevel Voltage Source Inverter," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 3, pp. 430-442, 2015.
- [23] A. Datta, A. Guha, and G. Narayanan, "An advanced gate driver for insulated gate bipolar transistors to eliminate dead-time induced distortions in inverter output," in *2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2014, pp. 1-6.
- [24] B. Weber, T. Brandt, and A. Mertens, "Compensation of switching dead-time effects in voltage-fed PWM inverters using FPGA-based current oversampling," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 3172-3179.

- [25] O. Kukrer, "Deadbeat control of a three-phase inverter with an output LC filter," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 16-23, 1996.