Minority carrier lifetime variations in multicrystalline silicon wafers with temperature and ingot position

Sissel Tind Søndergaard[1], Jan Ove Odden[2], and Rune Strandberg[1]

[1]University of Agder, Grimstad, Norway
[2]Elkem Solar AS, Kristiansand, Norway

Abstract **— The minority carrier lifetimes of multicrystalline silicon wafers are mapped using microwave photoconductive decay for different temperatures and ingot positions. Wafers from the top of the ingot display larger areas with lower lifetimes compared to wafers from the bottom. The lifetimes of low-lifetime areas are found to increase with the temperature, while the lifetimes of some high-lifetime areas decrease or remain unchanged. The relative improvement of the low-lifetime areas is considerably larger than the relative change in the high-lifetime areas. We suggest that the above-mentioned observations explain, at least partially, why previous studies have found the relative temperature coefficients of mc-Si cells to improve towards the top of the ingot.**

A.I. Introduction

The performance of a silicon solar cell depends on the minority carrier lifetime, which is affected by several parameters such as temperature, injection level and the type and concentration of impurities in the cell [1−4]. The temperature dependence of the lifetime should be of special interest for industrial purposes since field operation temperatures can be relatively high, negatively affecting the power output from the cell [5].

Multicrystalline (mc-Si) wafers made from a polycrystalline feedstock (poly-Si) are

widely used for industrial production of silicon solar cells due to the cost-effectiveness of the fabrication process. However, a relatively large and uneven distribution of impurities and crystal defects can be found throughout the ingot because of the quality of the feedstock and the solidification process [6, 7]. Several papers have shown that the minority carrier lifetime of mc-Si wafers varies with the wafer position in the ingot and this effect is considered to be impurity related [3, 8]. In recent work, it has been shown that the temperature coefficients of solar cells made from mc-Si vary along the height of an ingot [9]. A natural question to be raised is thus whether temperature variations affect the minority carrier lifetime differently throughout the ingot. Investigating this might provide information about how to optimize cells originating from different positions in an ingot as well as improve our understanding of how silicon cells perform in the field.

The present work is a study of the variations in minority carrier lifetime of mc-Si wafers, combining the effect of temperature and ingot position using microwave photoconductive decay (μ-PCD). The lifetimes are mapped at room temperature and at an elevated temperature of 56 °C, which is close to temperatures often encountered in the field.

A.II. Experimental Details

The studied samples were mc-Si wafers made from directional solidification of a poly-Si feedstock, produced industrially and passivated with a layer of 43 nm a-Si:H in a research laboratory. The lifetimes were measured using μ-PCD in a Semilab WT-2000PVN. To heat the wafers, a heat plate with a top section consisting of a thick slab of sintered aluminum oxide (alsint) was used. This material is an electrical insulator and the thickness of the slab ensures that underlying metallic parts do not interfere with the lifetime measurements. To secure exactly similar conditions, the wafers were placed on the heat plate also when mapping lifetimes at room temperature.

To control the repeatability of the lifetime measurements, one particular wafer was mapped at several occasions throughout the period through which the series of measurements was conducted. The results of these repeated control measurements are shown in Fig. A.1 where the shortest measured lifetime is presented as a function of measurement number. The error bars show the standard deviation of the 23 °C and the 56 °C measurements, respectively. The measured lifetimes change slightly during the period considered, however within the statistical fluctuations.

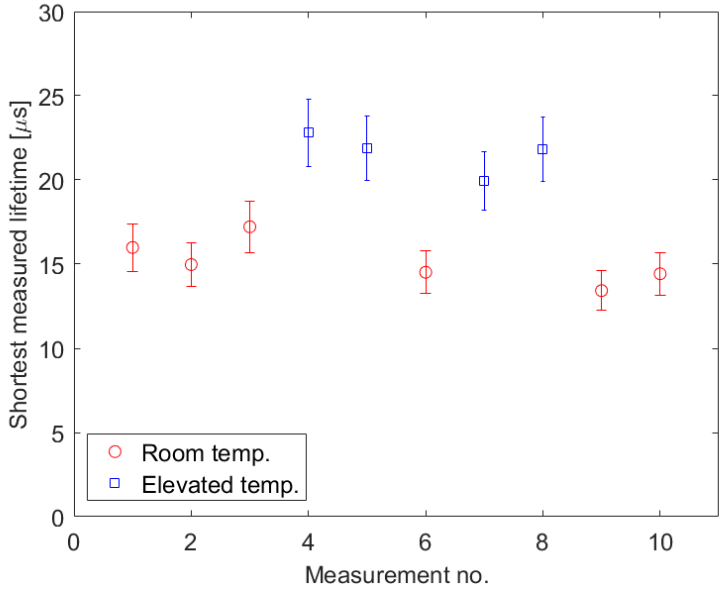

Figure A.1: Repeated control measurements of the shortest measured lifetime on a wafer. The error bars show the standard deviation of the 23 °C and the 56 °C measurements, respectively.

A.III. Results

The average lifetime of each wafer is shown in Fig. A.2 as a function of the position of the wafer in the ingot. Position 1 indicates the wafer closest to the bottom whereas 600 is close to the top. The average lifetime is found to increase by 3.4 % on average when the temperature is increased from 23 °C to 56 °C. However, conducting a Student's t-test, the difference in lifetimes with temperature is not found to be statistically significant. Furthermore, we observe a tendency that the average lifetime decreases throughout the ingot, which matches results in the literature [3, 8, 10].

The 0.1 % pixels with the longest measured lifetime on each wafer is shown in Fig. A.3 as a function of the wafer position. The longest lifetime decreases by 6.5 % on average when the temperature is increased, however this decrease is also not found to be statistically significant. Furthermore, we observe the tendency that the longest measured lifetime is lowest towards the top of the ingot.

The 0.1 % pixels with the shortest measured lifetime on each wafer is shown in Fig. A.4 as a function of the wafer position. The shortest lifetime is found to increase by 47.3 % on average when the temperature is increased. Furthermore, we observe a tendency that the shortest measured lifetime takes the shortest value at the top of the ingot.

A consistent increase in lifetime with temperature was found for areas on the wafers with lifetimes below 50 μs. The fraction of pixels on each wafer with lifetimes below 50 μs is shown in Fig. A.5 as a function of the wafer position. The fraction decreases by 55.3 %

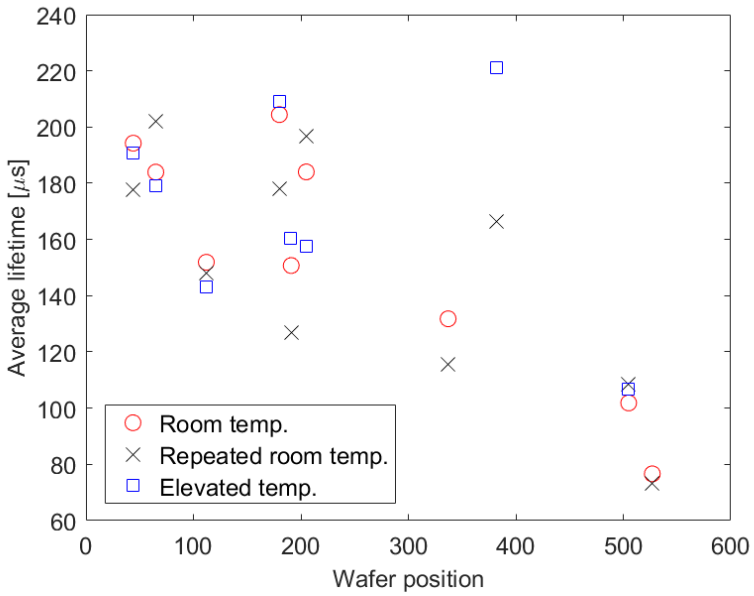

Figure A.2: Average lifetime of each wafer as a function of wafer position.

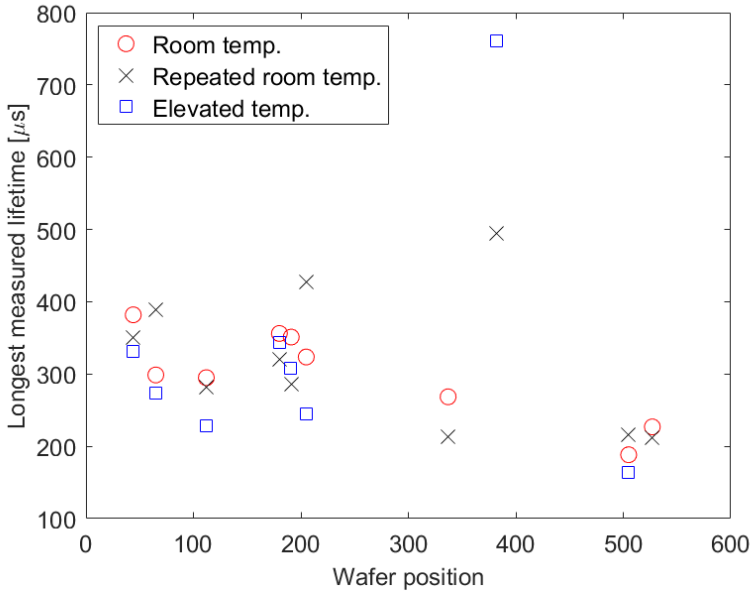

Figure A.3: 0.1 % pixels with longest measured lifetime as a function of wafer position.

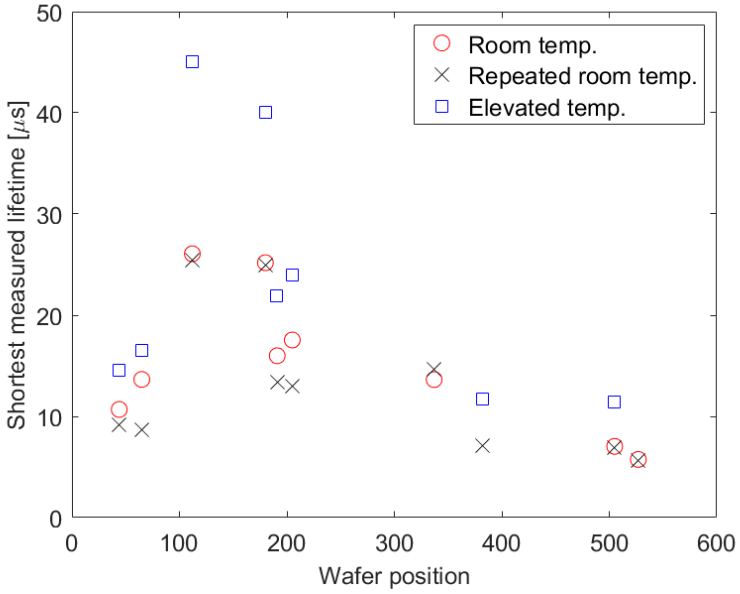

Figure A.4: 0.1 % pixels with shortest measured lifetime as a function of wafer position.

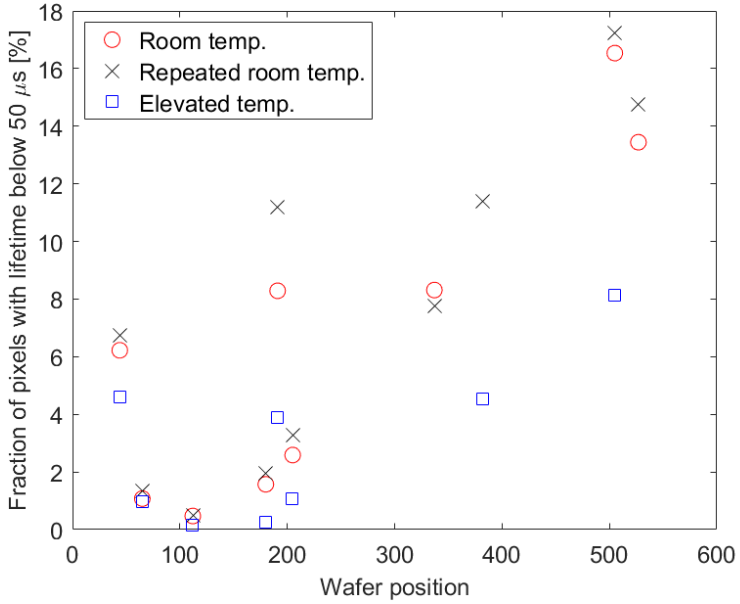

Figure A.5: Fraction of pixels with lifetime below 50 μs as a function of wafer position.

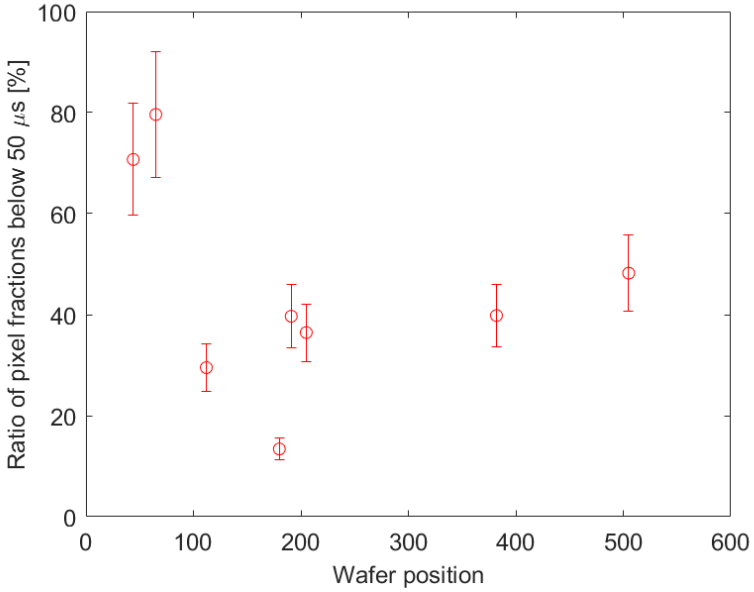

Figure A.6: Ratio of fractions of pixels with lifetime below 50 μs at 56 °C to 23 °C as a function of wafer position. The error bars are estimated from the standard deviation of repeated control measurements.

on average when the temperature is increased. In addition, Fig. A.5 shows the tendency that the wafers at the top of the ingot consist of a larger number of pixels with lifetimes below 50 μs. This matches the tendency found in Fig. A.4 where the shortest measured lifetime was shortest at the top of the ingot.

To visualize the effect of the temperature change, some additional data of the $< 50\,\mu$s areas are plotted in Fig. A.6. It shows the ratio of the fraction of pixels with lifetimes below 50 μs at 56 °C to the same fraction at 23 °C. Hence a low ratio corresponds to a drastic decrease in the number of low lifetime pixels when the temperature is increased. The error bars are estimated from the standard deviation of repeated control measurements of the lifetimes below $< 50\,\mu$s. This was calculated for one particular wafer and generalized to the remaining wafers.

We observe that the number of low-lifetime pixels decreases for all wafers when the temperature is increased. In addition, we see a tendency that the wafers from the middle and the top of the ingot seem to benefit considerably from the temperature increase, whereas the effect is relatively small for wafers from the bottom. Because of the low number of measurements this should only be interpreted as a possible trend. From Fig. A.6, we would expect a constant ratio throughout the ingot. However, the change in composition and distribution of impurities throughout the ingot might cause the wafers to respond differently to temperature changes, as will be discussed later.

A further investigation of the temperature effect can be seen in Fig. A.7, which shows

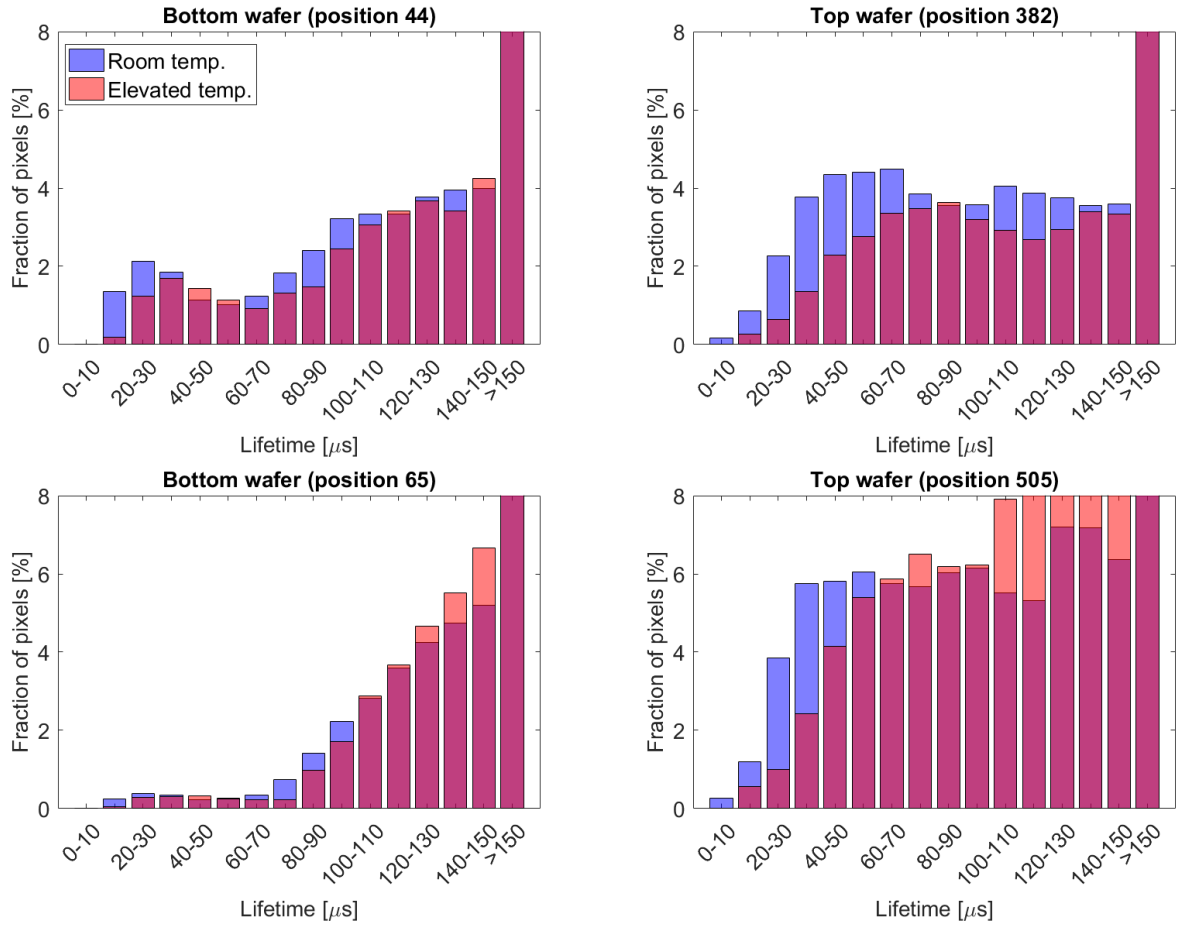

Figure A.7: Fraction of pixels of different low-lifetime intervals for bottom and top wafers.

the fraction of pixels in different lifetime intervals for two bottom and two top wafers at the relevant temperatures. The top wafers are found to consist of a larger fraction of pixels with lifetimes below 50 μs compared to bottom wafers, consistent with the trend observed in Fig. A.5. This fraction decreases with temperature for all lifetime intervals below 50 μs for top wafers, while this is not always the case for bottom wafers. Furthermore, the decrease seems to be larger for top wafers. The number of pixels with lifetimes above 150 μs responds differently to the temperature increase for the different wafers as shown in Fig. A.8. Some of the wafers experience a shift of the pixels towards lower lifetimes, whereas one of the top wafers display the opposite trend (note that the lifetime intervals for "top wafer (position 382)" differ from the other wafers). This shows that an increase in temperature in general is beneficial for areas with low lifetime but not necessarily for areas with a high lifetime.

A PC1D simulation is shown in Fig. A.9 relating the cell efficiency to the carrier lifetime at the two relevant temperatures. The simulation is based on standard cell parameters. For cells with lifetimes above 50 μs, a temperature increase results in a relatively large

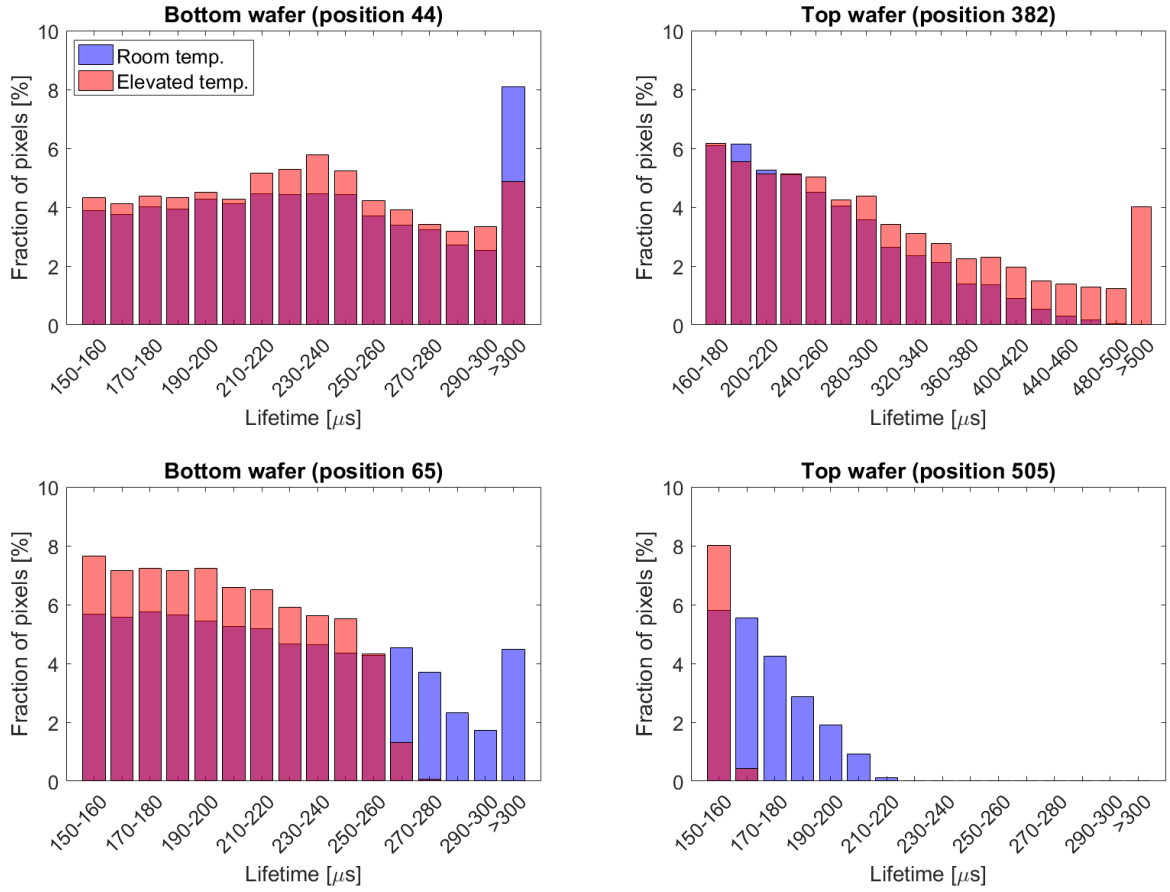

Figure A.8: Fraction of pixels of different high-lifetime intervals for bottom and top wafers. Note that the intervals for top wafer (position 382) differ from the other wafers.

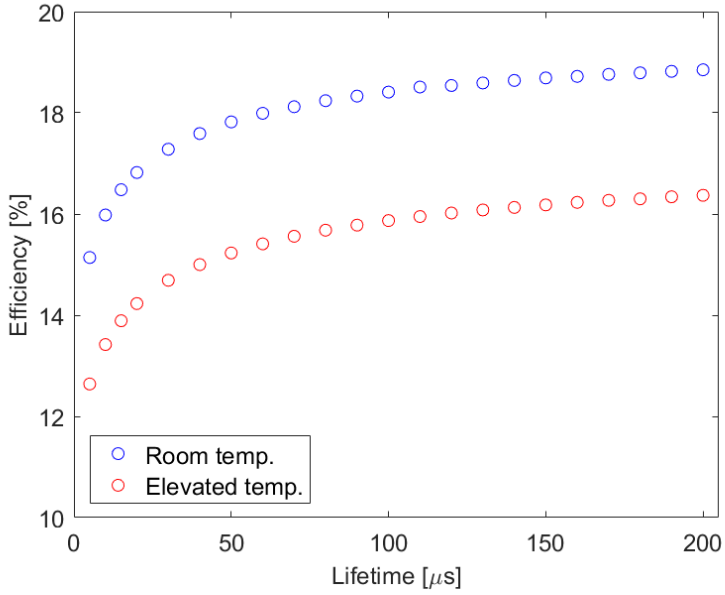

Figure A.9: PC1D simulation of cell efficiency as a function of lifetime.

efficiency reduction regardless of how the lifetime changes. For cells with lifetimes below 50 μs, an increase in temperature results in a significantly smaller efficiency reduction if the lifetime increases with the temperature, as is the case for the low-lifetime areas in this study. Since wafers from the top of the ingot in general show larger areas with low lifetimes, the relative performance of such cells is expected to decrease less with temperature compared to cells originating from the bottom of the ingot. Consequently, we expect the top cells to show better temperature coefficients, which agrees with the results in Ref. [9].

During the directional solidification of mc-Si, the majority of impurities will segregate towards the top of the ingot leaving a higher concentration of impurities in this area [8]. In addition, back diffusion from the crucible into the ingot can result in a higher concentration of impurities with large diffusion coefficients right at the bottom of the ingot [6]. An uneven distribution and composition of impurities might cause the wafers to respond differently to temperature changes and the wafers from the top of the ingot to display better temperature coefficients. This seems plausible since the capture cross sections of different impurities depend differently on temperature and might decrease, as observed for iron, copper, molybdenum and titanium [4, 11-13].

A.IV. Conclusion

The minority carrier lifetimes of mc-Si wafers have been studied for different temperatures and ingot positions. We found that wafers from the top of the ingot contained larger areas with lifetimes below 50 μs compared to wafers from the bottom. Areas with lifetimes below 50 μs in general experienced an increased lifetime when the temperature was increased. In high-lifetime areas, the lifetime decreased with temperature for some of the wafers, whereas others increased or remained constant.

These findings are believed to be impurity related, since the composition and distribution of impurities change throughout the ingot and in general is found to be larger at the top. Since the capture cross sections of some impurities decrease with temperature, this could explain why temperature coefficients previously have been found to be better for cells originating from the top of an ingot.

Acknowledgment

We would like to thank Gaute Stokkan at SINTEF, for generously sharing the heat plate with us, and Elin Stubhaug and Ragnar Ekker, who designed and made the heat plate as a part of their Masters project at NTNU.