Multiport DC-DC Converters for Hybrid Energy Systems

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UiA University of Agder

Doctoral Dissertations at the University of Agder 423

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Doctoral Dissertation for the Degree *Philosophiae Doctor (PhD)* at the Faculty of Engineering and Science, Specialisation in Renewable Energy

University of Agder
Faculty of Engineering and Science
2023

Doctoral dissertations at the University of Agder 423
ISSN: 1504-9272
ISBN: 978-82-8427-139-2

Printed by Make!Graphics
Kristiansand, Norway

Acknowledgements

I am humbled and grateful to have reached this milestone in my academic journey, and I would like to take a moment to acknowledge the many individuals who have in one way or the other contributed to the completion of this work.

Firstly, I would like to express my sincere appreciation to my supervisor, Prof. Huynh van Khang for his unwavering guidance, support, and mentorship. His expertise, intellectual curiosity, and insightful feedback have been indispensable throughout the course of my research. Your commitment to my academic development and well-being has been a source of great inspiration and motivation. In the league of super-sport agents and football managers like Jorge Mendes and José Mourinho, I consider you a super supervisor. I would also like to extend my gratitude to Prof. Rade Ciric, my co-supervisor, and Prof. Nand Kishor, an external volunteer collaborator on the PhD project, for their valuable feedback, constructive criticism, and challenging questions. Their insightful comments and suggestions have contributed significantly to the quality of this work, and I am deeply grateful for their time and effort. To Steve Schading, your help and technical support with fabrication and modification of equipment and tools is deeply appreciated.

I would also like to thank the many institutions and organizations that have supported my research, especially the Research Council of Norway. Their financial support has enabled me to pursue this research with vigor and enthusiasm. And to Prof. Yunwei Li of the University of Alberta, Edmonton, Canada, I am deeply grateful for their investment in my academic development, through the opportunity to conduct a six-month research visit in this Lab. Also, to Emma Elisabeth Horneman of the PhD Program Committee for Engineering (PPCE) for her efforts and help administratively and other things during my fellowship and studentship at the University of Agder (UiA). Your proactive attitude to your work and responsiveness to requests made my study life a lot easier.

My gratitude also goes to my family, especially my Mum and Dad, Prof. Elisha and Florence Jiya, my siblings, Jemimah and Nasara, I am forever grateful for your love, support, and encouragement. To my uncles and aunties, Mr. & Mrs. Obadiah & Sarah Jiya, Mr. & Mrs. John & Comfort Jiya, Mr. & Mrs. Andrew Jiya, Mr. & Barr. (Mrs.) Emmanuel and Martha Sule, Mr. & Mrs. Enock & Mary Jiya, Mr. & Mrs. Peter & Susan Jiya, your unwavering belief in me and your constant reassurance has been a source of strength and inspiration throughout my journey. And to my cousins, Dr. J. Y. Jiya (Ya Joe), Ya Yebo, Babayisa, Ya Victor, Uncle

Dauda, Samuel Samson, Samuel Jiyah, Joshua Jiya, and Mike Sule to list just a few, thank you for always being there for me, even when I couldn't be there for you.

I am also deeply grateful to my colleagues, Ghali Yakoub, Haidar Hosamo, Thomas Ferriday, Milad Golzar, Basant Paudyal, Arild Husebø, Jayachandra Malavatu, Pasan Gunawardena, Juan Pardo, Juan Diego, Raju Shrestha, Sarang Kumar, Rohan Money, Drs. Saba Mirza, Salem Ahmed, Nils Johannesen, Antoine Shyikira, Gulshan Noorsumar, Dipendra Subedi, Paula Molina, Carla Terron and Assoc. Prof. Jagath Senanayaka, for their camaraderie. The countless hours spent discussing ideas, sharing resources, and offering feedback have created a stimulating intellectual environment that has enriched my academic experience. I would also like to express my appreciation to my friends, Ayomide, Oscar Segbefia, Solomon Adamako, David Offo, Dr. Ofuafo Ajari, Marvelous Kasali, Joshua James, Christiana Stevens, Janet Carboo, Pius Oladoyin, Precious Maigeri, Dika Ututu, Jeremy Aweda, Yommy Madamori, Abigail Doshima, and Hannah Richi, for their unwavering support and encouragement during some of the challenging moments of my PhD journey.

I am particularly grateful to Profs. Abraham Usman, Jacob Tsado, Olushola Alabi, Rupert Gouws, Job Nmadu, Dr., and Dr. (Mrs.) Ogunrombi, Mr. Akin Ibimidun, Engr. Daniel Shaba, Dr. Bala Shehu, Dr. and Mrs. Abaya, Pastor Tunde Raji, and Evangs. Kayode and Fumi Olutimehin, whose unwavering encouragement, support, and belief in me has been a constant source of strength throughout my academic journey. Their support has provided a safe haven during the many moments of doubt and uncertainty.

Finally, I would like to dedicate this thesis to my Lord and King, God almighty, for the gift of salvation through his son Jesus Christ and for the Holy spirit whose inspiration and insight has been the cornerstone of my success. His love for me has provided a foundation of strength and resilience, and I could not have reached this point without Him.

In conclusion, I would like to extend my deepest appreciation to everyone who has supported me throughout my journey towards completing this thesis. Your unwavering support, encouragement, and belief in me have been instrumental in helping me to achieve this milestone, and for that, I am forever grateful.

Summary

Renewable energy sources (RESs) like solar and wind have gained attention for their potential to reduce reliance on fossil fuels and mitigate climate change. However, integrating multiple RESs into a power grid is challenging due to their unpredictable nature. Power electronic converters can manage hybrid energy systems by controlling power flow between RESs, storages, and the grid. Conventional single input dc-dc converters have limitations such as low efficiency, bulky designs, and complex control systems. Multiport dc-dc converters (MPCs) have emerged as a solution for hybridizing multiple sources, storages, and load systems by providing a common interface. Existing MPCs have limitations such as high component count, limited operational range, complex control strategies and restrictions on the number of inputs to list a few. Thus, there is a need to develop new MPCs that combine the advantages of existing designs while overcoming their limitations. Isolated MPCs with unipolar or bipolar outputs are needed that can accommodate any number of inputs, offer high voltage gain, use fixed magnetic components for galvanic isolation (regardless of the number of ports), and have a simplified control strategy. Additionally, new non-isolated MPCs with unipolar or bipolar outputs are required, featuring reduced component count, simultaneous power transfer and power flow between input ports, high voltage gain, low control complexity, and modular design allowing for arbitrary increase in the number of input ports. There is also an opportunity to apply MPCs in the integration of RESs and storages to ac grids through multilevel inverters for low component count, high efficiency, low harmonics, and higher power density. Further, advances in bipolar MPCs provide the chance to balance the dc bus without requiring a complex control system.

In this dissertation, five novel MPC topologies (T_A to T_E) of non-isolated (T_A, T_B and T_D) and isolated (T_C and T_E) configuration with unipolar (T_A, to T_C) and bipolar outputs (T_D and T_E) were developed and verified for various hybrid energy system applications. All these contributions were made in eight publications (Papers I – VIII), including three journals and five conference papers. These papers are listed in Chapter 1, highlighting the details of their specific contributions, respectively. Further, the ac grid integration through integrating some of the MPCs (T_A and T_D) with MLIs were explored and validated. The integration of the bipolar MPCs to bipolar dc transmission/distribution infrastructure with the possibility of supplying a critical unipolar dc load was also verified. The initial idea of T_A, a new non-

isolated MPC with unipolar outputs was presented in paper I with more detailed analysis and the experimental validations presented in paper II. Paper III presents T_C, an isolated MPC topology with unipolar outputs, along with key results. Paper IV, presents T_D, a novel family of non-isolated MPCs with bipolar outputs, and key results including the ac grid integration using an MLI is verified in this paper. In paper V, a modified unidirectional version of T_A was used to achieve the unipolar dc to ac grid integration, verifying the use of an auxiliary circuit and control-based approach for balancing the dc link voltage. Paper VII presents T_B, an improvement to T_A, which allows for power flow between the RES ports and the energy storage ports. The initial idea of T_E, a new isolated MPC with bipolar outputs was presented in paper VI with more detailed analysis, and the experimental validations were implemented in paper VIII. The verification of integrating T_E to a bipolar dc distribution infrastructure supplying a critical unipolar dc load was also presented in paper VIII. The steady state operation of these new MPC topologies was analysed mathematically and verified using detailed simulation and validated on an in-house hardware-in-the-loop (HIL) platform and on an experimental test rig, respectively. The novelty of the proposed MPC topologies is highlighted through detailed comparative studies, underscoring some important metrics such as component count, modularity, and voltage gain to list just a few. The development of these converters can significantly contribute to the integration of RESs and storages into the power grid and promote sustainable energy practices. This dissertation has five main chapters: the first presents the introduction and background to MPC, the second reviews the state of the art while the third and fourth presents the new MPCs proposed herein and the main results, respectively, and a concluding Chapter 5 at the end, highlighting the key findings and the limitations of this PhD study.

Sammendrag

Fornybare energikilder (RESs) som sol- og vindenergi har fått oppmerksomhet for sitt potensial til å redusere avhengigheten av fossile brensler og begrense klimaendringer. Imidlertid er det utfordrende å integrere flere RES-er i strømnettet på grunn av deres uforutsigbare natur. Kraftomformere med kraftelektronikk kan håndtere hybride energisystemer ved å kontrollere kraftflyten mellom RES-er, lagringsenheter og nettet. Konvensjonelle enkeltinngang DC-DC-omformere har begrensninger som lav effektivitet, klumpete design og komplekse kontrollsystemer. Multippel inngang DC-DC-omformere (MPC-er) har blitt en løsning for å kombinere flere kilder, lagringsenheter og lastsystemer ved å gi en felles grensesnitt. Eksisterende MPC-er har begrensninger som høyt komponenttall, begrenset operasjonsområde, komplekse kontrollstrategier og begrensninger på antall innganger, for å nevne noen. Det er derfor behov for å utvikle nye MPC-er som kombinerer fordelene med eksisterende design samtidig som de overvinner deres begrensninger. Det trengs isolerte MPC-er med unipolare eller bipolare utganger som kan romme et hvilket som helst antall innganger, tilby høy spenningsgevinst, bruke faste magnetiske komponenter for galvanisk isolasjon (uavhengig av antall porter) og ha en forenklet kontrollstrategi. I tillegg kreves det nye ikke-isolerte MPC-er med unipolare eller bipolare utganger, med redusert antall komponenter, samtidig kraftoverføring og kraftflyt mellom inngangsportene, høy spenningsgevinst, lav kontrollkompleksitet og modulært design som tillater vilkårlig økning i antall inngangsporter. Det er også muligheter for å bruke MPC-er i integreringen av RES-er og lagringssystemer i AC-nett gjennom flernivåinvertere for lavt komponenttall, høy effektivitet, lav harmonisk forvrengning og høyere effekttetthet. Videre gir fremskritt innen bipolare MPC-er muligheten til å balansere likestrømsbussen uten å kreve et komplekst kontrollsystem.

I denne avhandlingen ble det utviklet og verifisert fem nye MPC-topologier (T_A til T_E) av ikke-isolert (T_A, T_B og T_D) og isolert (T_C og T_E) konfigurasjon med unipolare (T_A til T_C) og bipolare utganger (T_D og T_E) for ulike anvendelser innen hybride energisystemer. Alle disse bidragene ble presentert i åtte publikasjoner (Artikkel I - VIII), inkludert tre tidsskrifter og fem konferanseartikler. Disse artiklene er oppført i kapittel 1, og detaljene om deres spesifikke bidrag blir fremhevet. Videre ble AC-nettintegrasjon gjennom integrering av noen av MPC-ene (T_A og T_D) med MLIs utforsket og validert. Integrering av bipolare MPC-er til bipolare DC-

transmisjons- / distribusjonsinfrastruktur med mulighet for å forsyne en kritisk unipolar DC-last ble også bekreftet. Den første ideen til T_A, en ny ikke-isolert MPC med unipolare utganger, ble presentert i artikkel I med mer detaljert analyse og eksperimentell validering i artikkel II. Artikkel III presenterer T_C, en isolert MPC-topologi med unipolare utganger, sammen med nøkkelresultater. Artikkel IV presenterer T_D, en ny familie av ikke-isolerte MPC-er med bipolare utganger, og nøkkelresultater, inkludert AC-nettintegrasjon ved bruk av en MLI, blir verifisert i denne artikkelen. I artikkel V ble en modifisert ensrettet versjon av T_A brukt for å oppnå integrasjon av unipolar likestrøm til vekselstrømnett, og bruken av en hjelpestrømskrets og en kontrollbasert tilnærming for å balansere likestrømslenken ble bekreftet. Artikkel VII presenterer T_B, en forbedring av T_A, som tillater kraftflyt mellom RES-porter og energilagringsporter. Den første ideen til T_E, en ny isolert MPC med bipolare utganger, ble presentert i artikkel VI med mer detaljert analyse, og de eksperimentelle valideringene ble implementert i artikkel VIII. Verifiseringen av integrering av T_E til en bipolær DC-distribusjonsinfrastruktur som forsyner en kritisk unipolar DC-last ble også presentert i artikkel VIII. Den stabile driftstilstanden til disse nye MPC-topologiene ble analysert matematisk og verifisert ved hjelp av detaljerte simuleringer og valideringer på en internt utviklet hardware-in-the-loop (HIL) plattform og på en eksperimentell testrigg, henholdsvis. Nyskapningen til de foreslåtte MPC-topologiene blir fremhevet gjennom detaljerte sammenlignende studier, og viktige mål som komponenttall, modularitet og spenningsgevinst blir understreket. Utviklingen av disse omformerne kan bidra betydelig til integreringen av RES-er og lagringssystemer i strømnettet og fremme bærekraftige energipraksiser. Denne avhandlingen har fem hovedkapitler: det første presenterer introduksjonen og bakgrunnen for MPC, det andre gir en gjennomgang av kunnskapsstatus, mens det tredje og fjerde presenterer de nye MPC-ene som er foreslått her, og hovedresultatene, henholdsvis. Avslutningsvis presenteres kapittel 5, som fremhever de viktigste funnene og begrensningene i denne doktorgradsstudien.

List of Publications

The following listed papers from latest to earliest are based on research activities conducted by the author within the framework of the PhD study and have been published or submitted for publications in peer-reviewed journals and conference proceedings.

I. **I. N. Jiya**, H. V. Khang, N. Kishor and R. Ciric, "Four Quadrant Switch Based Multiple-Input DC-DC Converter," in *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia)*, Singapore, Singapore, 2021, pp. 2199-2204, doi: 10.1109/ECCE-Asia49820.2021.9479432.

II. **I. N. Jiya,** A. M. S. Ali, H. V. Khang, N. Kishor and R. Ciric, "Novel Multisource DC-DC Converter for All-electric Hybrid Energy Systems," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 12934–12945, Dec. 2022, doi: 10.1109/TIE.2021.3131871.

III. **I. N. Jiya,** A. Salem, and H. V. Khang, "Novel Isolated Multiple-Input Buck-Boost DC-DC Converter for Renewable Energy Sources," *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Toronto, Canada, 2021, pp. 1-6, doi: 10.1109/IECON48115.2021.9589538.

IV. **I. N. Jiya,** H. V. Khang, N. Kishor, and R. M. Ciric, "Novel Family of High-Gain Nonisolated Multiport Converters With Bipolar Symmetric Outputs for DC Microgrids," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12151–12166, Oct. 2022, doi: 10.1109/TPEL.2022.3176688.

V. **I. N. Jiya,** H. V. Khang, A. Salem, N. Kishor and R. Ciric, "Integrated Multiport DC-DC and Multilevel Converters for Energy Sources," *2022 IEEE Industry Applications Annual Meeting*, Detroit, Michigan, 2022, pp. 1-7, doi: 10.1109/IAS54023.2022.9939764.

VI. **I. N. Jiya,** H. V. Khang, N. Kishor and R. Ciric, "Novel High Gain Multiport Isolated DC-DC Converter with Bipolar Symmetric Outputs," *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968834.

VII. **I. N. Jiya,** P. Gunawardena, H. V. Khang, N. Kishor and Y. Li, "Multiport DC-DC Converter for Integrating Energy Systems in All-Electric Vehicles," *2023 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International*

Transportation Electrification Conference (ESARS-ITEC), Venice, Italy, 2023, pp. 1-6, doi: 10.1109/ESARS-ITEC57127.2023.10114856.

VIII. **I. N. Jiya,** H. V. Khang, P. Gunawardena, N. Kishor and Y. Li, "Novel Isolated Multiport DC Converter with Natural Bipolar Symmetry for Renewable Energy Source Integration to DC Grids," in *IEEE Access*, (*Submitted*).

Other Works: The following papers were published during the time of the PhD project but are not included in the dissertation.

I. A. Salem, H. V. Khang, **I. N. Jiya** and K. G. Robbersmyr, "Hybrid Three-Phase Transformer-Based Multilevel Inverter With Reduced Component Count," in *IEEE Access*, vol. 10, pp. 47754-47763, 2022, doi: 10.1109/ACCESS.2022.3171849.

II. **I. N. Jiya,** Ahmed Salem, Huynh Van Khang, and Raimondas Pomarnacki, "Integrated Multiport DC-DC and Multilevel Converters for Multiple Renewable Energy Source Integration," in *IEEE Access*, (*Submitted*).

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List of Abbreviations and Symbols

AC	alternating current
BDC	bipolar dc-dc converter
BDCG	bipolar dc grid
CCM	continuous conduction mode
CMV	common-mode voltage
D	duty cycle
DAB	dual active bridge
DC	direct current
DCM	discontinuous conduction mode
D_{ieff}	effective duty of i
DMPPT	distributed maximum power point tracking
EMI	electromagnetic interference
ESR	equivalent series resistance
ESS	energy storage system
EV	electric vehicle
FB	full bridge
FBS	fully-controllable bidirectional switch
F_{SW}	switching frequency
GaN	gallium nitride
GVD	greinacher voltage doubler
HB	H-bridge
HIL	hardware-in-the-loop
HVDC	high voltage dc
IEA	international energy agency
IEEE	institute of electrical and electronics engineers
IGBT	insulated-gate bipolar transistor
i_L	inductor current
i_L	inductor current
i_o	output current
IPF	independent power flow
L_m	magnetizing inductance
MBDC	multiport non-isolated dc-dc converter with bipolar outputs
MIBDC	multiport isolated dc-dc converter with bipolar outputs
MIMO	multiple input multiple output

MISO	multiple input single output
MLI	multilevel inverter
MOSFET	metal–oxide–semiconductor field-effect transistor
MPC	multiport dc-dc converter
MPPT	maximum power point tracking
n	turns ratio
N_1	primary turns
N_2	secondary turns
$\emptyset$	phase shift
P&O	perturb and observe
PC	personal computer
P_{cap}	capacitor losses
PCS	pulsating current source
PI	proportional integral
P_{indC}	core losses
P_{indW}	winding losses
P_L	power losses
PMC	power management control
P_{onMOS}	MOSFET conduction losses
PS	phase shift
PV	photovoltaic
PVS	pulsating voltage source
PWM	pulse width modulation
RB	reverse blocking
R_{DSon}	on-state resistance
RES	renewable energy source
SBC	synchronous buck converter
SiC	silicon carbide
SISO	single input single output
SoC	state of charge
SPF	simultaneous power flow
T_A	topology A
T_B	topology B
T_C	topology C
T_D	topology D
T_E	topology E

THD	total harmonic distortion
t_{off}	off time
t_{on}	on time
T_S	switching period
UDCG	unipolar dc grid
VCS	variable carrier scheme
V_{dc}	dc link current
V_{dc}	dc link voltage
V_o	output voltage
$V_{o\text{-}ref}$	output voltage reference
V_{TR}	voltage transformation
ZCS	zero current switch
ZVS	zero voltage switch

Chapter 1

1 Introduction

1.1 Background

Despite the decreasing world population growth rate over the years, the human population on planet earth has continued to grow, reaching over eight (8) billion people so far [1]. This growing population coupled with a drastic increase in industrialisation on a massive scale, has brought about huge demands for energy. The international energy agency (IEA) projects a 25% increase in the global primary energy demand between the years 2017 and 2040. It is also predicted that if no further improvement occurs in energy efficiency, it could lead to a 50% increase in energy demands [2]. This rather radical increase in energy demand alongside the damaging effects of climate change and degradation of planet earth has resulted in an aggressive exploitation of non-renewable and pollutant sources of energy over the years. To combat the detrimental effects of man's long-standing pollution of the environment and attempt to attain a state of balance and environmental purity on planet earth, there has been a rise in the utilisation of renewable energy sources. Although the supply of energy from renewable energy sources (RESs) to the energy supply mix continues to grow to reach this state of balance and purity in the energy cycle, there needs to be a consistent increase in the efficiency of energy generation, supply, and utilisation. These needs define the drive of the power, energy, and electronics industry [3].

Due to the intermittent nature of many RESs, energy storage presents a huge opportunity in the advancement towards renewable or green energy solutions. To this end, hybridisation of energy sources and storages through power electronic converters, as illustrated in Figure 1.1, has been the theme of a lot of research [4]. Therefore, it is an effective and economic solution towards improving the performance of RESs. The application of hybridised energy systems cannot be overemphasized as they find relevance in a wide area of applications, ranging from dc micro grids, energy storage backup for communication systems to electric vehicles (EVs) of any kind. Especially, since all-electric hybrid energy systems have played a key role in microgrids [5] and zero-emission transportations, e.g in

ferry boats [6], EVs [7]. Hybridization in electric energy systems requires a simultaneous power flow of several electric energy sources, and bidirectional operations are strictly required in such systems equipped with energy storage. Further, distributed RE generation systems are the backbone of future power systems, which are mainly based on dc microgrids, since they have no issue with reactive power and synchronisation beside advantages like lower losses and less conductor material, as compared to the ac microgrids [8–10]. Three-wire dc bus grid systems, called bipolar dc grids (BDCG) are also fast gaining popularity since they have been recently implemented in telecommunication systems, EVs and marine vessel charging, data centres and high voltage dc (HVDC) transmission and distribution systems [11–13]. This fast adoption is due to the higher efficiency because to transmit the same power, the current is smaller in BDCGs than in unipolar dc grids (UDCGs). The reliability of BDCGs is also higher than that of UDCGs because when one of the poles fails, the other pole can continue to transmit power with reduced capacity. Further, BDCGs offer an easier and better-quality conversion from dc to ac voltage using multilevel inverters (MLIs), due to the three voltage levels ($\pm\frac{V_o}{2}$ and V_o) while UDCGs offer only one voltage level. With the increasing penetration of multiple RESs, which are intermittent in nature, power electronic converters have gained popularity for effective energy utilization [14]. Power electronic converters can be categorized based on their application in four main groups namely, dc-ac, ac-dc, ac-ac and dc-ac converters and can be either isolated or non-isolated based on the feature of magnetic isolation or lack thereof [15]. However, among the others, dc-dc converters (e.g. buck, boost, buck-boost and full-bridge converters etc.) have been widely used to convert the different voltage levels of several dc sources to a standard operating voltage in dc microgrids [16]. Further, with the attractive features of BDCGs and UDCGs, RESs and dc loads can be more easily integrated by dc-dc converters [17] as shown in Figure 1.1. However, many sources and loads have different voltage levels, requiring many single-input single-output (SISO) dc-dc converters to step-up or step-down the voltage to or from the dc bus. Consequently, bulky and complex configurations, as well as high component count and cost, amidst global semiconductor chip shortages are the major reluctances of using SISO dc-dc converters in energy source and storage hybridization systems [18, 19].

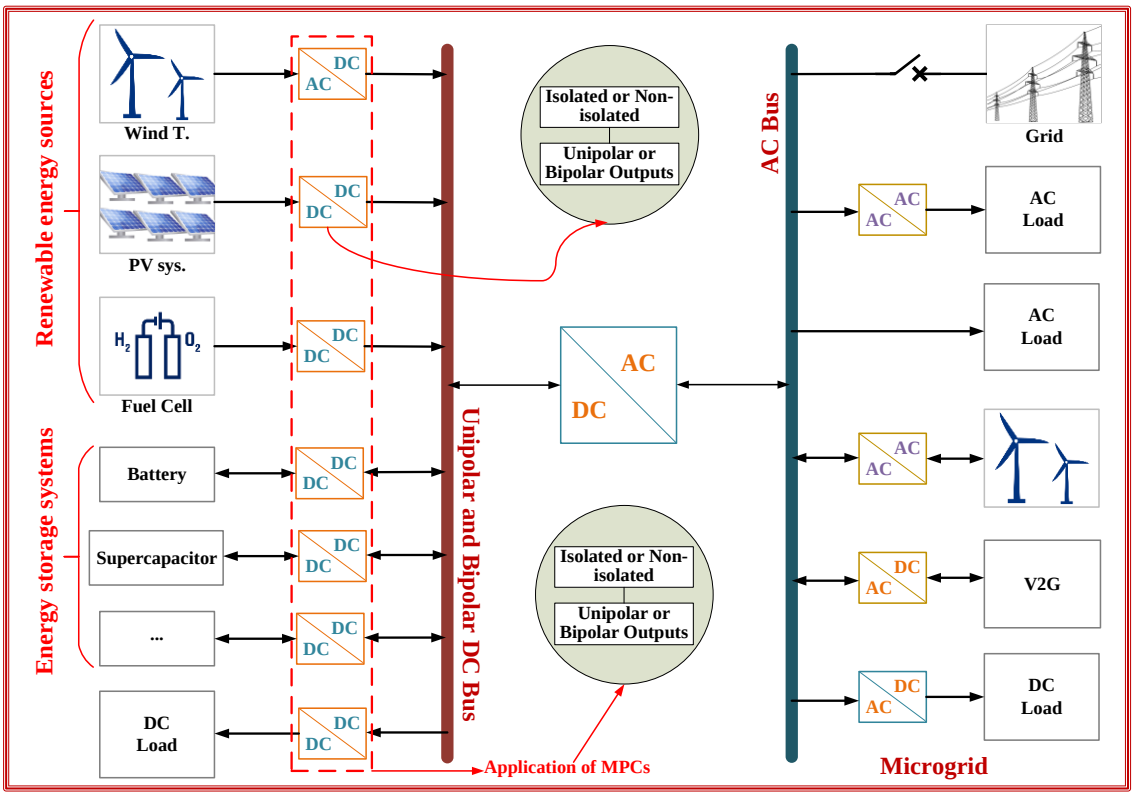


Figure 1. 1: Schematic overview of a hybrid energy system with multiple sources, storages and loads enabled by power electronic converters.

Multiport dc-dc converters (MPCs), which are generally derived from conventional SISO converters with a goal of sharing as much components as possible between the input ports of the MPCs [20, 21], have lately been offered as a solution to the mentioned problems in SISO dc-dc converters [22–25]. To this end, a lot of research has gone into proposing several MPCs isolated (with galvanic) and non-isolated (without galvanic) isolation. The isolated MPCs are based on magnetically connected circuits (through transformers or coupled inductors) while the non-isolated MPCs are based on electrically connected circuits [15]. Due to the magnetic separation of input and output given by the magnetic components, isolated MPCs have significant features of soft switching ability, high gain, and safety over non-isolated MPCs [22, 23]. Several isolated MPCs have been proposed, but their common limitation is the use of multiple windings for the inputs of the transformers or coupled inductors based on flux additivity [22, 23, 26–28]. This leads to reduced power density, increased size, and control complexity since the phase-shifted pulse width modulation (PS-PWM) control is required to achieve simultaneous power transfer from the input sources in certain cases. Further, since multiple windings are required at the primary side

of the magnetics for the input sources, and multiple clamping circuits will also be required, thus further increasing component count and potentially control complexity if any active clamping is to be applied. To mitigate these issues, isolated MPCs with only two windings, one primary and secondary each, have been proposed in [24, 25, 29, 30]. However, these MPCs also suffer from high component count with some requiring multiple inductors and capacitors at each input [29]. Bulky structure and complex control restrict the isolated MPCs from hybrid energy systems, which do not require an isolation feature. The non-isolated MPCs have features of reduced size, cost, and ease of miniaturization [31]. These features allow non-isolated MPCs to gain popularity over isolated counterparts in hybrid energy systems with extensive developments in recent years [32–42]. MPCs can also be either multi output or single output topologies. In [23, 24, 34, 35, 40, 42], MPCs with multiple-inputs and single-outputs (MISO) have been proposed for RES integration with features such as reduced component count and simplified control strategy, but they are all unsuitable for BDCG systems because they have only one output port. To overcome this, isolated and non-isolated MPCs with multiple inputs and outputs (MIMO) have been proposed in [43–46]. However, these MIMO MPCs must deal with cross-regulation of the voltage at the output ports, requiring complex controllers to suppress this problem. This problem birthed the need for bipolar dc-dc converters (BDCs), which typically have only two symmetrical outputs, one for each pole (positive and negative), respectively. To resolve this, multiport BDCs have been proposed recently in [47–50]. However, these multiport BDCs have some disadvantages such as: they cannot allow for an arbitrary independent power flow from either of the input sources to the bipolar dc bus, aside the requirement for complex control to achieve balanced symmetric output voltages, significant component count, limitation on number of inputs and low voltage gain. These disadvantages underline the demand for novel multiport BDCs to fill the need. Furthermore, compared to their unipolar counterparts, fewer MPCs with bipolar symmetric outputs have been proposed in literature.

Summarily, despite of the plethora of research in this field, there is still a gap to be filled in energy system hybridization and the implementation of MPCs with both unipolar and bipolar outputs for hybrid energy system applications. The opportunities to develop new MPCs using the latest technological developments in power electronics for application in grid integration are abundant.

1.2 Motivation and research problem

Opportunities for further developments in MPCs, which are largely classified based on the galvanic isolation (that is, the isolated and non-isolated topologies) with either unipolar or bipolar outputs, can be summarized around three key areas. Firstly, in component count, there is a need to further increase the number of components shared by the input ports of the MPCs. An increase in this metric reduces the overall component count and potentially increases the power density of the MPC and the efficiency of conversion as well as that of the converter. Secondly, the control of power sharing among the inputs to the respective MPC, especially during simultaneous power transfer from the inputs to the dc link has received less attention over the years. Lastly, there is more room to propose new MPCs, which have desirable performance and operational characteristics and still possess the attractive feature of high voltage gain. Particularly, in the isolated MPC topologies, the need to propose new MPCs, whose inputs can be arbitrarily increased, without modifications to the core of the magnetic component utilized in achieving galvanic isolation, is noteworthy. In the non-isolated counterparts, which are usually characterized by low voltage gain, there is need to explore the possibilities of increasing the voltage gain through novel MPC topologies, while also retaining the characteristic of low component count. Further, the MPCs with bipolar symmetric outputs have a longstanding challenge of maintaining the symmetry of the bipolar outputs under disturbances in the output voltage or/and loads. Thus, the need for implementation of less complex control strategies to maintain balanced bipolar output voltage or natural output voltage symmetry with low component count, cannot be overemphasized. These issues give rise to the need for this research.

1.3 Contributions of the dissertation

The scientific contributions of this dissertation are highlighted in this section and are based on three IEEE journal papers (two published and one under review) and five conference papers (four published and one accepted). Figure 1.2 presents an overview of how these contributions fit into the scope of MPCs. These contributions cover the isolated and non-isolated MPCs with and without bipolar outputs and their applications for grid integration.

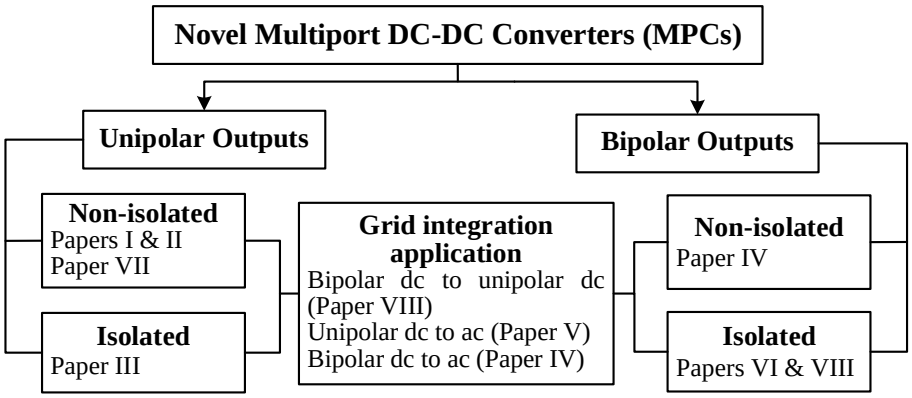


Figure 1. 2: Contributions of this dissertation based on the scope of MPCs.

Paper I: Four Quadrant Switch Based Multiple-Input DC-DC Converter

Summary: In this paper, a novel non-isolated multiport dc-dc converter (MPC) is proposed and analysed for two inputs. The MPC uses four-quadrant switches, only one inductor and capacitor. It is capable of bidirectional operation in non-inverting buck-boost configuration and can accommodate the simultaneous transfer of energy from more than one source of different voltage levels to the DC bus. As compared to existing MPCs of similar characteristics in literature, the proposed converter utilizes less number of inductors and requires only one switch to integrate any extra energy storage. Different operation modes of the proposed MPC are numerically verified and validated on a high-fidelity hardware-in-the-loop (HIL) device.

Contribution: A non-isolated MPC with unipolar outputs based on bidirectional switches with unique attributes and low part count is proposed. It is recommended for energy storage hybridisation applications where bidirectional power flow is required. Numerical simulations and HIL implementation were performed to verify the operation of the proposed MPC.

This paper has been published as:

I. N. Jiya, H. Van Khang, N. Kishor and R. Ciric, "Four Quadrant Switch Based Multiple-Input DC-DC Converter," in *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia)*, Singapore, Singapore, 2021, pp. 2199-2204, doi: 10.1109/ECCE-Asia49820.2021.9479432.

Paper II: Novel Multisource DC-DC Converter for All-Electric Hybrid Energy Systems

Summary: In paper II, the novel non-isolated MPC proposed in paper I is further verified with an application focus for all-electric hybrid energy storage systems. The proposed MPC is capable of bidirectional operation in non-inverting buck-boost configuration and can accommodate the simultaneous energy transfer from multiple sources of different voltage levels to the dc bus. As compared to counterparts, the proposed MPC utilizes a smaller number of inductors and requires only one bidirectional switch to integrate any extra energy storage. Within the framework, a novel voltage transformation, operation modes and control method are presented in detail. This is in addition to a detailed comparison of the proposed MPC with other existing MPCs with similar characteristics to highlight its unique superiority. The performance and key features of operation with varying voltage levels and duty cycles of the proposed MPC are numerically verified through a high-fidelity HIL platform and experimentally validated on an in-house test rig.

Contribution: Although the initial idea alongside preliminary results based on simulations of the MPC proposed in paper II was presented in paper I, the detailed analysis and features are further experimentally validated using an in-house SiC-switch based experimental test rig. Within this framework, a novel voltage transformation factor is proposed, and a single input single output (SISO) controller for parallel configuration with multiple voltages involved is introduced and verified on the high-fidelity HIL platform.

This paper has been published as:

I. N. Jiya, A. M. S. Ali, H. Van Khang, N. Kishor and R. Ciric, "Novel Multisource DC-DC Converter for All-electric Hybrid Energy Systems," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 12934–12945, Dec. 2022, doi: 10.1109/TIE.2021.3131871.

Paper III: Novel Isolated Multiple-Input Buck-Boost DC-DC Converter for Renewable Energy Sources

Summary: An isolated MPC with unidirectional buck-boost characteristics and simultaneous power transfer is proposed for multi-sources in renewable

energy systems in paper III. As compared to existing isolated MPCs with unipolar outputs, the proposed MPC significantly reduces the component count and control complexity since it requires a fixed coupled inductor with only one primary and secondary winding each for any number of inputs and does not require any phase-shifted pulse-width modulation. The operation of the proposed converter for simultaneous power transfer from multiple sources with varying voltages is numerically verified in simulation and validated on OPAL-RT's OP5700 HIL validation platform.

Contribution: An isolated MPC with unipolar outputs is proposed, based on reverse blocking switches with unique attributes of low part count and fixed primary and secondary windings. It is recommended for renewable energy source applications, where only unidirectional power flow is required. Numerical simulations and HIL implementation were performed to verify the operation of the MPC in paper III.

This paper has been published as:

I. N. Jiya, A. Salem, and H. Van Khang, "Novel Isolated Multiple-Input Buck-Boost DC-DC Converter for Renewable Energy Sources," *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Toronto, Canada, 2021, pp. 1-6, doi: 10.1109/IECON48115.2021.9589538.

Paper IV: Novel Family of High-Gain Nonisolated Multiport Converters With Bipolar Symmetric Outputs for DC Microgrids

Summary: Bipolar dc grid systems are fast gaining attraction for renewable energy source (RES) integration, because of their merits of higher reliability, efficiency and robustness as compared to the unipolar dc grids. However, the progress in multiport converters, resulting into lower cost and more compact design for bipolar microgrid systems, is slow. Therefore, paper IV proposes a novel family of five non-isolated multiport dc-dc converter topologies with bipolar symmetric outputs. The performance and key operational features of the proposed converters under varying input voltages, duty cycles and loads are numerically verified and experimentally on an in-house test setup to prove the concept of the proposed converters. In the experimental validation, the operation of the converter under

simultaneous and arbitrary individual power transfer from two input ports is tested. Further, the easy integration of the proposed converters with a multilevel inverter to achieve high-quality ac voltages is demonstrated. As compared to the few existing counterparts, the proposed converters have a competitive edge in terms of higher number of input ports and voltage gains. Alongside the possibility of arbitrary independent power flow from the input ports, inherently symmetrical outputs require a simple balance control for asymmetrical members of the family.

Contribution: In this paper, a novel family of five non-isolated MPCs with bipolar outputs (MBDCs) is proposed. These MBDCs possess novel features of high gain, simplified control, ability to arbitrarily increase the number of inputs and inherently symmetrical bipolar outputs or simple output voltage balancing control in the case of the asymmetrical topologies. Within this framework, the proposed novel family of MBDCs is analysed for two input sources of equal and unequal input voltage levels under simultaneous power transfer from both sources. The analysis is then numerically verified and experimentally validated using an in-house SiC-switch based experimental test rig. Finally, the integration of the proposed MBDCs with future dc-ac conversion systems was also demonstrated.

This paper has been published as:

I. N. Jiya, H. Van Khang, N. Kishor, and R. M. Ciric, "Novel Family of High-Gain Nonisolated Multiport Converters With Bipolar Symmetric Outputs for DC Microgrids," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12151–12166, Oct. 2022, doi: 10.1109/TPEL.2022.3176688.

Paper V: Integrated Multiport DC-DC and Multilevel Converters for Energy Sources

Summary: Paper V presents a novel converter system for integrating multiple renewable energy sources for both dc and ac grids. The proposed converter system is formed by integrating a modified unidirectional version of the novel MPC topology presented in papers I and II with a multilevel inverter topology. This was done to achieve multiple source integration with low component count and higher efficiency on the multiport converter section and efficient dc to ac conversion on the multilevel inverter section.

As compared to counterparts in literature, where each energy source requires its own dc converter and the dc to ac conversion is achieved using a two-level converter, the converter system proposed in this paper has more attractive features of buck-boost operation, better power quality characteristics and low part counts. Within the framework, an auxiliary circuit-based dc link voltage balancing technique is proposed to balance the voltage on the dc link as compared to the more complex control-based balancing scheme. Open and closed loop operations of the converter system are numerically verified using simulations and validated by a high-fidelity hardware-in-the-loop implementation platform.

Contribution: A converter system for integrating multiple energy sources and converting to ac with unique attributes of low part count, high gain and high-quality ac power is proposed. A comparison of two methods of balancing the dc link capacitor voltage is evaluated, and both were found to achieve desirable performance characteristics. This converter system is recommended for renewable energy source integrations applications, where conversion to ac is also required. The converter system was validated using numerical simulations and on the HIL validation platform.

This paper has been published as:

I. N. Jiya, H. Van Khang, A. Salem, N. Kishor and R. Ciric, "Integrated Multiport DC-DC and Multilevel Converters for Energy Sources," *2022 IEEE Industry Applications Annual Meeting*, Detroit, Michigan, 2022, pp. 1-7, doi: 10.1109/IAS54023.2022.9939764.

Paper VI: Novel High Gain Multiport Isolated DC-DC Converter with Bipolar Symmetric Outputs

Summary: In paper VI, an isolated multiport dc-dc converter with inherently symmetric bipolar outputs (MIBDC) is proposed. The suggested converter has a competitive advantage over its few counterparts in terms of the number of input ports, voltage gain, and natural symmetry of the outputs. Furthermore, because the proposed MIBDC uses a fixed transformer with only one primary and secondary winding for any number of inputs, it considerably decreases component count and control complexity. The proposed converter's operation is quantitatively tested in

simulation and on OPAL-RT's HIL validation platform for independent and simultaneous power transfer from multiple sources with varying voltages.

Contribution: An isolated MPC with bipolar outputs is proposed, based on the centre tapped transformer of a dual active and phase-shifted full-bridge converter. It has a unique attribute of inherently symmetrical bipolar outputs. As compared to counterparts, its number of inputs can be arbitrarily increased without any modifications to the core of the isolation transformer. It is recommended for energy source hybridisation applications where bidirectional power flow is not required. Numerical simulations and implementation on the HIL validation platform was performed to verify the operation of the proposed MPC.

This paper has been published as:

I. N. Jiya, H. Van Khang, N. Kishor and R. Ciric, "Novel High Gain Multiport Isolated DC-DC Converter with Bipolar Symmetric Outputs," *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968834.

Paper VII: Multiport DC-DC Converter for Integrating Energy Systems in All-Electric Vehicles

Summary: In this paper, a non-isolated multiport dc-dc converter (MPC) of non-inverting buck-boost configuration is proposed for integrating multiple energy resources in automotive applications. A typical example of such automotive application is an electric vehicle (EV), powered by one or more renewable energy sources (RESs) and consisting of one or more energy storage systems (ESSs), e.g. batteries and supercapacitors. The inputs to the MPC are clustered based on source or storage and integrated using uni- or bi-directional switches, respectively. It is capable of bi-directional operation between the storage cluster and the dc link, allowing for a simultaneous transfer of energy from more than one source of varying voltage levels (irrespective of its' cluster) to the dc link. The proposed MPC is analysed for four inputs, comprising of two per cluster in this paper. As compared to existing MPCs in literature, the proposed converter utilizes a fixed number (two) of inductors and is robust such that it requires only one

additional switch to integrate any extra energy storage or source in a respective cluster. Different operating modes of the proposed MPC are numerically verified and validated on OPAL-RT's OP5700 hardware-in-the-loop (HIL) platform.

Contribution: The non-isolated MPC with unipolar outputs proposed in paper VII is suggested as an improvement to the MPC in papers I and II. This is because the MPC in papers I and II can only accommodate energy storages while the MPC in paper VII can accommodate both storages and sources. Numerical simulations and HIL implementation were performed to verify the open and closed loop operation of this MPC.

This paper has been submitted as:
I. N. Jiya, P. Gunawardena, H. Van Khang, N. Kishor and Y. Li, "Multiport DC-DC Converter for Integrating Energy Systems in All-Electric Vehicles," *2023 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, Venice, Italy, 2023, pp. 1-6, doi: 10.1109/ESARS-ITEC57127.2023.10114856.

Paper VIII: Novel Isolated Multiport DC Converter with Natural Bipolar Symmetry for Renewable Energy Source Integration to DC Grids

Summary: In paper VIII, the novel isolated MPC with bipolar inherently symmetric outputs (MIBDC) proposed in paper VI is analysed. The suggested converter has a competitive advantage over its few counterparts in terms of the number of input ports, voltage gain, and natural symmetry of the outputs. Further, the proposed MIBDC uses a fixed transformer with only one primary and secondary winding for any number of inputs, it considerably decreases component count and control complexity. The converter requires a comparatively simple control structure, using only a single input single output (SISO) controller, such as the standard double loop PI controller. The proposed converter's operation is quantitatively tested in simulation and experimentally verified on OPAL-RT's OP5700 hardware-in-the-loop (HIL) platform for open and closed loop performance under varying conditions.

Contribution: By adopting a DAB-based and a FB-based topology with a fixed two winding (one primary and secondary winding each) transformer and many ports constructed using pulsating voltage sources, the MIBDC presented in paper VIII addresses the constraints of previous topologies. The component count is kept minimal, while the single inductor is time multiplexed to allow for any arbitrary independent and simultaneous power transfer from multiple sources. Further, a distributed MPPT (DMPPT) technique is proposed to reduce the complexity and thus requiring only one MPP controller for any number of inputs. The initial idea of the MIBDC proposed in this work has been presented in paper VI while the detailed analysis and features are numerically verified and results from experimental validation using the HIL test rig are presented in this paper.

This paper has been submitted as:
I. N. Jiya, H. Van Khang, P. Gunawardena, N. Kishor and Y. Li, "Novel Isolated Multiport DC Converter with Natural Bipolar Symmetry for Renewable Energy Source Integration to DC Grids," in *IEEE Transactions on Industrial Electronics*, (*Submitted*).

1.4 Dissertation structure

This dissertation consists of five chapters, numbered one to five, and is presented as follows:

Chapter 1: Introduction

In chapter one, a brief background and introduction to MPCs is provided alongside the motivation of the research. The main contributions of the dissertation are highlighted, and the structure of the dissertation is addressed.

Chapter 2: State-of-the-art

This chapter presents a literature review of the recently developed MPC topologies in terms of their structure, unique features, and drawbacks. The MPCs considered cover four broad MPC categories, that is, the isolated and non-isolated MPCs with unipolar outputs and, the isolated and non-isolated MPCs with bipolar outputs. This is done with the aim of highlighting the gaps in the existing MPC topologies,

which usher in the novel MPCs proposed in this dissertation to fill these gaps as presented in chapter 3.

Chapter 3: Novel multiport converter topologies

Chapter 3 presents the circuit configurations of the novel MPCs in this dissertation. Their steady state operating characteristics and control strategies are analyzed, and some grid integration applications were also presented.

Chapter 4: Results and discussions

A summary of the results and findings is presented in chapter five, based on papers I-VIII, in which the operation and performance characteristics of the novel MPCs are numerically verified and experimentally validated through in-house laboratory test rigs. Furthermore, their novel features are emphasized by comparative analysis with existing MPCs of similar structure and characteristics.

Chapter 5: Concluding remarks

The conclusions drawn based on the work carried out in the research are presented in chapter five. Further, the limitations and future room improvements are also highlighted.

Chapter 2

2 State of the art

In this chapter, some interesting MPC topologies developed recently are reviewed to highlight their characteristics, salient features, and limitations. The reviewed MPC topologies cover the topologies that address hybridization of multiple energy sources and/or storages. Specifically, the isolated and non-isolated MPCs with unipolar and bipolar outputs are addressed in this chapter.

MPCs are generally synthesized broadly based on two strategies [51–57]. One is the derivation from cognate MPCs through graph-based generalization and duality [20, 58, 59]. The second strategy is by the modification of the conventional SISO converters (such as the traditional buck, boost and buck-boost converters to name a few), using pulsating voltage and current sources to introduce multiple inputs to the traditional SISO converters [60–63]. Several different types of MPCs exist based on their classification, application, and some other performance characteristics [51, 53, 54, 57]. The different types of MPCs include single input MPCs with multiple outputs which may be unipolar or bipolar [64–69] and multiple input MPCs with single [23, 24, 34, 35, 40, 42] or multiple [43–46] outputs, which may be unipolar or bipolar [47–50] as well. The MPCs could also be isolated or non-isolated [15], that is regarding the galvanic separation between the inputs and outputs. As their designation suggests, single input MPCs have only one input port, so they cannot be applied in multiple energy source or storage hybridization. On the other hand, MPCs with multiple inputs can be used to integrate multiple energy resources to one or more dc buses depending on the number of outputs, thereby eliminating the need for many SISO converters for the same function. Therefore, the review in this chapter focuses only on the relevant isolated and non-isolated MPCs developed recently with multiple inputs and single unipolar outputs or multiple outputs which are bipolar. Firstly, the non-isolated MPCs with unipolar outputs are reviewed, next the isolated MPCs with unipolar outputs, the non-isolated MPCs with bipolar outputs and the isolated MPCs with bipolar outputs, respectively from Sections 2.1 to 2.4. This consideration covers the base on the different MPCs, applicable for energy system hybridization, which is the focus area of the research in this dissertation.

2.1 Non-isolated MPCs with unipolar outputs

Figures 2.1 to 2.5 presents some of the recently developed non-isolated MPCs with a unipolar output, that can be used for energy system integration into a dc link as presented in [32, 36–39]. The number of shared components in the MPCs is highlighted in blue to underscore the redundancy in these MPCs and underline the effectiveness of component count savings in these topologies.

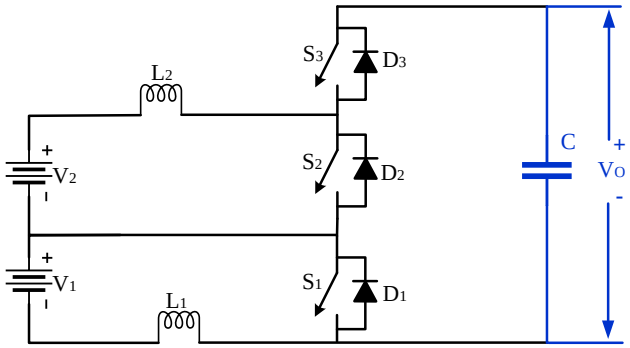


Figure 2. 1: Developed non-isolated MPCs with unipolar outputs proposed in [32].

The MPC in Figure 2.1 [32], presents a structure derived from the cascade of a traditional double-boost converter. For two inputs to this MPC, two inductors are required: one for each input, three controllable and uncontrollable switches and one shared dc link capacitor to filter out the output voltage. This MPC is capable of bidirectional operation, hence can be used for energy storage hybridization. However, the MPC can only boost the inputs, so the voltage of the energy storage devices at the input must always be lower than the dc link. Further, the MPC is incapable of arbitrary independent power flow from the input ports, thus it can only operate in simultaneous power flow mode to the dc link, which reduces the flexibility of the storage devices used in this MPC.

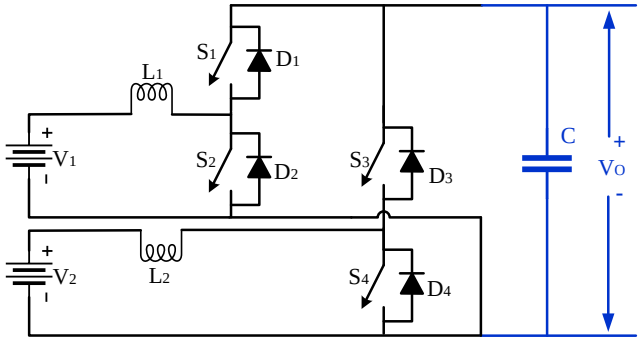


Figure 2. 2: Developed non-isolated MPCs with unipolar outputs proposed in [36].

The MPC in Figure 2.2 proposed in [36] is very similar to the MPC in [32], which is also derived from the double boost converter structure. For two inputs to the MPC, it also requires two inductors, one for each input port, and the dc link capacitor is also shared by all the inputs. However, in this case, each input port requires one half-bridge switch with two controllable and uncontrollable switches. The MPC in Figure 2.2 is also bidirectional and can only deliver supply the dc link in boost mode and so the storage devices need to always have a lower voltage than the dc link. Additionally, in this MPC, arbitrary independent and simultaneous power flow can be achieved since each input port has its own half-bridge switch.

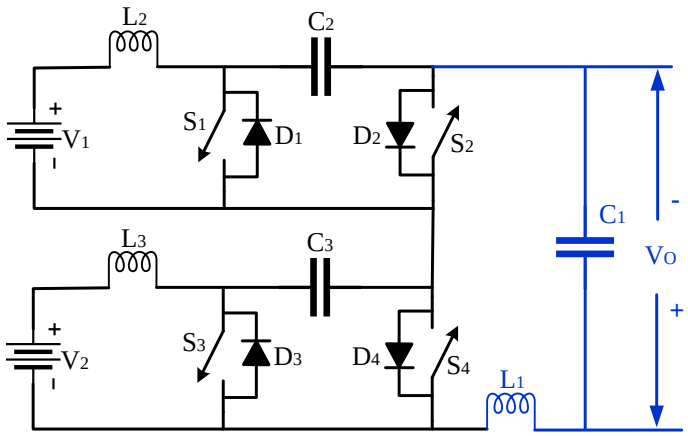


Figure 2. 3: Developed non-isolated MPCs with unipolar outputs proposed in [39].

In Figure 2.3, an MPC derived from the Ćuk converter is proposed in [39]. It is constructed by each input having its own pulsating voltage cell, which consists of an inductor, capacitor and two controllable and uncontrollable switches, while the inputs all share the filter components. This MPC is basically a cascade connection of the traditional Ćuk converter with the output inductor and capacitor shared among the inputs. One key limitation of this MPC is that, for its ideal operation, the energy storage devices at the input must be identical and have similar voltage levels for simultaneous power flow to be achieved. Further, the output voltage is inverted, and so an additional circuitry is required to achieve non-inverted outputs. Figure 2.4, a cascaded connection of the H-bridge synchronous buck-boost converter structure is used to synthesize the MPC as proposed by the authors in [38]. Each of the input ports to the MPC has an inductor and a half-bridge switch, consisting of two controllable and uncontrollable switches while they all share the same half-bridge switch and the dc link capacitor at the output. Being capable of simultaneous and independent power flow arbitrarily, the MPC can also buck and

boost the input voltages, thus there is no restriction on the voltage of the storage devices at the input in relation to the dc link. Furthermore, the MPC can also allow power flow between the input ports such that one energy storage device can charge the other.

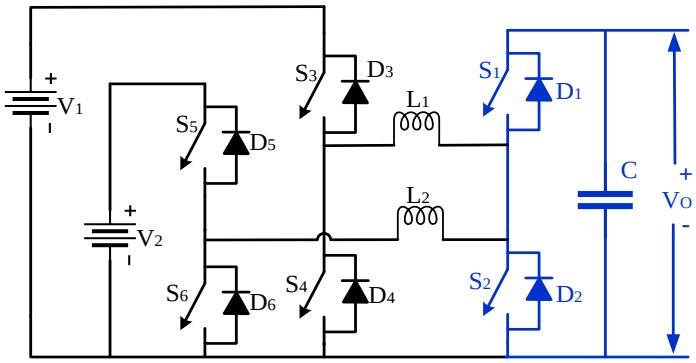


Figure 2. 4: Developed non-isolated MPCs with unipolar outputs proposed in [38].

The MPC in Figure 2.5 proposed in [37] is similar in structure, operation, and construction to the MPC in Figure 2.4 proposed in [38]. It also has a half-bridge at each input, but the input half-bridge has only one controllable switch. While it can buck or boost the input voltages to the dc link, the dc link can only charge the storage devices in buck mode of operation, restricting the voltage level on the input ports in relation to the dc link. Further, arbitrary independent and simultaneous power flow from the inputs to the dc link can be achieved, but power flow between the input ports cannot be achieved since only one controllable switch exists in the input half-bridges.

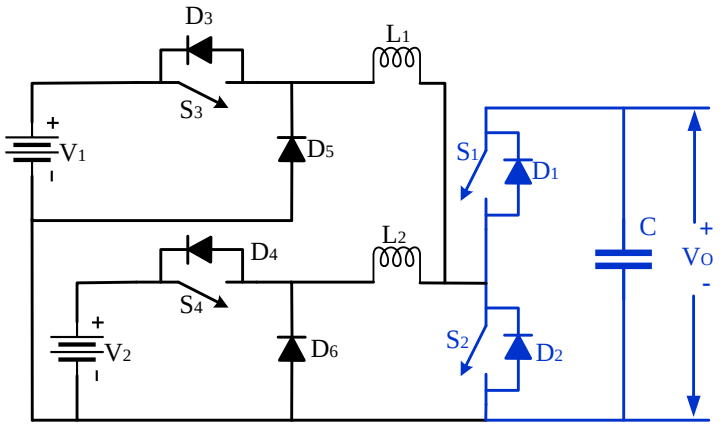


Figure 2. 5: Developed non-isolated MPCs with unipolar outputs proposed in [37].

Summarily, the features of reduced size, cost, and ease of miniaturization [31], allow non-isolated MPCs to gain popularity in energy systems with extensive developments in recent years. However, the non-isolated MPC in [32] is not

capable of independent power flow from the input ports with simultaneous power flow, being possible in boost mode only. While the MPCs in [36, 38, 39] are bidirectional buck-boost topologies, but every additional input port to the converters requires an additional inverter leg and an inductor, increasing the board footprint and cost. The MPCs in [36, 39] using a high component count can operate in buck/boost modes, but they do not allow for a simultaneous power transfer from the input ports, or power transfer between ports. The MPCs in [32, 37] require lower component counts as compared to [36, 39], but the power from the input ports can be simultaneously transferred only in the boost mode. These inadequacies in the existing non-isolated MPCs with unipolar outputs highlight the need to develop and validate novel MPC topologies, which feature much better component count reduction, while being robust enough to allow for simultaneous power transfer and power flow between the input ports.

2.2 Isolated MPCs with unipolar outputs

Figures 2.6 to 2.9 present some of the recently developed isolated MPCs with unipolar outputs. Again, to underscore the shared components in these MPCs, the components, that are shared by all the input ports, are highlighted in blue. These isolated MPCs mostly use a transformer or coupled inductor to achieve galvanic isolation between the input and output ports of the MPCs.

The MPC in Figure 2.6 proposed in [70] is a multi-active bridge MPC, having multiple active and passive full bridges at the primary and secondary sides respectively. This MPC is derived based on the dual active bridge (DAB) converter and the principle for generating the input ports is on the basis of pulsating current sources (PCS). A multi-quadrant transformer is used to achieve isolation. This isolated unipolar MPC is unidirectional and so can only be used to interface energy sources such as wind and solar PV systems. The downside of this MPC is quite obvious as the component count is huge, and the number of input ports cannot be arbitrarily increased without having to modify the isolation transformer. This is ignoring the losses that will arise due to the multiple passive bridge at the output port.

To improve upon the issue of component count with multiple active and passive bridges at the primary and secondary outputs of the unipolar isolated MPC in [70], the MPC proposed in [23] and presented in Figure 2.7, addresses this, by keeping the secondary sides passive full-bridge fixed at just one full-bridge while also eliminating the inductors at the input ports, thus making the input ports to become

PVSs. This drastically reduces the component count and potentially increases the efficiency of the MPC. Also, the number of shared components is improved to achieve less redundancy in the component utilization. However, one key limitation remains, requiring multiple active bridges at the input ports, or one for every additional input. Further, the number of input ports cannot be arbitrarily increased without modifications to the core of the isolation transformer.

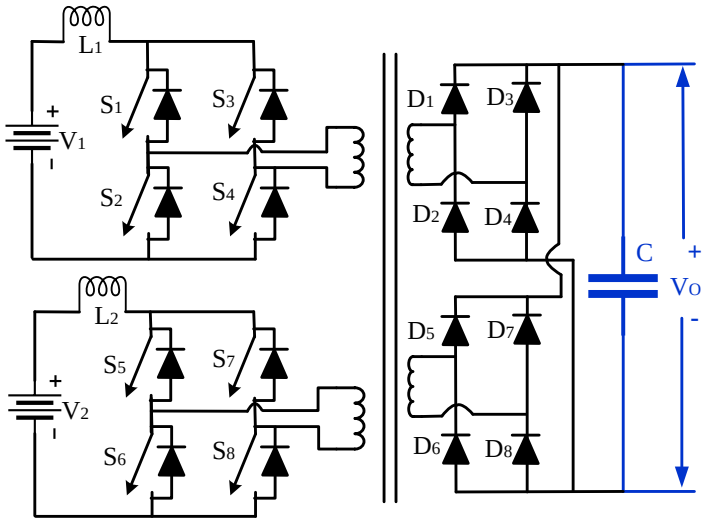


Figure 2. 6: Developed isolated MPCs with unipolar outputs as proposed in [70].

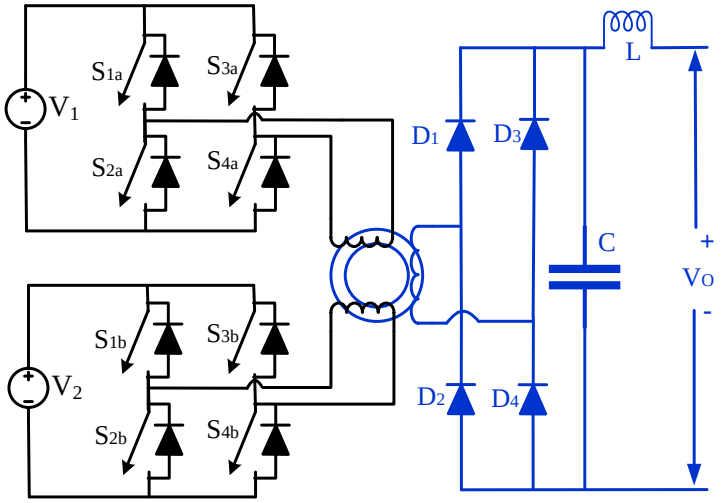


Figure 2. 7: Developed isolated MPCs with unipolar outputs as proposed in [23].

Figure 2.8 presents an isolated MPC proposed in [24], to address two key limitations of the MPCs in [23, 70], which are the lack of bidirectional operation and the lack of possible expansion of the MPCs' inputs without modification to the isolation transformer. To accomplish this, the MPC in [24] uses the traditional DAB converter to achieve the isolation and unipolar output. Meanwhile, the multiple inputs are introduced with each input port, having its own half-bridge

switch consisting of two controllable and uncontrollable switches. These inputs are like the PVSs of their non-isolated counterparts in [36–38], thus having a hugely reduced component count and increased robustness as well as operational characteristics. Although the number of components is reduced as compared to previously proposed MPCs in [23, 70], the component count is still quite significant and the MPC can only boost the input voltages, so it has a natural limitation on the voltage level of the inputs in relation to the output voltage.

To address the aforementioned drawbacks, the MPC proposed in [29] as presented in Figure 2.9, achieves a massive reduction in component count by adopting a modification of the traditional flyback converter. Using coupled inductors, also known as the flyback transformers, to achieve galvanic isolation, each input is paired with an inductor and a reverse blocking switch configuration (that is, a controllable and uncontrollable switch connected in series), thus yielding a PCS for each input port. This is markedly an improvement in the component count and potentially increased efficiency as compared to the MPC in [24], but the MPC in [29] has two limitations, one is that it is a unidirectional MPC and so cannot be used in energy storage application. The other limitation is that it is plagued by the power limit on the traditional flyback converter.

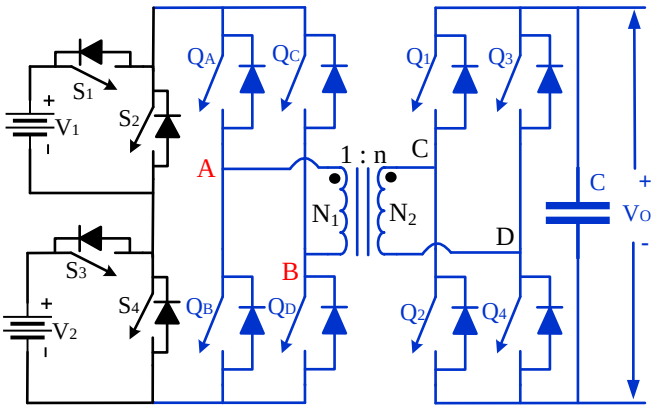


Figure 2. 8: Developed isolated MPCs with unipolar outputs as proposed in [24].

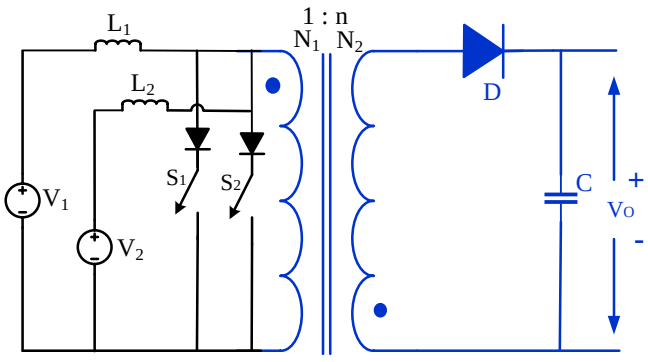


Figure 2. 9: Developed isolated MPCs with unipolar outputs as proposed in [29].

Summarily, the MPCs proposed in [23, 28] have a fixed number of input sources as well as complex control strategy, requiring phase shifted pulse width modulation (PS-PWM). Further, the MPC in [70] can only operate in boost mode. The component count of the MPCs in [24, 29] is lower than that of [23, 28]. Having no restriction on the number of input ports, they both require a fixed magnetic component for any number of input ports but the control strategy in [24] is PS-PWM. Hence, it is important to develop isolated MPCs with a unipolar output, which combine the advantages of [24, 29], by using a fixed magnetic component for galvanic isolation, with no limitations on the number of input ports, while further reducing the number of components with a simplified control strategy.

2.3 Non-isolated MPC with bipolar outputs

Figure 2.10 presents the only MPCs in literature, which both have multiple inputs and bipolar outputs as proposed in [47, 48]. The two MPCs were proposed for the integration of one energy source and storage device each with no possibility to arbitrarily increase the number of input ports.

The MPC proposed in [48] as presented in Figure 2.10 (a) uses two active switches and six passive switches alongside one inductor and two capacitors (one for each pole of the dc bus). It is a unidirectional buck MPC proposed for integrating a supercapacitor stack with a solar PV module for peak power shaving. Its unidirectional characteristic is huge downside since there is no way to recharge the energy storage port. Although the component count is significantly less than that of the MPC in [47], the bipolar output voltage is naturally asymmetrical under unbalanced load and so a complex closed loop control strategy is required to maintain the symmetry.

To improve upon the lack of bidirectional operation of the MPC in [48], the non-isolated MPC in [47] is proposed as presented in Figure 2.10 (b). The bipolar dc bus of this MPC is achieved through the cascade connection of two soft switched Greinacher voltage doublers (consisting of four capacitors, two inductors and two diodes). Using this approach, the bipolar dc bus can maintain natural symmetry under unbalanced loads without the need for any complex controller. Further, in this MPC, the energy storage port is controlled using a controllable switch and so the storage device can be recharged, although arbitrary single input mode of operation is still a limitation.

In summary, to our knowledge, the non-isolated MBDCs in [47, 48] are the most promising solutions for non-isolated MPCs with bipolar outputs so far in literature.

However, they are restricted to have two inputs, and cannot be extended for an arbitrary number of inputs, which is a key feature of MPCs. Additionally, they both cannot allow for an arbitrary independent power flow from either of the input sources to the bipolar dc bus, aside the low voltage gain feature and the requirement for complex control to achieve balanced symmetric output voltages in [48], and using high component count in [47]. Further, fewer MPCs with bipolar symmetric outputs exist for dc microgrids or integrating RES in literature as compared to the unipolar counterparts. Thus, it is necessary to develop and validate non-isolated MPCs with bipolar outputs which feature high voltage gain, low control complexity and modularity such that the number of input ports can be arbitrarily increased cannot be overemphasized.

2.4 Isolated MPC with bipolar outputs

To solve some of the issues plaguing non-isolated MPCs with bipolar outputs as discussed earlier, Figure 2.4 presents the few attempts at proposing isolated MPCs with bipolar outputs. Just like in the case of the non-isolated bipolar MPCs, far fewer isolated bipolar MPCs have been proposed as compared to their unipolar counterparts.

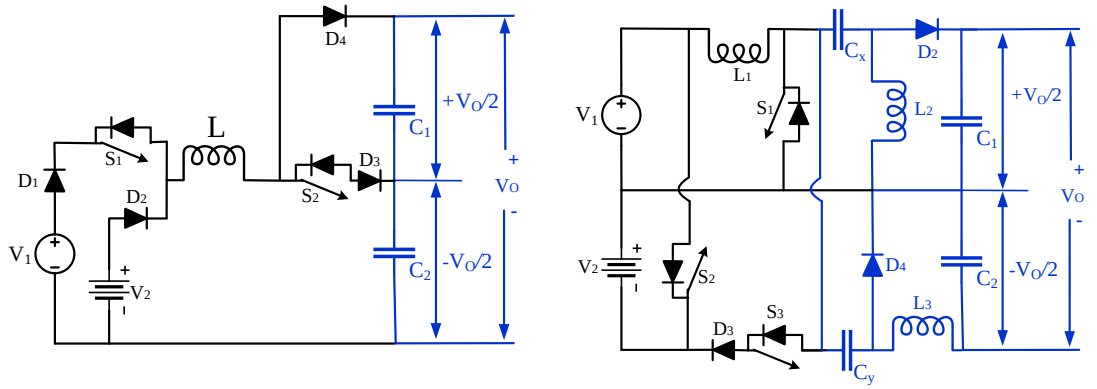


Figure 2. 10: Recently proposed non-isolated MPCs with bipolar outputs in (a) [48], and (b) [47].

The isolated bipolar MPC in Figure 2.11 (a) was synthesized based on the SISO DAB converter. It has the active full bridge at the primary side of the center tapped isolation transformer and a passive full bridge at the secondary side. It also has two extra diodes and an active half-bridge for maintaining the symmetry at the poles of the bipolar dc bus under unbalanced loads. Under this configuration, the MPC can achieve a a higher gain than the non-isolated counterparts, this is in addition to the increased safety margin due to the isolation transformer. However, it is still

plagued with the limitation on the number of inputs, as well as the lack of arbitrary single input mode of operation. Therefore, this MPC can only operate in simultaneous mode of power transfer from the inputs to the dc link. Further, the MPC cannot achieve bidirectional operation and so it is impossible to recharge the energy storage devices.

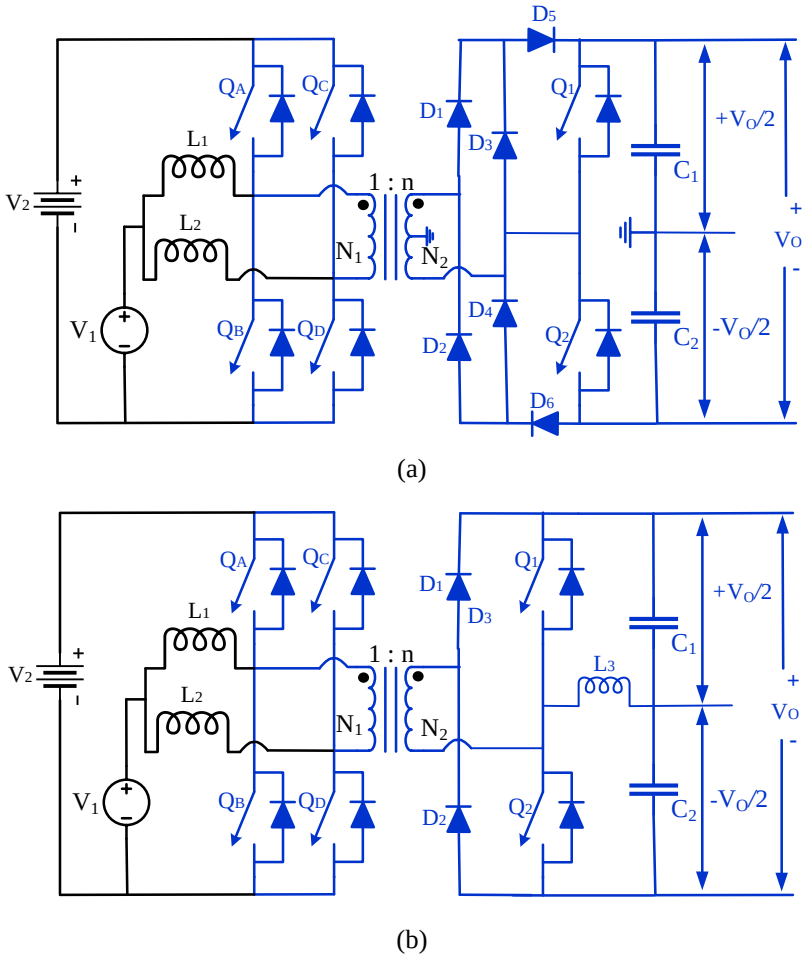


Figure 2. 11: Recently proposed isolated MPCs with bipolar outputs in (a) [49], and (b) [50].

To further reduce the component count of the bipolar isolated MPC in Figure 2.11 (a), the MPC in [50] as presented in Figure 2.11 (b) was proposed. It is also based on the conventional SISO DAB converter, but in this case, the isolation transformer is not center tapped. Further, the switch count is reduced by introducing a synchronous buck converter to maintain the symmetry of the bipolar output voltage under unbalanced loads. Although an additional inductor is introduced at the output, the MPC in Figure 2.11 (b) has four diodes fewer and a smaller core requirement than the MPC in Figure 2.11 (a). This could potentially result in increased efficiency but the key limitation of the number of input ports remains. Furthermore, it also can only operate in simultaneous power flow mode,

hence it is inflexible and lacks bidirectional capability, so the energy storage device cannot be recharged.

In a nutshell, the non-isolated bipolar MPCs in [47, 48] have low gain, power density, and only two inputs to the MPCs, thus they can't be expanded to have an arbitrary number of inputs, being one of the key features of MPCs. Further, they pose a safety issue due to the lack of magnetic isolation. Although the isolated bipolar MPCs in [49, 50] are the only proposed isolated bipolar MPCs in literature so far, featuring soft switching in some cases just like the non-isolated counterparts in [47, 48]. However, they both cannot allow for an arbitrary independent power flow from any of the input ports to the bipolar dc bus. This is aside the requirement for complex control to maintain symmetric output voltages under unbalanced loads, the limitation on the number of inputs and the low voltage gain. Therefore, novel isolated bipolar MPCs are required to tackle some of these disadvantages. Also, as compared to their unipolar counterparts, far fewer isolated MPCs with bipolar naturally symmetric outputs have been proposed in literature.

2.5 Grid integration applications

The increased penetration of RESs has led to a paradigm shift in the electrical energy generation and utilization from centralised to distributed generation systems [71]. Distributed generation systems are hence the backbone of future power systems, which are majorly based on dc microgrids, since they have no issues with reactive power and synchronisation among many other advantages as compared to the ac microgrids [9, 10]. However, in many conventional power systems, there is a high prevalence of ac power systems [72]. Thus, the need to convert the power generated from RESs from dc to ac cannot be overstated. Conventionally, the two-level inverter is implemented for converting dc to ac harvesting energy from RESs, but they have several limitations such as, high switching losses and total harmonic distortion (THD), requiring large filter components, to name just a few drawbacks [73].

MLIs have become one of the most attractive solutions for converting dc to ac at high power levels [74] due to their appealing features such as: low switching losses, small/zero common-mode voltage (CMV), low THD, lower electromagnetic interference, smaller filter component sizes and lower cooling requirements to name just a few [75]. Having all these merits over the traditional two-level inverter has been the motivation for the development of new MLI topologies. Although a lot of work has been done in proposing novel topologies of

MLIs [76–78], one aspect that has received significantly less attention is the conditioning of the input sources to accommodate the integration of RESs. Most existing topologies assume the inputs to be constant dc sources. This is ideal but is impractical in applications because most RESs vary in output voltage during operation [79].

To address this issue, some attempts have been made to propose MLIs, which have a provision to preprocess the outputs of RESs prior to the ac conversion stage [80–84]. In the MLI topologies proposed in [80–83], the preprocessing of the power from the RESs is integrated into the MLI topology in a manner that provides boosting features to the ac output. However, these topologies have two limitations. Firstly, the number of RESs, that can be integrated into the ac grid, is restricted to only one. Secondly, they are only capable of boosting the input voltages. To address this, the MLI proposed in [84] integrates two RESs using two cascaded dc-dc converters prior to the MLI stage, which allows for buck-boost operation and multiple inputs. However, with this structure, each RESs requires its own dc converter, leading to high component count, high power losses, higher system cost, lower power density and efficiency. Further, with the introduction of multiple RESs, there is the issue of dc link capacitor voltage balancing. MLIs used for multiple RESs require three dc link capacitors connected in series to equally split the dc link voltage across them [79]. Therefore, there is need to adequately balance the voltage across them to avoid distortions in the output waveforms and preserve the power quality. This usually requires a complex control system to achieve equally balanced dc link voltage across the three capacitors [85]. This creates a unique opportunity to fill the gap by applying MPCs in the integration of RESs to ac grid through MLIs, to achieve attractive features of low component count, high efficiency, low THD and higher power density. Further, the advances in bipolar MPCs comes with the yet unexplored chance to adequately balance the dc bus without requiring a complex control system for balancing dc link capacitor voltage.

Chapter 3

3 Novel multiport converters

In this chapter, the new multiport dc-dc converters (MPCs) proposed in this dissertation are presented. The circuit configuration and steady state analysis of the five novel MPCs based on papers I to VIII are presented in sections 3.1 to 3.5 respectively. Figure 3.1 presents a map of how the new MPCs labelled topology A (T_A) to topology E (T_E) fit into the different types of MPCs. Further, Section 3.6 presents the grid integration for some of the proposed MPC topologies, and finally Section 3.7 presents the analysis of their voltage gains.

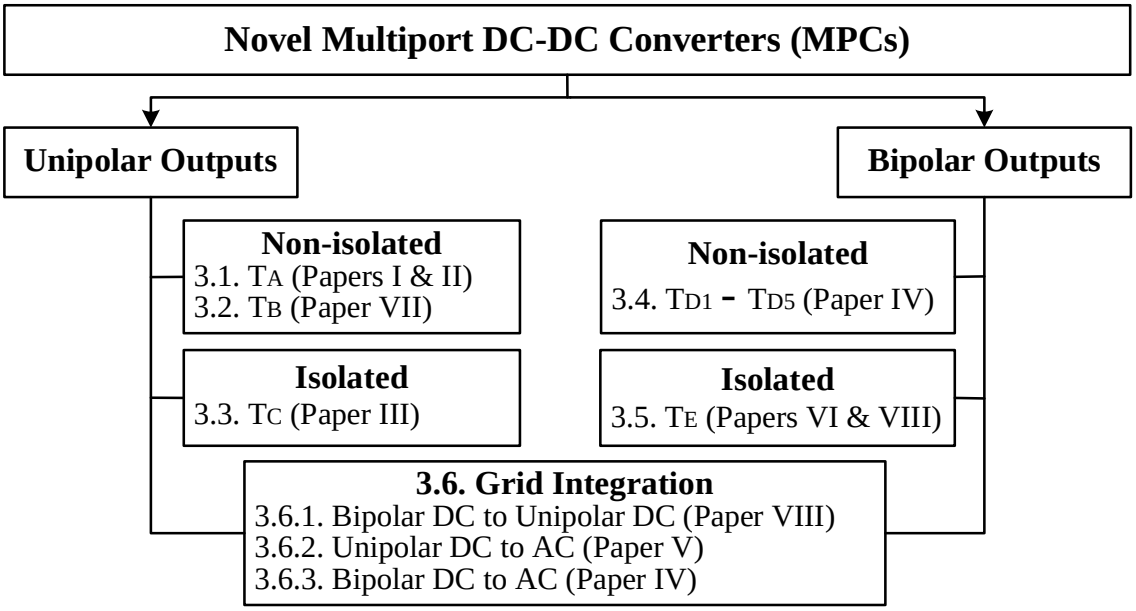


Figure 3. 1: Layout of the new MPC topologies proposed in this dissertation.

3.1 Proposed MPC topology A (T_A)

3.1.1 Circuit description

The circuit configuration of MPC T_A is presented in Figure 3.2, which consists of one inductor, one capacitor and four-quadrant switches. Four-quadrant switches, also known as fully-controllable bidirectional switches (FBSs), or matrix switches in some cases, are power electronic switches that can control ON-state current and OFF-state voltage bidirectionally. Figure 3.3 presents different implementations of

FBSs, including two gates, directing the flow of current through the switch. To achieve the ideal switching afforded by FBSs, two unidirectional switches (MOSFET or IGBTs with their respective anti-parallel diodes) are connected in anti-series configuration. In Figures 3.3 (a) and (b), the SiC-MOSFETs are connected in common source and drain configuration, respectively. Another interesting approach to achieve monolithic FBSs is illustrated in Figure 3.3 (c), in which two reverse blocking switches (RBSs), mostly IGBTs (RB-IGBTs) are connected in anti-parallel, thereby eliminating the two anti-parallel diodes as required in Figures 3.3 (a) and (b). This could result in lowering the losses, increasing efficiency and reducing switch cost [86], but IGBTs can only be applied for low switching frequency (<20 kHz), increasing the filter requirement in the MPC [87]. Yet, this configuration has received an attention as discussed in [88–90], achieving reverse blocking high electron mobility transistors (HEMTs), allowing for high frequency switching at high power applications. This progress leads to new possibilities for monolithic FBSs from GaN HEMTs as in [91]. The FBSs in T_A allows for a bidirectional power flow between the DC bus and energy storage systems. This converter is capable of bucking and boosting the input voltage in all operation modes. Further, it requires only one additional FBS when another input port is introduced to the MPC.

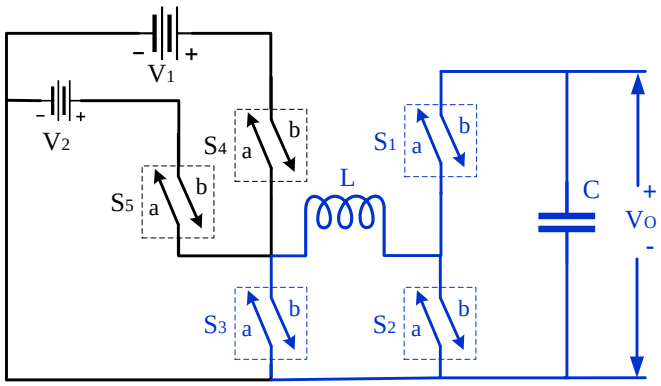


Figure 3. 2: The proposed MPC topology A.

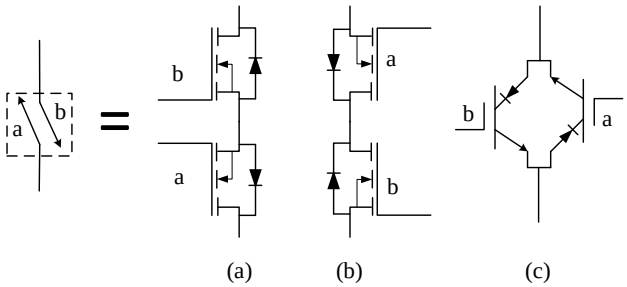


Figure 3. 3: Four-quadrant switch using (a) common source (b) common drain and (c) reverse blocking IGBTs in antiparallel configuration.

3.1.2 Steady state analysis

The T_A can operate in five modes when using two input sources. The first four modes (A-D) represent the interaction between the DC bus and two energy storage devices exclusively, e.g. from V_1 or V_2 to the DC bus, and vice- versa, respectively. Mode E will be elaborated later, representing the situation, in which both energy storages V_1 and V_2 supply the DC bus simultaneously. Figure 3.4 presents steady-state waveforms in the associated continuous conduction mode (CCM) for modes A to D. The switching period T_S is divided into two, T_1 and T_2, for the inductor charging and discharging period, respectively, in all four modes of operation.

In mode A of T_A, only V_1 is supplying the DC bus, thus the inductor L is charged during time T_1 by switching ON S_{4b} and S_{2b}. During T_1, the voltage V_L becomes V_1 while the inductor current i_L increases with a gradient of V_1/L. After time T_1 has elapsed, T_2 follows immediately. During this period, L discharges through C to the DC bus by switching ON S_{1a} and S_{3a}. During this time, V_L becomes $-V_o$ (the output voltage) and i_L decreases with a gradient of V_O/L. Similarly, when the converter operates in the opposite direction, by sending energy from the DC bus to V_1 in mode C, L is charged by switching ON S_{1b} and S_{3b} during T_1, while it discharges during T_2 by switching ON S_{4a} and S_{2a}. V_L is V_o and (V_1-V_o) during T_1 and T_2, respectively, while i_L increases with a gradient of V_O/L during T_1 and decreases with a gradient of $(V_1-V_o)/L$ during T_2. The interaction between V_2 and the DC bus in mode B and D is as earlier described for modes A and C, respectively. S_1 to S_3 do not need to block the reverse current as required in S_4 to S_N. The demerit of using only a MOSFET with its freewheeling diode in a synchronous configuration for S_1 to S_3, as listed in [92], makes FBSs very attractive.

The voltage balance analysis on the steady state waveform in Figure 3.4 proves that the proposed converter can operate in the buck and boost modes, depending on the duty ratio D, where D is T_1/T_S or the ratio of the inductor charging time to the total switching period. Therefore, the conventional equation (3.1) describing the relationship between the input V_{in} and output voltage V_{out} of the basic buck-boost converter applies to this converter for modes A to D.

$$V_{out} = \left[T_1/T_2\right]V_{in} = \left[D/(1-D)\right]V_{in} \tag{3.1}$$

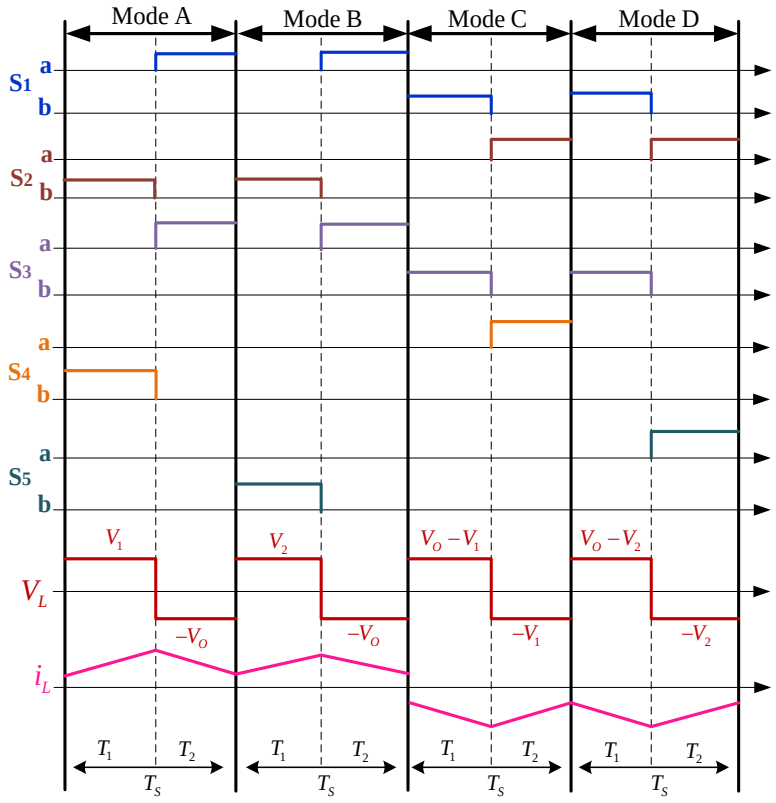


Figure 3. 4: Steady-state waveforms of operation in CCM for modes A to D.

The simultaneous mode of operation was earlier referred to as mode E, in which both V_1 and V_2 supply to the DC bus as illustrated in Figure 3.5. This mode is necessary when the required power of the DC bus cannot be satisfied by only a single energy storage. Two or more energy storages then must supply the energy simultaneously. Figure 3.6 shows the steady state CCM waveforms, where the inductor charging period T_1 is further sub-divided into two for the studied two-input MPC. This sub-division is directly proportional to the number of input sources of T_A providing a simultaneous power transfer. During T_1, switches S_{4b}, S_{5b} and S_{2b} are all ON. However, in the first subdivision of T_1, the inductor voltage V_L is equal to V_1, which is the source voltage with the highest potential difference. Accordingly, L charges with a gradient of V_1/L. When the first subdivision period of T_1 is over, S_{4b} is turned OFF while S_{5b} and S_{2b} remain ON. In the second subdivision of T_1, V_L becomes V_2 while the inductor continues to charge with a gradient of V_2/L. This process will continue with more than two inputs in the decreasing order of the magnitude in their input voltages. When the inductor charging period is over, S_{5b} and S_{2b} are turned OFF, being immediately followed by the discharging period T_2. During T_2, L discharges through the capacitor to the DC bus by switching ON S_{1a} and S_{3a}, thus V_L becomes $-V_o$, while L discharges

with a slope of the sum of the input voltages during their respective ON time divided by the inductance. Therefore, L will discharge with a gradient of $(D_{1eff}+D_{2eff}V_2)/L$ during T_2 as shown in Figure 3.6.

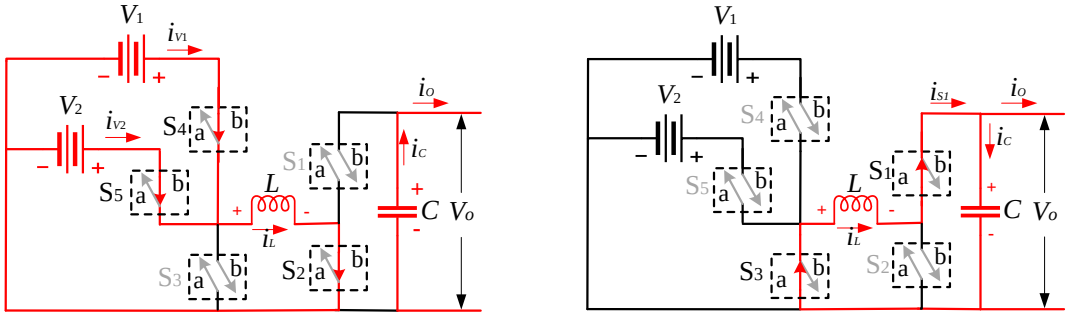


Figure 3. 5: Path of current flow during mode E for inductor (a) charging and (b) discharging during steady state operation.

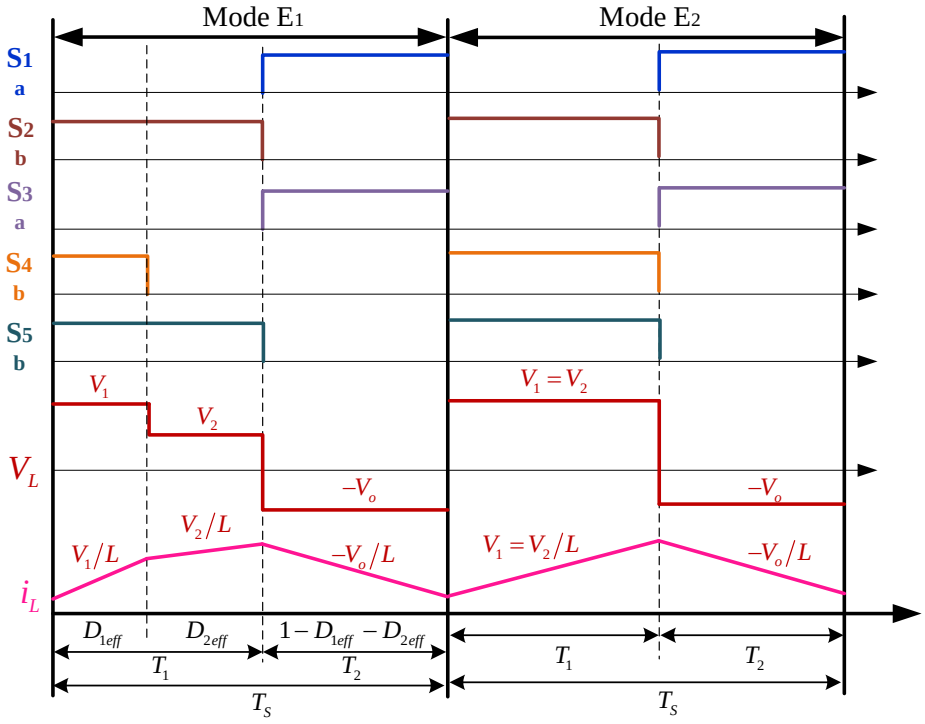


Figure 3. 6: Steady-state CCM waveform in mode E.

For an effective commutation in mode E, some basic principles need to be respected to achieve the simultaneous power transfer to the load. When the voltages are unequal in mode E_1 in Figure 3.6, with magnitude of the sources arbitrarily arranged in order of decreasing magnitudes such that $V_1 > V_2 > \cdots > V_N$ for N input ports, then the duty cycle of the PWM signal controlling the input sources (S_{4b} and S_{5b} in the two input T_A) must be in such a way that $D_1 < D_2 < \cdots < D_N$ and vice versa, where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ... ,

$D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. If the source magnitudes are equal such that $V_1 = V_2 = \cdots = V_N$ for *N* input ports in mode E_2, duty cycles of the PWM signal controlling the input sources (S_{4b} and S_{5b} in the case of the two input converter) must be as $D_1 = D_2 = \cdots = D_N$ in order to achieve the equal power delivery from the sources. If it is required that the power delivery from the sources must be unequal, then the values of $D_1, D_2, \ldots, D_N$ can be determined in order of increasing magnitude of the required power delivery from the respective sources. The relationship between the input sources and output voltage in steady state is given by (3.2) for *N* input sources.

$$V_o = \left[\sum_{i=1}^{N} D_{(i)eff} V_i\right] \Big/ \left[1 - \sum_{i=1}^{N} D_{(i)eff}\right] \tag{3.2}$$

The simplicity of control is one of the key merits of T_A as other MPCs would require a multiple-input multiple output (MIMO) control structure. T_A only requires a single-input single-output (SISO) control structure. The closed-loop operation using a double-loop PI controller is illustrated in Figure 3.7. The control layer consists of the secondary and primary controller, which is the double loop PI controller, the power management controller (PMC) and the pulse width modulator (PWM). The secondary controller sets the output voltage reference ($V_{o\text{-}ref}$), depending on T_A's mode of operation. It also determines the proportion of power flow from the sources when operating in a simultaneous power flow mode or mode E. To do this, it determines a scaling factor k_1 to k_{N-1}, which is obtained by comparing the total power capacity (kw_T) of all the sources to the individual power capacities (kw_1 to kw_N) for sources (V_1 to V_N) as described in (3.3), respectively, or based on other pre-programmed constraints, such as the state of charge (SoC).

$$\left.\begin{aligned} & k_1 = \frac{kw_1}{kw_T} \\ \left(kw_T = kw_1 + \cdots + kw_N\right), \quad & \vdots \\ & k_{N-1} = \frac{kw_{N-1}}{kw_T} \end{aligned}\right\} \tag{3.3}$$

The output voltage (V_O) and inductor current (i_L) are used to determine the control variable D_C. D_C is the effective ON time to charge the inductor to achieve the target output voltage as described in (3.4). To achieve the desired controller performance, the linearised inner current and output voltage-loop transfer functions, G_{id}, (3.5) and G_{vd}, (3.6), are developed. The PI gains of controllers, C_i and C_v, are heuristically selected to achieve the desired performance.

$$D_C = \sum_{i=1}^{N} D_{(i)eff} \tag{3.4}$$

$$G_{id} = \frac{\left[s\left(\sum_{i=1}^{N} D_{(i)eff} V_i \right) \Big/ L \right] + \left[\left(\sum_{i=1}^{N} D_{(i)eff} V_i \right) \Big/ RLC \right]}{s\left(s + \frac{1}{RC} \right) + \frac{1}{LC}} \tag{3.5}$$

$$G_{vd} = \left[\left(\sum_{i=1}^{N} D_{(i)eff} V_i \right) \Big/ LC \right] \Big/ \left[s\left(s + \frac{1}{RC} \right) + \frac{1}{LC} \right] \tag{3.6}$$

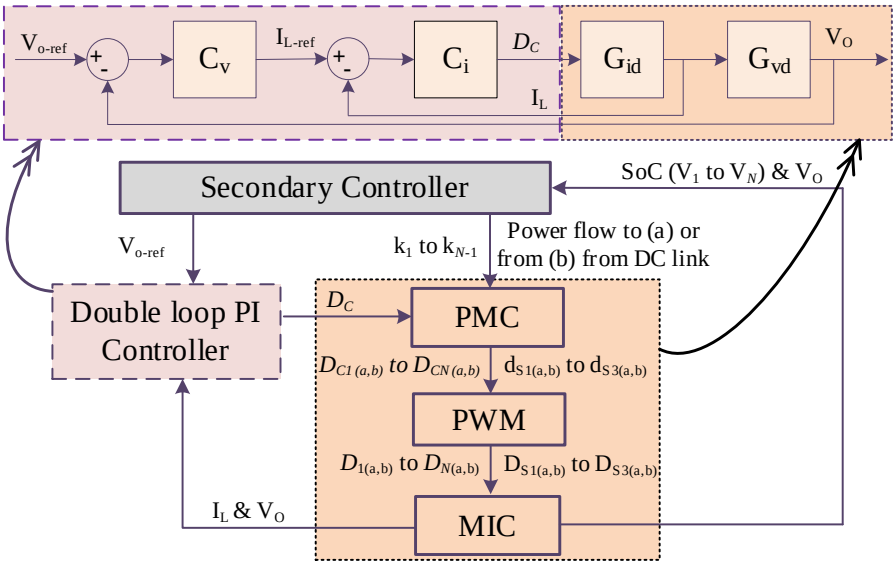


Figure 3. 7: Converter operational control structure.

Table 3. 1: Parameter scaling by the PMC and PWM

Mode of Operation		PMC	PWM
Mode A or B (V_i to V_O)	T_1	$D_C=D_{Ci(b)}=d_{S2b}$	D_{ib} goes to $S_{(i+3)b}$& D_{S2b} to S_{2b}
	T_2	$1–D_C=d_{S1a}=d_{S3a}$	D_{Sia} goes to S_{1a}& D_{S3a} to S_{3a}
Mode C or D (V_O to V_i)	T_1	$D_C=d_{S1b}=d_{S3b}$	D_{S1b} goes to S_{1b}.& D_{S3b} to S_{3b}
	T_2	$1–D_C=D_{Ci(a)}=d_{S1a}=d_{S3a}$	D_{ia} goes to $S_{(i+3)a}$& D_{S2a} to S_{2a}
Mode E ($\sum_{i=1}^{N} V_i$ to V_O)	T_1	$D_C=d_{S2b}$& scaled using (9)	D_{ib} to D_{Nb} goes to $S_{(i+3)b}$ to S_{Nb} & D_{S2b} to S_{2b}
	T_2	$1–D_C=d_{S1a}=d_{S3a}$	D_{Sia} goes to S_{1a}& D_{S3a} to S_{3a}

The operation of the PMC and the PWM is summarised on Table 3.1. The function of the PMC is to adequately manage power and energy supply among sources based on instructions from the secondary controller. At the output of the PMC, $D_{C1(a,b)}$ to $D_{CN(a,b)}$ corresponding to $D_{1(a,b)}$ to $D_{N(a,b)}$ at the output of the PWM refer to the duties applied to the switches controlling the respective input ports i.e. S_{i+3} to S_{N+3}. While $d_{S1(a,b)}$ to $d_{S3(a,b)}$ corresponding to $D_{S1(a,b)}$ to $D_{S3(a,b)}$ at the output of

the PWM refer to the duties applied to S_1 to S_3. In mode E, the sum of currents from the sources is presented in (3.7), and the PMC determines $D_{C1b} - D_{CNb}$ according to (3.8).

$$I_1 + I_2 + \cdots + I_N = I_L\left(\sum_{i=1}^{N} D_{(i)eff}\right) \tag{3.7}$$

$$\left.\begin{aligned} D_{C1b} = D_{1eff} &= k_1\left(\sum_{i=1}^{N} D_{(i)eff}\right) \\ &\vdots \\ D_{C(N-1)b} = D_{N-1eff} &= k_{N-1}\left(\sum_{i=1}^{N} D_{(i)eff}\right) \\ D_{CNb} = D_{Neff} &= \sum_{i=1}^{N} D_{(i)eff} - \sum_{i=1}^{N-1} D_{(i)eff} \end{aligned}\right\} \tag{3.8}$$

3.2 Proposed MPC topology B (T_B)

3.2.1 Circuit description

Figure 3.8 presents the T_B, a non-isolated MPC, consisting of two inductors, one capacitor, RBSs and FBSs. T_B is of the H-bridge structure with buck-boost characteristics, cognate to the MPCs proposed in [38, 93] and essentially an improvement to T_A. The input sources are grouped into two clusters with one consisting of the energy sources and the other energy storages. The energy source cluster, which can be used in integrating sources such as solar PVs, is highlighted in blue color in Figure 3.8 with the associated inductor. Since the energy sources are unidirectional in nature, RBSs are used to integrate them into the converter system. Conversely, the energy storage (e.g., battery, supercapacitors etc.) cluster highlighted in red color utilises FBSs since they are bidirectional in nature. The proposed MPC is thus robust, being capable of over twenty different modes of operation for a two-cluster configuration consisting of two inputs per cluster. In this configuration, the MPC operation summarized on Table 3.2 can be classified into the single- and multi-input interaction. The single-input interaction covers bidirectional power flow between the dc link and the energy storage cluster (V_3 and V_4) individually. Similarly, unidirectional power flow from the energy source cluster (V_1 and V_2) to the dc link and to the energy storage cluster (V_3 and V_4) individually. The multi-input interaction consists of several combinations of power flow across both clusters to deliver power to the dc link simultaneously. T_B can

also deliver power simultaneously from all or any combination of the inputs to the dc link and simultaneously from the energy source cluster to the energy storage cluster individually.

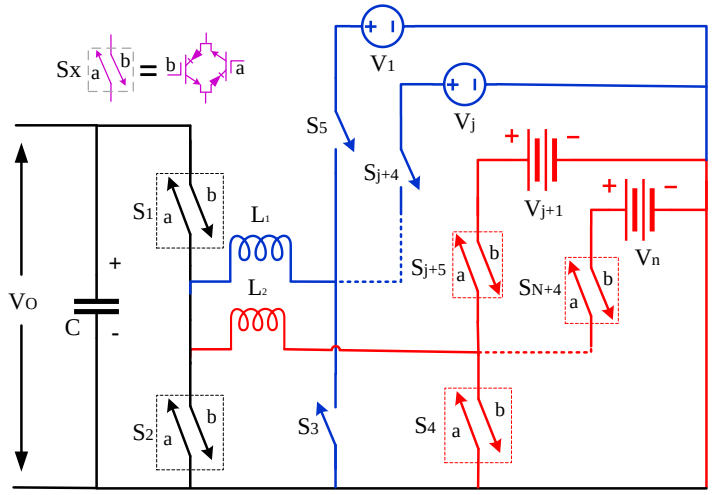


Figure 3. 8: Circuit schematic of T_B for integrating multiple energy sources and storages.

In contrast to conventional MPCs, which require n inductors for N input sources and two additional switches [38], T_B utilizes only one inductor per cluster and for any input sources. It needs only one additional FBS or RBS when introducing an input port to any of the respective clusters. Further, T_B can integrate both energy sources and storages as against its close competitor in [93], which can only integrate storages. Six key operating modes of the proposed MPC as illustrated in Figure 3.9 are analysed for steady state continuous conduction modes (CCM) of operation in the following sub section.

3.2.2 Steady state analysis

The single input interaction between the ports of T_B basically refer to independent power flow from the input ports to the dc link, the reverse flow of power from the dc link to the energy storage cluster and similarly the individual recharging of the energy storages directly from the energy source cluster. The switching pattern for these modes of operation are summarized in the first ten rows of Table 3.2. Also, the illustration of the path of current flow and steady state waveforms in CCM are presented in Figures 3.9 and 3.10, respectively.

From the CCM waveforms in steady state shown in Figure 3.10 and the switching patterns on Table 3.2, in single-input interaction, the switching period T_s is divided into two, T_1 and T_2, for the inductor charging and discharging periods, respectively. These modes are basically similar in operation to the standard non-inverting buck-

boost converter. Using the volt-second balance analysis on the steady state waveform of the converter presented in Figure 3.10, it can be observed that this converter can operate in the buck or boost modes depending on the duty ratio 'd_x' applied across the switches. Where d_x is the ratio of the respective inductor charging time to the total switching period, that is $d_x = T_1/T_S$. Therefore, the conventional equation (3.9) describing the relationship between the input and output voltage of the basic buck-boost converter applies to this converter as well for single input interaction modes.

Table 3. 2: Switching pattern for the different modes of operation

Mode of Operation		Switching Pattern	
		T_1	T_2
Single input interaction	V_1 to dc link	S_5, S_{2b}	S_3, S_{1a}
	V_2 to dc link	S_6, S_{2b}	S_3, S_{1a}
	V_3 to dc link	S_{7b}, S_{2b}	S_{4a}, S_{1a}
	V_4 to dc link	S_{8b}, S_{2b}	S_{4a}, S_{1a}
	dc link to V_3	S_{1b}, S_{4b}	S_{7a}, S_{2a}
	dc link to V_4	S_{1b}, S_{4b}	S_{8a}, S_{2a}
	V_1 to V_3	S_5, S_{4b}	S_3, S_{7a}
	V_1 to V_4	S_5, S_{4b}	S_3, S_{8a}
	V_2 to V_3	S_6, S_{4b}	S_3, S_{7a}
	V_2 to V_4	S_6, S_{4b}	S_3, S_{8a}
Multiple input interaction	V_1 & V_2 to V_3	S_5, S_6, S_{4b}	S_3, S_{7a}
	V_1 & V_2 to V_4	S_5, S_6, S_{4b}	S_3, S_{8a}
	V_1 & V_2 to dc link	S_5, S_6, S_{2b}	S_3, S_{1a}
	V_3 & V_4 to dc link	S_{7b}, S_{8b}, S_{2b}	S_{4a}, S_{1a}
	V_1 & V_3 to dc link	S_5, S_{7b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_2 & V_3 to dc link	S_6, S_{7b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_1 & V_4 to dc link	S_5, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_2 & V_4 to dc link	S_6, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_1, V_2 & V_3 to dc link	S_5, S_6, S_{7b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_1, V_2 & V_4 to dc link	S_5, S_6, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_1, V_3 & V_4 to dc link	S_5, S_{7b}, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_2, V_3 & V_4 to dc link	S_6, S_{7b}, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
	V_1, V_2, V_3 & V_4 to dc link	S_5, S_6, S_{7b}, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}

$$V_{out} = \frac{T_1}{T_2} V_{in} = \frac{d_x}{1 - d_x} V_{in} \tag{3.9}$$

The multi-input mode, where both energy sources (i.e. cluster 1) V_1 and V_2 are simultaneously supplying the dc bus is illustrated in Figures 3.9 (a) and 3.10 (V_1 & V_2 to dc link). During this mode of operation, the inductor charging period, T_1

is further subdivided into two or more, depending on the number of simultaneous input sources. This study analyses two inputs for the first cluster of the MPC thus only two sub-divisions of T_1 are required. During time T_1, switches S_5, S_6 and S_{2b} are all switched ON. However, in the first subdivision of T_1, the voltage across the inductor is the highest source voltage V_1. When the first subdivision period of T_1 is over, S_5 is OFF while S_6 and S_{2b} remain ON. In the second subdivision of T_1, the voltage across the inductor becomes V_2. This process will continue if the MPC had more than two inputs for the first cluster, in decreasing order of the magnitude in their input voltages. When T_1 is over, S_6 and S_{2b} are OFF, and the discharging period T_2 starts. During T_2, L_1 discharges through the capacitor C to the dc bus by turning ON S_{1a} and S_3, so the voltage across the inductor is $-V_o$. The effective voltage across the inductor from each input is given by the product of the effective ON time of that input and its voltage magnitude. As shown in Figure 3.10 (V_1 & V_2 to dc link), this effective voltage is $D_{1eff}V_1$ for the first subdivision of the inductor charging time and $D_{2eff}V_2$ for the second subdivision. Therefore, L_1 will charge with a gradient of $(D_{1eff}V_1 + D_{2eff}V_2)/L_1$ during T_1 while it discharges with a slope of $-V_o/L_1$ during T_2.

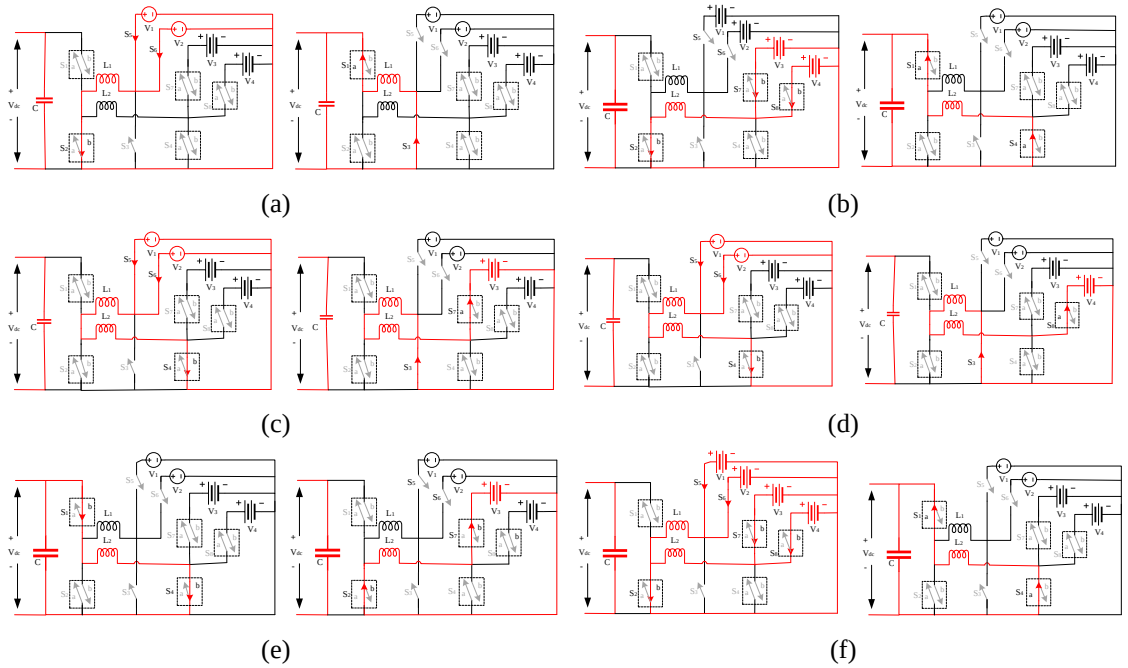


Figure 3. 9: Path of current flow in T_B during the charging and discharging of the inductors where (a) is simultaneous power flow from energy source cluster to the dc link, (b) is simultaneous power flow from energy storage cluster to the dc link, (c & d) is simultaneous power flow from energy source cluster to the energy storage cluster respectively, (e) is power flow from the dc link to the first storage device and (f) is simultaneous power flow from both clusters to the dc link.

Similarly, for simultaneous power flow from both energy storages (cluster 2), in which V_3 and V_4 are simultaneously supplying the dc bus as illustrated in Figures 3.9 (b) and 3.10 (V_3 & V_4 to dc link), T_1 is also subdivided into two. During T_1, switches S_{7b}, S_{8b} and S_{2b} are all switched ON. In the first subdivision of T_1, the voltage across the inductor is the highest source voltage V_3. When the first subdivision of T_1 is over, S_{7b} is OFF while S_{8b} and S_{2b} remain ON. In the second subdivision of T_1, the voltage across the inductor becomes V_4. During T_2, L_2 discharges through capacitor C to the dc bus by turning ON S_{1a} and S_4, so the voltage across L_2 is $-V_o$. Therefore, as shown in Fig. 3.10 (V_3 & V_4 to dc link), the effective voltage for the first subdivision of the inductor charging time is $D_{3eff}V_3$ and $D_{3eff}V_4$ for the second subdivision. Therefore, L_2 will charge with a gradient of $(D_{3eff}V_3 + D_{4eff}V_4)/L_2$ during T_1 while it discharges with a slope of $-V_o/L_2$ during T_2.

Likewise, for simultaneous power flow from both clusters to the dc link, V_1, V_2, V_3 and V_4 are simultaneously supplying the dc bus as illustrated in Figs. 3.9 (f) and 3.10 (All inputs to dc link). Just as described above for simultaneous power transfer exclusively from each cluster, L_1 and L_2 are simultaneously time multiplexed to achieve concurrent power delivery to the dc link from all input sources. During time T_1, switches S_5, S_6, S_{7b}, S_{8b} and S_{2b} are all switched ON, in the first subdivision of T_1, the voltage across the L_1 and L_2 is V_1 and V_3, respectively. When the first subdivision of T_1 is over for any or both clusters S_5 and S_{7b} is OFF while S_6, S_{8b}, and S_{2b} remain ON until the end of the second subdivision when they are all OFF. During T_2, L_1 and L_2 are discharged through the capacitor C to the dc bus by turning ON S_{1a} S_3 and S_4, so the voltage across the inductor is $-V_o$. Hence, as shown in Fig. 3.10 (All inputs to dc link), the effective voltage of L_1 charging time is $D_{1eff}V_1$ and $D_{2eff}V_2$ for the first and second subdivision, respectively. And that of L_2 is $D_{3eff}V_3$ and $D_{4eff}V_4$ for the first and second subdivision, respectively. Therefore, L_1 and L_2 will charge with a gradient of $(D_{1eff}V_1 + D_{2eff}V_2)/L_1$ and $(D_{3eff}V_3 + D_{4eff}V_4)/L_2$ during T_1 while they both discharge with a slope of $-V_o/L_1$ and $-V_o/L_2$, respectively, during T_2.

Further, for simultaneous power flow from both energy sources (cluster 1) V_1 and V_2 to the energy storages (cluster 2) V_3 and V_4 as illustrated in Figures 3.9 (c & d) and 3.10 (V_1 & V_2 to V_3 & V_4), respectively, T_1 is also subdivided into two. During T_1, switches S_5, S_6 and S_{4b} are all switched ON. In the first subdivision of T_1, the voltage across L_1 and L_2 is the highest source voltage V_1 and -V_1, respectively.

When the first subdivision of T_1 is over, S_5 is OFF while S_6 and S_{4b} remain ON. In the second subdivision of T_1, the voltage across L_1 and L_2 becomes V_2 and $-V_2$, respectively. Therefore, as shown in Fig. 3.10, this effective voltage is $D_{1eff}V_1$ for the first subdivision of T_1 and $D_{2eff}V_2$ for the second subdivision. During T_2, L_1 and L_2 charge and discharge, respectively, to the energy storage cluster by turning ON S_3 and S_{7a} or S_{8a}, depending on which energy storage device is being recharged (V_3 or V_4 respectively). Therefore, the voltage across L_1 and L_2, respectively, during T_2 is $-V_3$ and V_3 or $-V_4$ and V_4, depending on which energy storage device is being recharged (V_3 or V_4 respectively). Thus, L_1 and L_2 will charge and discharge, respectively, with a gradient of $(D_{1eff}V_1 + D_{2eff}V_2)/L_1$ and $(D_{3eff}V_3 + D_{4eff}V_4)/L_2$ during T_1 while during T_2 they discharge and charge with a slope of $-V_3/L_1$ or $-V_4/L_1$ and V_3/L_2 or V_4/L_2, depending on the energy storage device being charged.

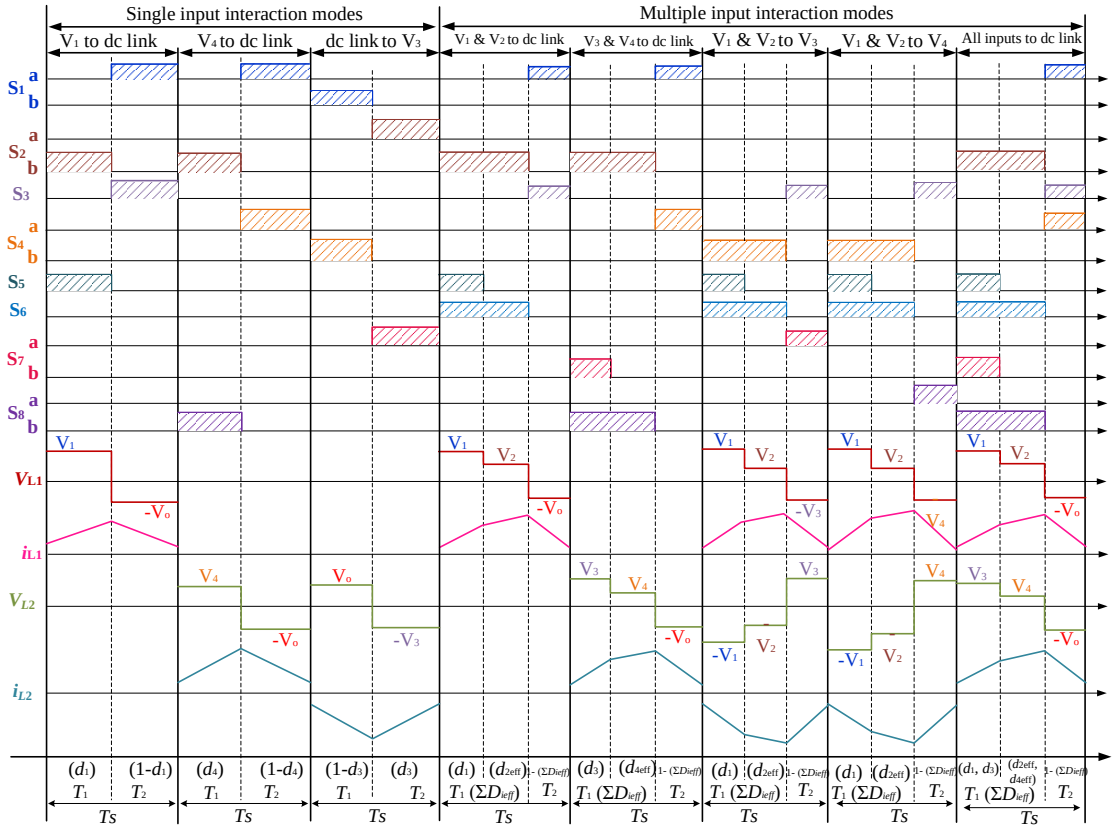


Figure 3. 10: Steady state waveforms of the MPC operation in CCM for key modes of operation.

By applying the volt-second balance to the steady state waveforms for multi-input interaction in Fig. 3.10, the relationship between the input sources and the output voltage is given by (3.10 – 3.11) for power delivery to the dc link exclusively from

cluster 1 and 2, respectively, and by (3.12) for when both clusters are supplying the dc link. For inter-port interaction, i.e. when the energy storages (cluster 2) are being recharged directly from cluster 1, the relationship between the source voltages and energy storage devices is described by (3.13).

$$V_O = \left[\sum_{i=1}^{j}\left(D_{(i)eff}V_i\right)\right] \Big/ \left[1-\sum_{i=1}^{j}D_{(i)eff}\right] \tag{3.10}$$

$$V_O = \left[\sum_{i=j+1}^{N}\left(D_{(i)eff}V_i\right)\right] \Big/ \left[1-\sum_{i=j+1}^{N}D_{(i)eff}\right] \tag{3.11}$$

$$V_O = \frac{\max.\left[\sum_{i=1}^{j}\left(D_{(i)eff}V_i\right), \sum_{i=j+1}^{N}\left(D_{(i)eff}V_i\right)\right]}{1-\left[\max.\left(\sum_{i=1}^{j}D_{(i)eff}, \sum_{i=j+1}^{N}D_{(i)eff}\right)\right]} \tag{3.12}$$

$$V_3 \, or \, V_4 = \left[\sum_{i=1}^{j}\left(D_{(i)eff}V_i\right)\right] \Big/ \left[1-\sum_{i=1}^{j}D_{(i)eff}\right] \tag{3.13}$$

Furthermore, just like in T_A, for effective commutation of switches in multi-input interaction, some principles need to be respected to achieve simultaneous power transfer to the dc link or energy storage cluster (cluster 2). If the magnitude of the input voltages per cluster is arbitrarily arranged in order of decreasing magnitudes such that $V_1 > V_2 > \cdots > V_j$ for cluster 1 and $V_{j+1} > V_{j+2} > \cdots > V_N$ for cluster 2, the duty cycles of the PWM signals of controlling the input ports per cluster, must be in such a way that $D_1 < D_2 < \cdots < D_j$ for cluster 1 and $D_{j+1} < D_{j+2} < \cdots < D_N$ for cluster 2 and vice versa. Where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, … , $D_j = D_{1eff} + D_{2eff} + \cdots + D_{jeff}$ and $D_{j+1} = D_{j+1eff}$, $D_2 = D_{j+1eff} + D_{j+2eff}$, … , $D_N = D_{j+1eff} + D_{j+2eff} + \cdots + D_{Neff}$, respectively, for clusters 1 and 2. However, if the voltage magnitudes of any clusters are equal such that $V_1 = V_2 = \cdots = V_j$ then the duty cycles of the PWM signals must be in such a way that $D_1 = D_2 = \cdots = D_j$ in order to achieve equal power delivery from each of the sources. If the required power delivery from the sources is unequal, then $D_1, D_2, \ldots, D_j$ can be determined in order of increasing magnitude from the respective sources.

3.3 Proposed MPC topology C (T_C)

3.3.1 Circuit description

The circuit schematic of T_C an isolated MPC with unipolar output is presented in Figure 3.11. It involves the use of a coupled inductor, a capacitor, a diode, an *RC*D clamping circuit, and RBSs controlling the respective input sources. The MPC is capable of unidirectionally bucking or boosting the input voltage depending on its application. It requires only one additional RBS (S_W) when additional inputs are being introduced. One of the main selling points of T_C is that contrary to conventional topologies where each input of the isolated MPC has its own primary winding, this MPC needs only one primary winding for any number of inputs, resulting in smaller size. Further, only one clamping circuit is required since only one primary winding is needed by T_C, control is also simple for passive clamping.

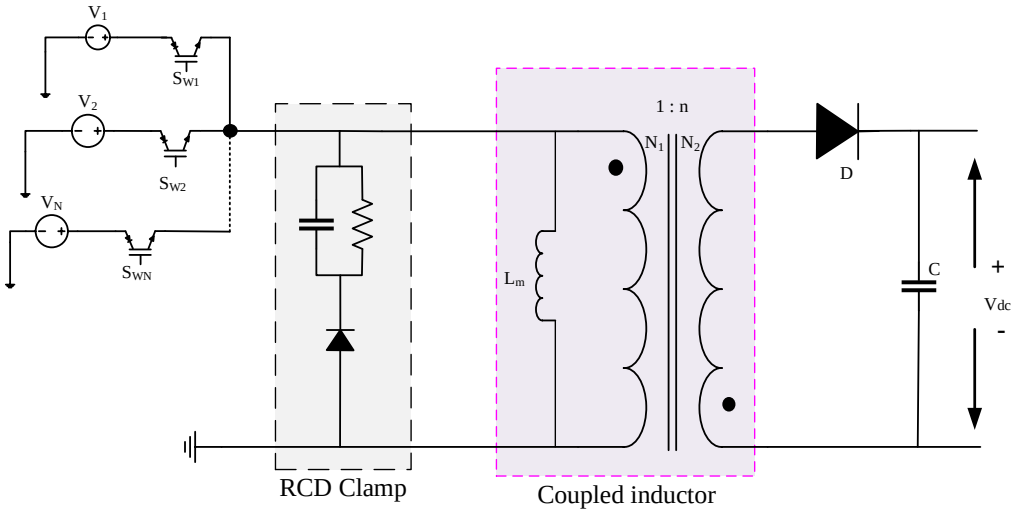
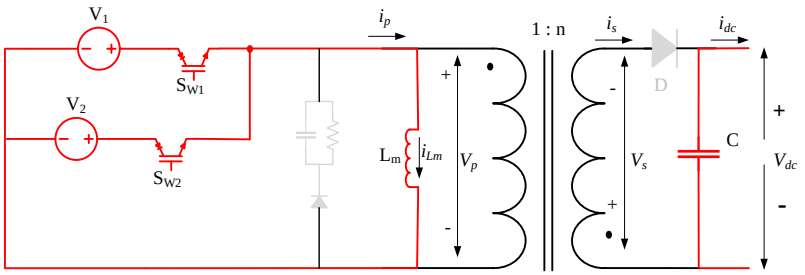


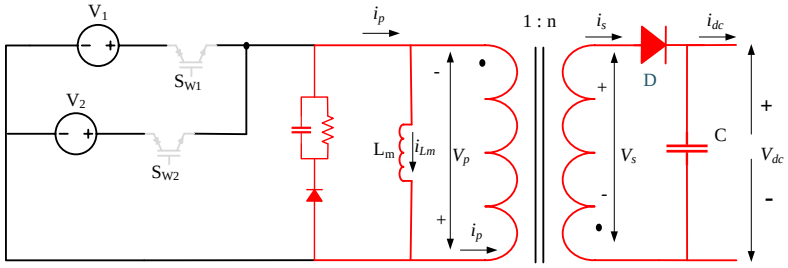
Figure 3. 11: Flyback-based isolated MPC.

3.3.2 Steady state analysis

In single input modes, when energy is delivered from only one of the inputs to the dc bus, that is from V_1 or V_2. The respective switch S_{W1} or S_{W2} is turned ON to charge the magnetizing inductance (L_m) for a period of DT_S, where D is the duty cycle and T_S is the total switching period. During switching time $(1-D)T_S$, the switch is turned OFF and then diode, D, conducts to discharge L_m to the dc bus. Thus, the converter will operate like a standard flyback converter, where (3.14) and (3.15) describe the relationship between input and output voltages for continuous conduction (CCM) and discontinuous conduction modes (DCM), respectively.



(a)



(b)

Figure 3. 12: Path of current during L_m (a) charging and (b) discharging for simultaneous operation of a two-input configuration of T_C.

$$V_{dc} = \frac{V_{in} D}{1-D} n \tag{3.14}$$

$$V_{dc} = V_{in} D \sqrt{\frac{R}{2L_m} T_S} \tag{3.15}$$

For simultaneous power transfers from two or more sources, as illustrated in Figure 3.12 with two input switches controlling all the sources are turned ON at the same time but turned OFF in the order of decreasing magnitude of the respective voltages. Therefore, the charging of L_m is time multiplexed as illustrated in Figure 3.13 for the operation of two simultaneous inputs.

In steady state CCM as illustrated in Figure 3.13, the switching period is divided into two main parts, the charging and discharging times of L_m. The first part is further subdivided depending on the number of inputs of T_C in simultaneous operation:two divisions (D_{1eff} and D_{2eff}) in this case while the second part remains fixed as $(1 - \sum_{i=1}^{N} D_{ieff})$ indicating the discharging time of L_m. When the switches are turned ON, current flows from the source with the highest potential first or V_1 in this case, so L_m is charged with a slope of V_1/L_m during D_{1eff}. When the time D_{1eff} is elapsed, V_2 takes over to continue charging L_m with a slope of V_2/L_m during D_{2eff}. This continues up to D_{Neff} with a slope of V_N/L_m for any number of inputs. At the end of the charging time, $\sum_{i=1}^{N} D_{ieff}$, L_m is discharged to the dc bus with a slope of $-[(V_{dc}/n)/L_m]$, where n is the turns ratio

N_2 / N_1 of the coupled inductor. By applying volt-second balance of the resulting steady state CCM waveform in Figure 3.13, the input-output voltage is described by (3.16).

$$V_{dc} = \left(\left[\sum_{i=1}^{N} V_i D_{ieff} \right] \Big/ \left[1 - \sum_{i=1}^{N} D_{ieff} \right] \right) n \tag{3.16}$$

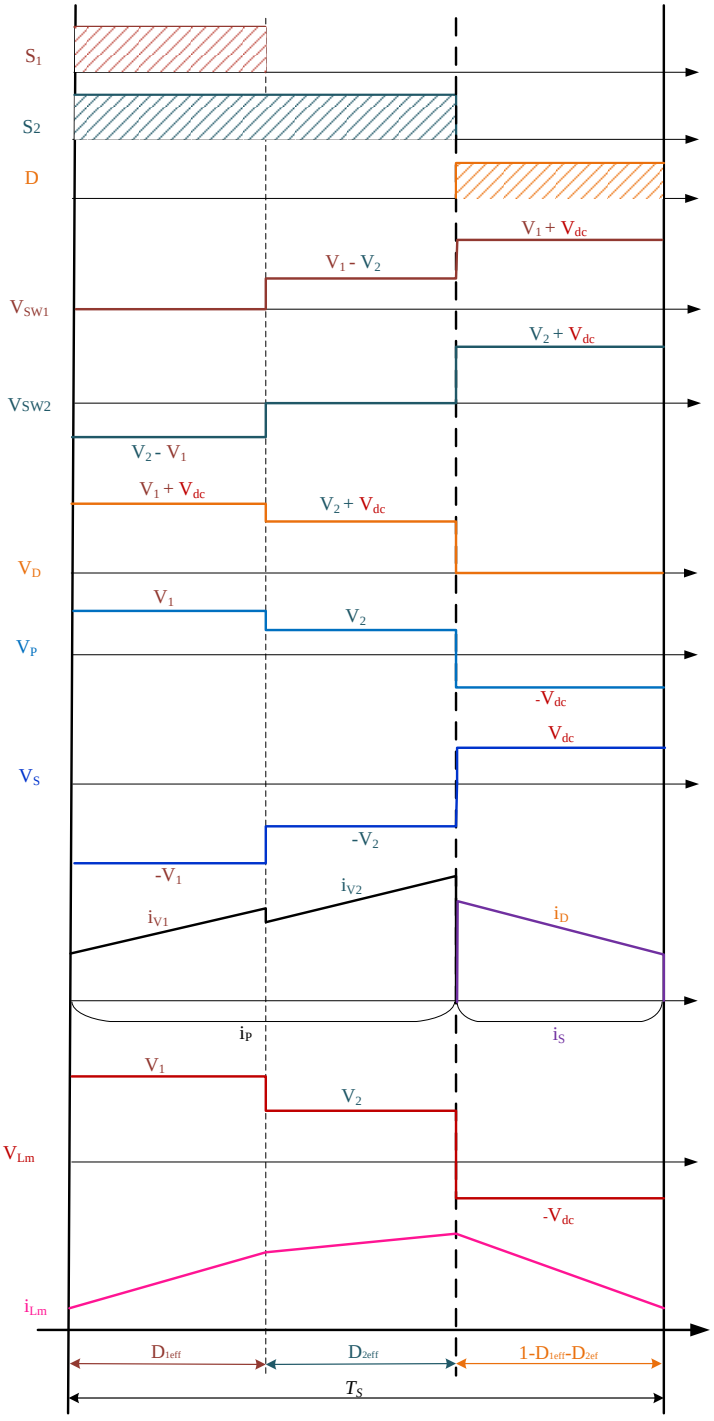


Figure 3. 13: Steady state CCM waveform for the MIC with two inputs.

For an effective commutation of the switches in multi-input mode, some principles need to be respected to achieve simultaneous power transfer to the load. When the voltages are unequal, the magnitude of the sources is arbitrarily arranged in order of decreasing magnitudes such that $V_1 > V_2 > \cdots > V_N$, the duty cycles of the PWM signals of controlling the input sources, e. g S_{W1} and S_{W2}, must be such that $D_1 < D_2 < \cdots < D_N$, and vice versa, where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ..., $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. However, if the source voltages are equal such $V_1 = V_2 = \cdots = V_N$, duty cycles of the PWM signals must be in such a way that $D_1 = D_2 = \cdots = D_N$ to achieve an equal power delivery from the sources. If the required power delivery from the sources is unequal, $D_1, D_2, \ldots, D_N$ can be determined in order of increasing magnitude of the required power delivery from the respective sources.

In the conventional application of flyback converters, a popular approach is its operation in DCM due to ease of stabilization and the possibility of zero current and voltage switching (ZCS and ZVS), although ZVS is only possible with additional circuitry. The steady state waveform for DCM operation of T_C is illustrated in Figure 3.14. The main difference between the DCM and the CCM operation previously described is that in DCM, L_m is designed to be much smaller than that required for CCM. Consequently, the slope of the current in L_m, the primary winding and the secondary winding is much steeper in DCM than in CCM. Therefore, at the end of each switching period, the core is completely discharged.

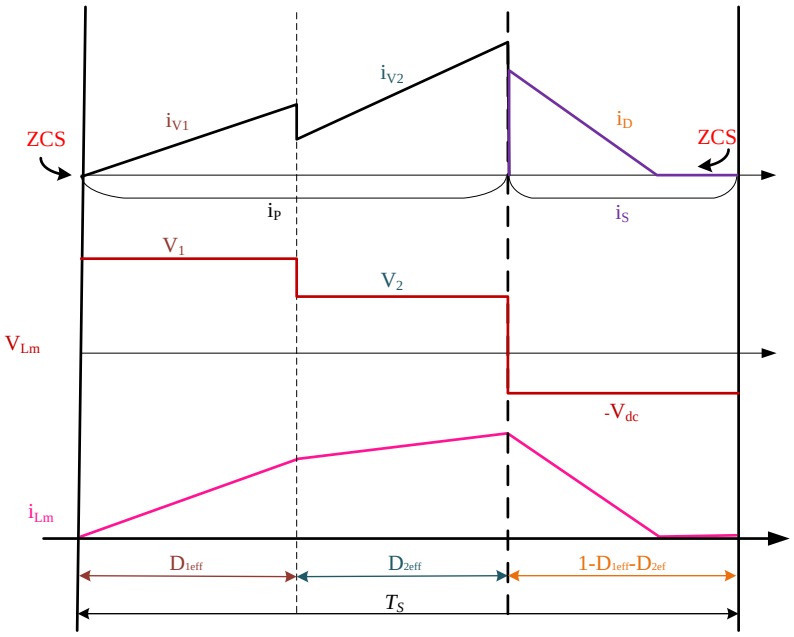


Figure 3. 14: Steady state DCM waveform for the two inputs configuration of T_C.

From the steady state DCM waveform presented in Figure 3.14, the input-output voltage relationship is described by (3.17), which is obtained by volt-second balance and balancing the input and output power such that DCM operation is guaranteed. From Fig. 3.14, it is observed that ZCS can be achieved at turn ON of switches S_{W1} to S_{WN} while the diode will also benefit from ZCS at its turn OFF. However, the conduction losses are much higher since the DCM has a higher peak current than CCM. Consequently, the inductor core will also be much larger at high power applications. Therefore, the DCM operation of the proposed MPC is only attractive for low power applications.

$$V_{dc} = \sum_{i=1}^{N} V_i D_{ieff} \sqrt{\frac{R}{2L_m} T_S} \tag{3.17}$$

3.4 Proposed MPC topology D (T_D)

3.4.1 Circuit description

T_D is a family of five (T_{D1} – T_{D5}) multiport bipolar dc-dc converters (MBDCs), being presented in Figure 3.15. It consists of five unidirectional non-isolated MBDCs, which are derived from the basic buck-boost converter. They all have bipolar symmetric outputs. The first three members, T_{D1} – T_{D3}, have their bipolar outputs derived from the Greinacher voltage doubler (GVD) while the last two, T_{D4} and T_{D5}, have their bipolar outputs derived from a synchronous buck converter (SBC). The MBDCs with bipolar outputs based on the GVD have a higher component count than those with bipolar outputs based on the SBC, but their control complexity is lower since the bipolar outputs do not need any controller to balance the output voltage as required in SBC output based MBDCs. Further, the MBDCs with two inductors (L_1 and L_2) switched by three diodes (D_1–D_3) at the dc conversion stage have higher gains than those with only one (MBDC types A and D). The switched inductor cells implemented to achieve high gain were first proposed in [94], but its application in T_{D2}, T_{D3}, and T_{D5} yields at least two times (2x) higher gain than that in [94]. Furthermore, they are all capable of simultaneous and independent power flow from the input ports to the bipolar dc links, being capable of producing three voltage levels, $\pm\frac{V_o}{2}$ and V_o. The proposed family of MBDCs allows for integrating RESs such as PV systems, wind turbine and fuel cells to a bipolar dc bus. For analysis, the input sources are referred to as basic dc

sources V_1–V_N. The following subsection presents the steady state analysis of the MBDCs in detail.

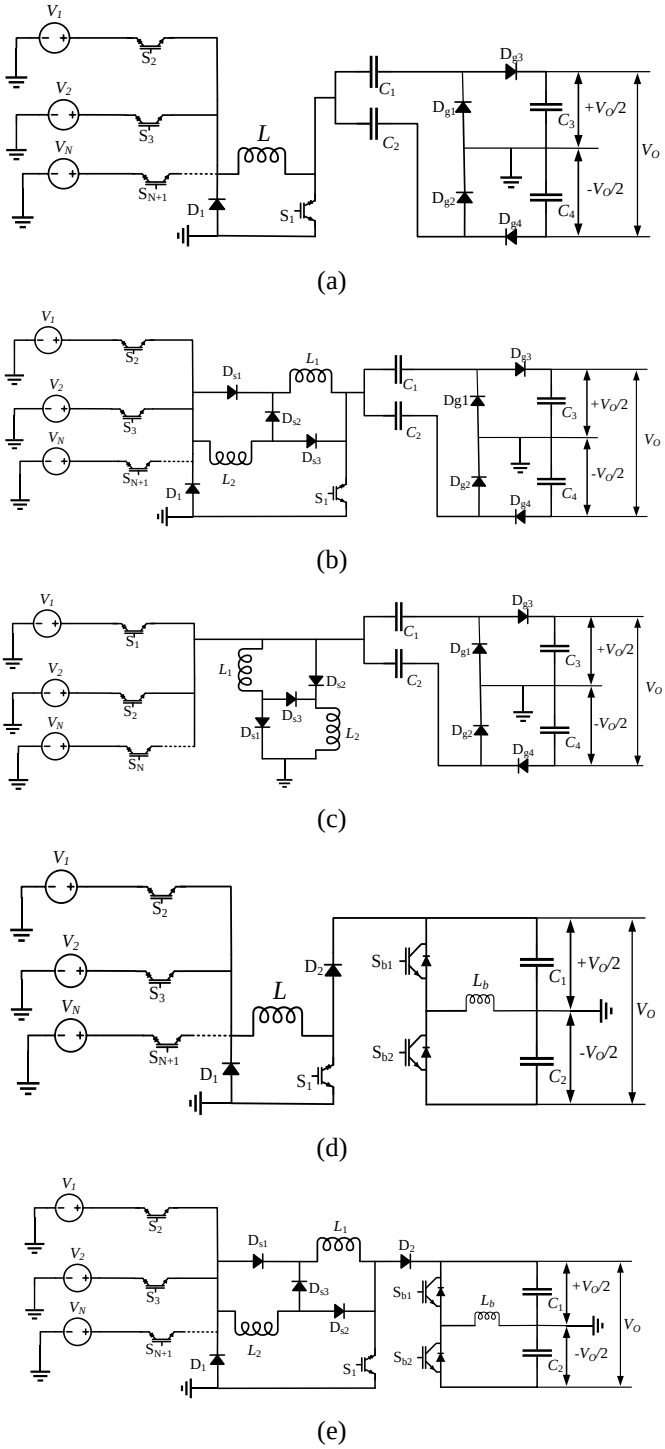


Figure 3. 15: Schematic of T_D with (a) T_{D1}, (b) T_{D2}, (c) T_{D3}, (d) T_{D4} and (e) T_{D5}.

3.4.2 Steady state analysis

T_{D1} is presented in Figure 3.15 (a) and it consists of five diodes, one inductor, four capacitors and N+1 reverse blocking switches, where N is the number of input ports to the MBDC. The capacitors, C_1 – C_4 and the diodes D_{g1} – D_{g4} are responsible for

the bipolar output stage based on the GVD. Meanwhile, switches S_1 – S_{N+1}, diode D_1 and inductor L, are responsible for the dc conversion stage. For T_{D1} with two inputs, Figure 3.16 (a) describes the path of current during the MBDC's operation during simultaneous power transfer from the two input ports to the dc link. Further, the steady state waveforms of this MBDC's operation with two inputs simultaneously for two scenarios, when the voltage of both input ports are equal ($V_1 = V_2$) and when they are unequal ($V_1 > V_2$) is presented in Figure 3.16 (b). For both scenarios, the switching period is divided into two main parts $\sum_{i=1}^{N} D_{ieff}$ and $1 - \sum_{i=1}^{N} D_{ieff}$. The first parts D_{1eff} and D_{2eff} are essentially D_{ieff}, since the MBDC is analysed for two voltage sources, referring to the effective time during which the sources are charging the inductor while the second main division, $1 - D_{1eff} - D_{2eff}$, is the discharging of the inductor.

All the switches S_1 – S_3 are turned ON at the same time during the switching period, T_S, with S_2 turned off and the end of D_{1eff} to end the inductor charging by V_1 and then V_2 is allowed to continue charging the inductor to until both S_1 and S_3 are turned OFF at the end of D_{2eff}. The inductor is charging with a slope of $\left(\sum_{i=1}^{N} D_{ieff} V_i\right)/L$ during which diodes D_{g1} and D_{g4} are discharging capacitors C_1 and C_2 to the dc link. At the end of the inductor charging time, it discharges to the dc link with a slope of $(-V_O/2)/L$ through D_1, D_{g2} and D_{g3}. The same charging and discharging actions of the inductor are observed when the input voltages are equal ($V_1 = V_2$). Similarly, in single input mode, i.e when only one of the sources is supplying the dc link, the inductor is charged with a slope of V_i/L during D_i for the respective input port. By applying volt-second balance on the steady state waveforms in Figure 3.16 (b), the output voltage, V_o, of T_{D1} is described by (3.18).

$$V_o = 2\left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3.18}$$

Figure 3.15 (b) presents T_{D2}, consisting of N+1 RBSs, eight diodes, two inductors and four capacitors. Like T_{D1}, C_1 – C_4 and the diodes D_{g1} – D_{g4} are also responsible for the bipolar output stage based on the GVD while the other components are responsible for the dc conversion stage with D_{s1} – D_{s3}, L_1 and L_2, forming the diode switched inductor component of the MBDC. Through the diode switched inductor component, T_{D2} can achieve a higher output voltage than T_{D1}. For the analysis of T_{D2} with two input voltages, the path of current flow and the steady state waveforms are shown in Figure 3.17, respectively. From these Figures, it can be

observed that the operation of T_{D2} is similar to that of T_{D1} except that the inductor L in T_{D1} is split into two, L_1 and L_2, in T_{D2} through the switched diodes. During the charging of L_1 and L_2, D_{s1} and D_{s2} are forward biased, and each inductor is charged with a slope of $\left(\sum_{i=1}^{N} D_{ieff} V_i\right)/L$, so in the discharging mode, D_1 and D_{s3} are forward biased while the inductor slope is $(-V_O/4)/L$ for each inductor. By applying volt-second balance on the steady state waveforms presented in Figure 3.17 (b), the output voltage, V_o, for T_{D2} is described by (3.19).

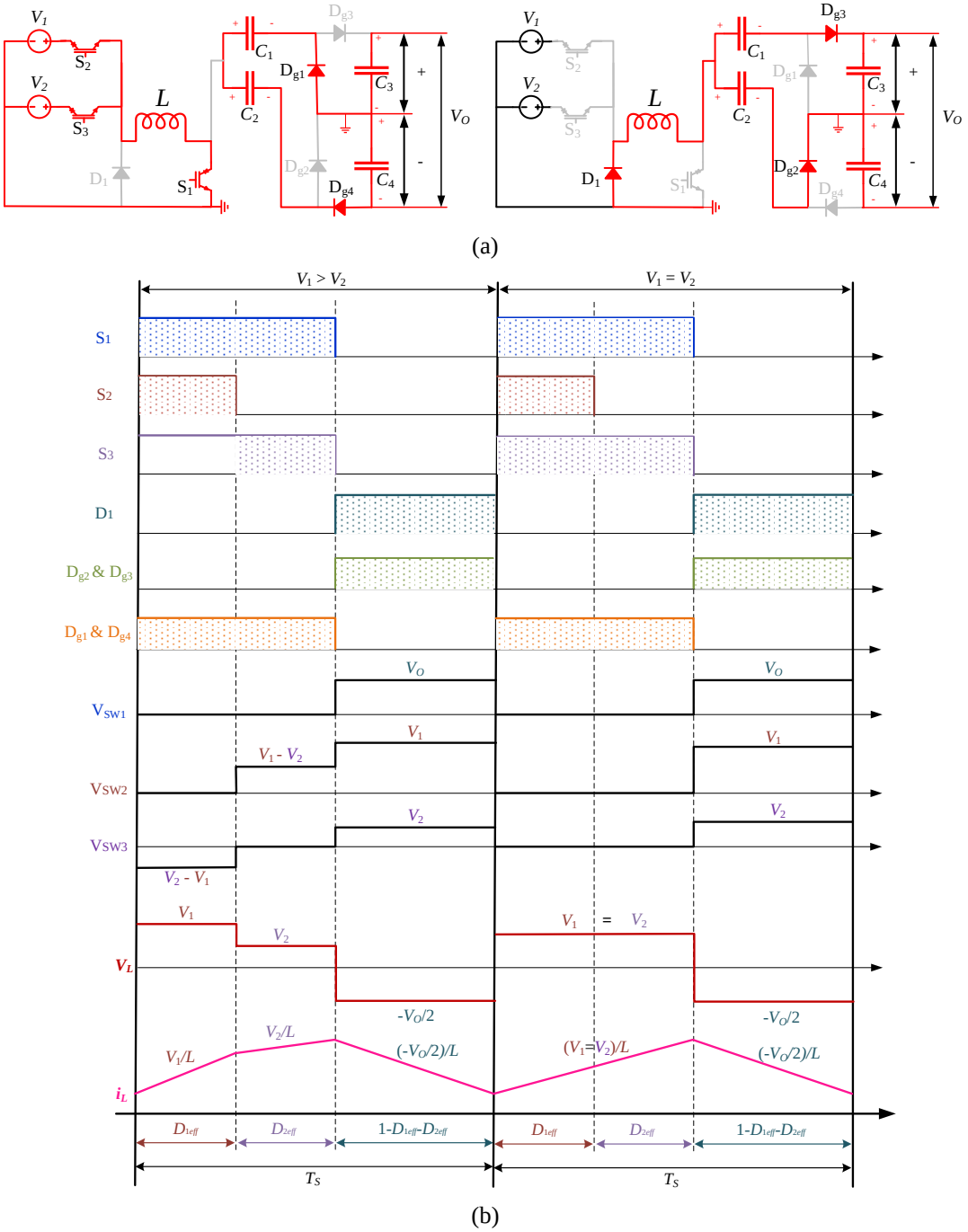


Figure 3. 16: T_{D1} with (a) path of current flow for inductor charging and discharging time, respectively, and (b) steady state CCM waveforms.

$$V_o = 4\left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3.19}$$

T_{D3} is presented in Figure 3.15 (c), consisting of N RBSs, seven diodes, two inductors and four capacitors, resulting in one less reverse blocking switch and diode than T_{D2}. For the analysis of T_{D3} with two input voltages, the path of current flow is presented in Figure 3.18 (a), and the steady-state waveforms are shown in Figure 3.18 (b). Like T_{D2}, capacitors $C_1 - C_4$ and the diodes D_{g1}–D_{g4} are also responsible for the bipolar output stage based on the GVD while D_{s1}–D_{s3}, S_1–S_N, L_1 and L_2 are responsible for the dc conversion stage. In T_{D3}, diode switched inductor components are directly connected to ground, thus the currents through L_1 and L_2 are higher than those of T_{D2}. Therefore, although each inductor is charged with a slope of $\left(\sum_{i=1}^{N} D_{ieff} V_i\right)/L$ when D_{s1} and D_{s2} are forward-biased during $\sum_{i=1}^{N} D_{ieff}$, each inductor discharges with a slope of $(-V_O/8)/L$. By applying volt-second balance on the steady state waveforms presented in Figure 3.18 (b), the output voltage, V_o, for T_{D3} is described by (3.20).

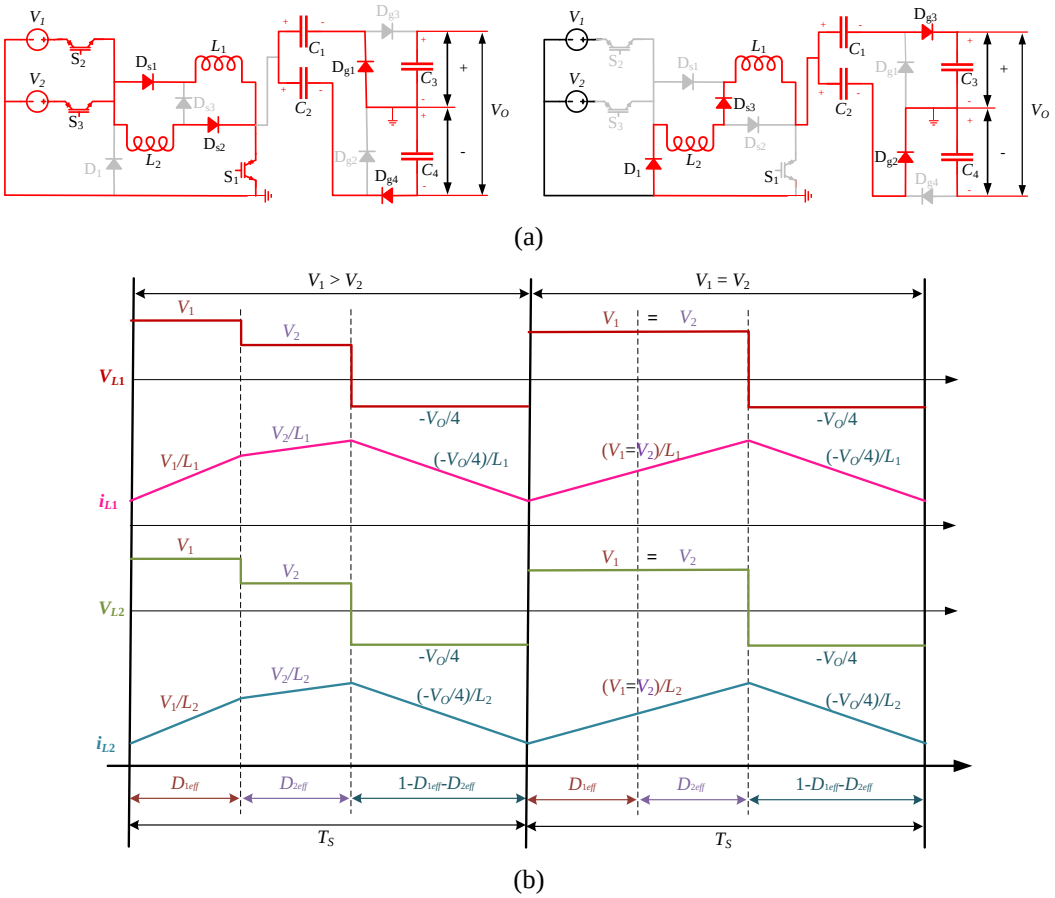
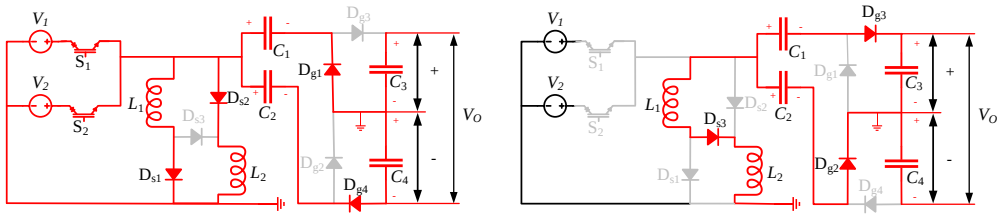


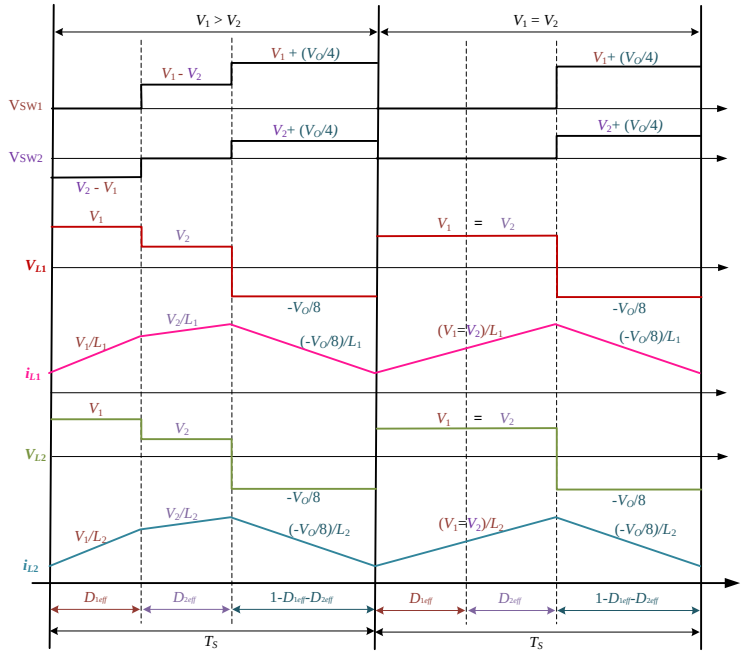
Figure 3. 17: T_{D2} with (a) path of current flow for inductor charging and discharging time, respectively, and (b) steady state CCM waveforms.

$$V_o = 8\left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3.20}$$

The circuit topologies for T_{D4} and T_{D5} are presented on Figure 3.15 (d) and (e), respectively, except that the GVD based bipolar dc bus is replaced with a SBC based bipolar dc bus. T_{D4} has two capacitors and four diodes less than T_{D1}, but one half-bridge switch is introduced alongside diode, D_2, and inductor, L_b, in T_{D4}. For the analysis of T_{D4} with two input sources, the path of current flow is presented in Figure 3.19 (a) and the steady state waveforms are shown in Figure 3.19 (b). The operation of T_{D4} is similar to that of T_{D1} except that during the discharging of the inductor, both D_1 and D_2 are forward-biased. Further, the bipolar dc bus switches S_{b1} and S_{b2} are independently and synchronously controlled with a constant duty cycle of 50% to ensure that the bipolar output voltages, $\pm\frac{V_o}{2}$, are balanced irrespective of the possible imbalance in the loads applied across the different poles. Although an additional control is required, the open loop control is sufficient to maintain balanced output voltages.



(a)



(b)

Figure 3. 18: T_{D3} with (a) path of current flow for inductor charging and discharging time respectively and (b) steady state CCM waveforms.

Similarly, T_{D5} in Figure 3.15 (e), has two capacitors and four diodes less than T_{D2}, but like T_{D4}, one switch half-bridge, diode, D_2, and inductor, L_3, are introduced. Comparing the path of current flow presented in Figure 3.20 (a) and the steady state waveforms in Figure 3.20 (b) for the analysis of T_{D5} with two input voltage sources, to that of T_{D2}, it can be observed that they are both similar except that when the inductors, L_1 and L_2, are discharging, diodes D_1, D_2 and D_{s3} are forward-biased. Further, its bipolar dc bus behaves exactly as that of T_{D4}. By applying volt-second balance on the steady state waveforms of T_{D4} and T_{D5}, the output voltages are the same as those of T_{D1} and T_{D2}, which are, (3.18) and (3.19), respectively.

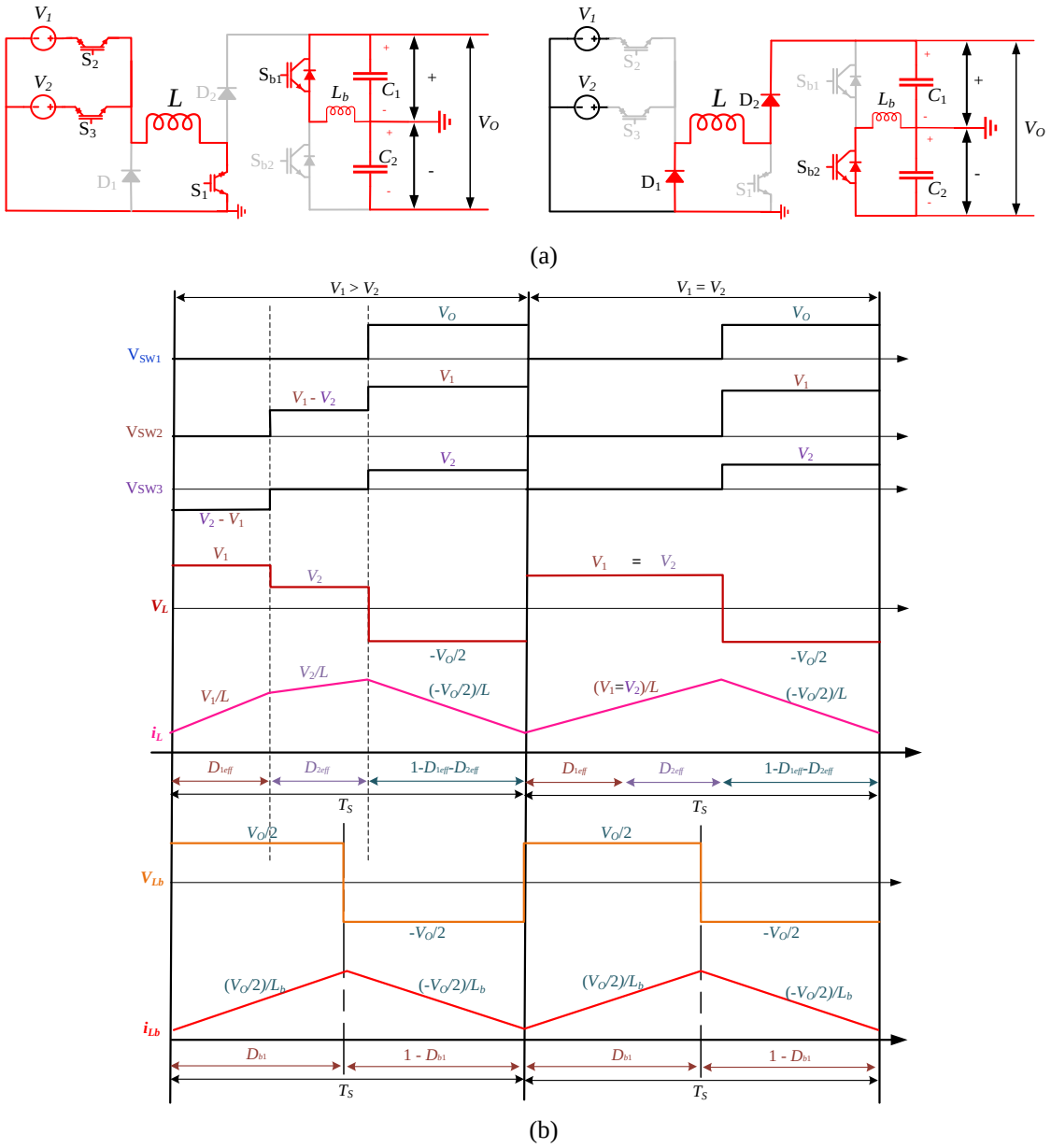
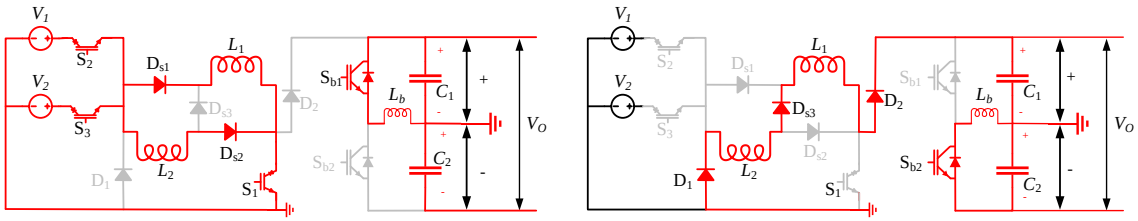
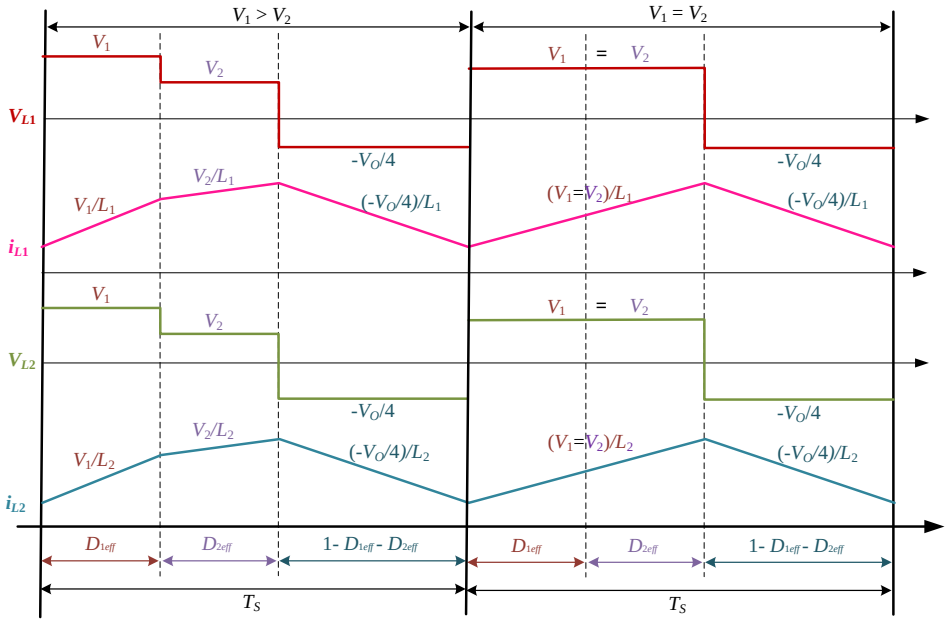


Figure 3. 19: T_{D4} with (a) path of current flow for inductor charging and discharging time respectively and (b) steady state CCM waveforms.

One key feature of the MBDCs in T_D is that independent power flow from the input sources to the bipolar dc link can be carried out arbitrarily. To achieve this, the switch controlling the input port, which is not required to supply the dc link, is turned OFF throughout the switching period. For example, if V_1 is required to supply the dc link for T_{D1}, during the inductor charging time (D_{ieff}), S_1 and S_2 are turned ON with the same duty cycle (D_{1eff}). After this, the inductor discharges through forward-biasing D_1 exactly as described earlier during simultaneous power flow mode, while S_3 is left OFF for the entire switching period. Similarly, if V_2 is required to supply the dc link, S_1 and S_3 are turned ON with the same duty cycle (D_{2eff}) during the inductor charging time (D_{ieff}) while S_2 is left OFF for the entire switching period. Further, arbitrary independent power flow is achieved in similar fashion for all the other members of the family, including in T_{D3} for which the switch controlling the input sources V_1 and V_2 are S_1 and S_2, respectively.



(a)



(b)

Figure 3. 20: T_{D5} with (a) path of current flow for inductor charging and discharging time, respectively and (b) steady state CCM waveforms.

For MBDCs in T_D to effectively operate in simultaneous power transfer from the input ports to the dc link, some principles need to be respected. When the voltages are unequal, the sources are arbitrarily arranged in the controller in order of decreasing magnitude such that $V_1 > V_2 > \cdots > V_N$ for N input ports, the duty cycle of the switches controlling the respective input ports (i.e., S_2 to S_{N+1} for T_{D1}, T_{D2}, T_{D4} & T_{D5} and S_1 to S_N for T_{D3}), must be in such a way that $d_1 < d_2 < \cdots < d_N$ and vice versa, where $d_1 = D_{1eff}$, $d_2 = D_{1eff} + D_{2eff}$, $\cdots$, $d_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. If the source voltages are equal, such that $V_1 = V_2 = \cdots = V_N$, the duty cycles controlling the respective input sources can be equal or in order of increasing the magnitude of power required from each respective source. However, in all cases except type C, the duty cycles applied to S_1 for all the MBDCs must be the maximum duty applied to the switches controlling the input ports i.e., $d_{max} = {}_{i=1}^{N}[max.\, d_i] = d_N$. Further, it is important to note that for simultaneous power transfer to take place, switches S_1 to S_N (T_{D3}) and S_1 to S_{N+1} (for the others) must be implemented using reverse blocking switches. These reverse blocking switches, which have recently received attention in literature [88], prevent reverse conduction prevalent in the traditional switches.

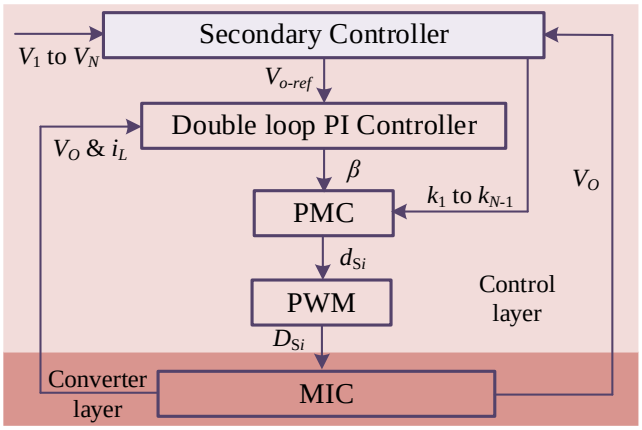


Figure 3. 21: Control structure of the proposed family of MBDCs.

Figure 3.21 presents the control structure of the MBDCs in T_D. The control layer consists of the secondary controller, the double loop PI controller, PMC and the PWM. The secondary controller sets the output voltage reference ($V_{o\text{-}ref}$), depending on the required operating mode of the MBDC. It is responsible for the proportion of power flow from the sources when operating in a simultaneous power flow mode. To do this, the secondary controller determines scaling factors k_1 to k_{N-1}, which are obtained by comparing the total power capacity (kw_T) of all the sources to the individual power capacities (kw_1 to kw_N) for sources (V_1 to V_N)

as in (3.3), or based on other parameters like the maximum power point tracking (MPPT). V_O and i_L are used to determine the control variable β, which is the time required to charge the inductor(s). The non-linear equations of the inductor currents and output capacitor voltages of the MBDCs presented in (3.21) are obtained and linearised. Taylor series expansion is used to obtain the inner current and output voltage-loop transfer functions, G_{id}, (3.22) and G_{vd}, (3.23). Further, the PI gains of the double loop PI controllers are heuristically selected based on G_{id}, (3.22) and G_{vd}, (3.23). The PMC based on the scaling instructions from the secondary controller determines $D_{1eff} - D_{Neff}$ and the respective duty cycles according to (3.24).

$$\left.\begin{array}{l} \left(\gamma = \sum_{i=1}^{N} V_i D_{ieff}\right), \quad \dfrac{di_L}{dt} = \left(\dfrac{\gamma + V_o}{L}\right)\beta - \dfrac{V_o}{L} \\ \left(\beta = \sum_{i=1}^{N} D_{ieff}\right), \quad \dfrac{dV_C}{dt} = \dfrac{i_L(1-\beta)}{C} - \dfrac{V_o}{RC} \end{array}\right\} \tag{3.21}$$

$$G_{id} = \frac{\left[s\gamma/L\right] + \left[\gamma/RLC\right]}{s\left(s + \dfrac{1}{RC}\right) + \dfrac{1}{LC}} \tag{3.22}$$

$$G_{vd} = \left[\gamma/LC\right] \Big/ \left[s\left(s + \frac{1}{RC}\right) + \frac{1}{LC}\right] \tag{3.23}$$

$$\left.\begin{array}{c} D_{1eff} = k_1\beta \\ \vdots \\ D_{N-1eff} = k_{N-1}\beta \\ D_{Neff} = \beta - \sum_{i=1}^{N-1} D_{ieff} \end{array}\right\} \quad , \quad \left.\begin{array}{c} d_1 = D_{1eff} \\ d_2 = D_{1eff} + D_{2eff} \\ \vdots \\ d_{N-1} = \sum_{i=2}^{N-1} D_{ieff} \\ d_N = \sum_{i=1}^{N} D_{ieff} \end{array}\right\} \tag{3.24}$$

3.5 Proposed MPC topology E (T_E)

3.5.1 Circuit description

T_E presented in Figure 3.22 are two multiport isolated dc-dc converters with bipolar symmetric outputs (MIBDC). These MPCs are synthesized by the integration of a traditional dual active bridge (DAB) or a phase-shifted full bridge (PS-FB) converter, which has been modified to use a secondary side center tapped

transformer to achieve bipolar symmetry on the outputs. The multiple inputs are achieved through pulsating voltage sources and a time multiplexed inductor charging scheme to control the output voltage and facilitate the inclusion of inputs of varying voltage levels. To reduce the control complexity of the DAB section in Figure 3.22 (a), the MPC in Figure 3.22 (b) is proposed by replacing the secondary active bridge with a diode H-bridge. Thus, it is like the conventional PS-FB converter with the introduction of the secondary side center tapping of the isolation transformer to facilitate bipolar outputs. Both topologies in Figure 3.22 have the same multi-input power processing mechanism, involving RBSs S_1 to S_N, one diode, capacitor, and inductor, respectively. Furthermore, the converters can provide three voltage levels, $\pm V_o/2$ and V_o, on the dc links. For the steady state continuous conduction mode (CCM) analysis in this dissertation, T_E in Figure 3.22 (b) will be analyzed for two inputs under individual and simultaneous power transfer modes, since the key principles of operation described are essentially applicable from PS-FB to the DAB based MIBDC.

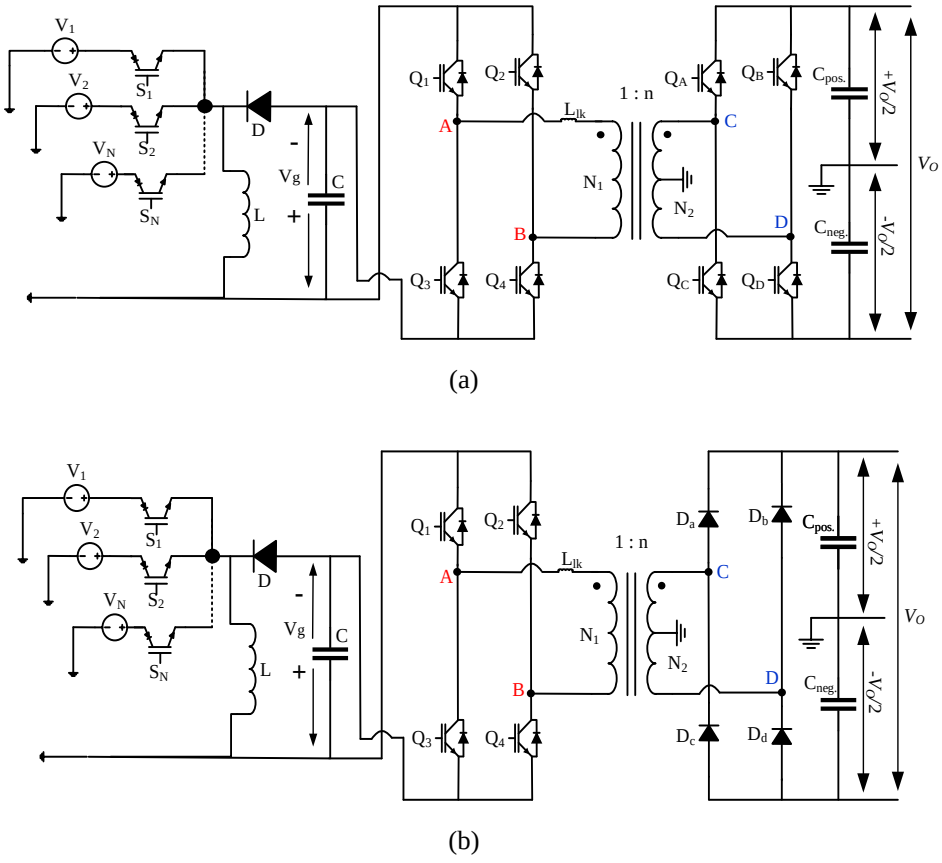


Figure 3. 22: T_E based on (a) dual-active-bridge and (b) full-bridge converters.

3.5.2 Steady state analysis

The independent power flow mode of T_E is characterized by power flow from any of the inputs (V_1 or V_2 for a two-input T_E) to the bipolar dc bus. The respective switch controlling each input source S_1 for V_1 or S_2 for V_2 is turned ON to charge the inductor, L, for a period of DT_S, where D is the duty cycle and T_S is the total switching period. During (1-D)T_S, the OFF time of the respective switch, diode D conducts in the direction as described in Figure 3.23 (b) to discharge L. Thus, the multiport section operates like a standard inverting buck-boost converter, and capacitor C has a voltage as described by (3.25). While the multiport section is in operation, the PS-FB section is also operating simultaneously as described in Figure 3.24. The isolation transformer section of T_E is operated in such a way that the active switches, Q_1 – Q_4 experience zero voltage switching (ZVS). Detailed explanation of this operation is presented in [95] and summarized here. The pulse signal for these switches is presented on the steady state waveform in Figure 3.24. The total switching period for Q_1 – Q_4 is divided into 10, (t_0 – t_{10}) to accommodate the phase shift ($\emptyset$) and the deadtime required to achieve ZVS. At t_0, Q_1 and Q_4 are ON with Q_1 turned ON at t_0 and Q_4 turned ON at t_8, in the previous cycle, both with ZVS. V_S remains 0, until t_1 when the current in the primary winding reverses to positive and V_S becomes equal to $2nV_g$ or V_o, and V_P is equal to V_g. Diodes D_a and D_d are forward biased to charge $C_{pos.}$ and $C_{neg.}$ up to $\pm V_o/2$, respectively, for the positive and negative poles and V_o across the full dc link thereby also supplying the load. At t_2, Q_4 is turned OFF, V_P and V_S become 0 and after a deadtime (t_3 – t_2), Q_3 is turned ON with ZVS at t_3. At t_4, Q_1 is turned OFF and after the deadtime (t_5 – t_4), Q_2 is turned ON with ZVS, V_P becomes -V_g and the primary current begins reversal to negative until t_6 when it is completely negative and V_S also becomes -V_o. Between t_3 and t_6, diodes D_a – D_d are reverse-biased, and $C_{neg.}$ and $C_{pos.}$ are discharged to supply the loads until t_6 when D_2 and D_3 are forward biased. At t_7, Q_3 is turned OFF and Q_4 is turned ON after the deadtime (t_8 – t_7) at t_8 with ZVS. Q_2 is turned OFF at t_9 and after a deadtime t_{10} – t_9, t_0 arrives when Q_1 turns ON again with ZVS, thus t_0 and t_{10} are essentially the same. Between t_6 and t_8, $C_{neg.}$ and $C_{pos.}$ are charging again then discharging to the load between t_8 and t_1 when diodes D_a – D_d are reverse-biased. Under steady state CCM operation, the relationship between the input voltage and the dc link is described by (3.26), where $\emptyset$ is the phase shift and n is the turn ratio (N_S/N_P) of the transformer.

$$V_g = \frac{V_{in} D}{1 - D} \tag{3.25}$$

$$V_o = \frac{V_{in}D}{1-D} 2\phi n = 2V_g \phi n \tag{3.26}$$

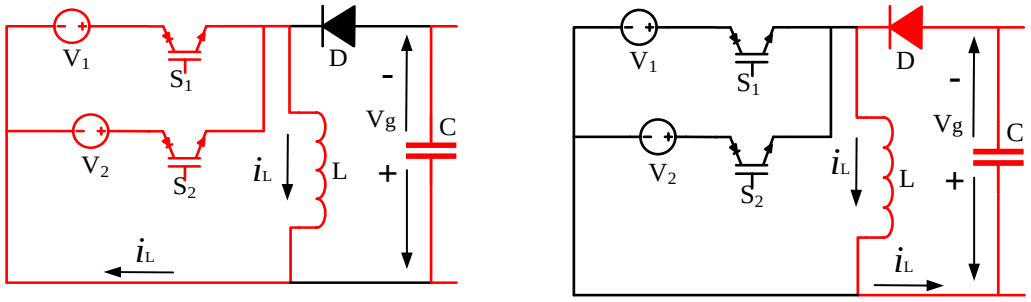


Figure 3. 23: Path of current flow in in the multiport section during (a) charging and (b) discharging of *L*, for simultaneous power flow with two inputs.

When a power transfer is required from more than one input to the dc link as illustrated in Figure 3.23 for two inputs, the converter switches to simultaneous power flow mode. The switches S_1 to S_N controlling all the sources are turned ON at the same time but turned OFF in the order of decreasing magnitude of the respective voltages. Thus, the charging of L is time multiplexed as illustrated in Figure 3.24, for the power delivery from two inputs simultaneously.

In steady state CCM as illustrated in Figure 3.24, the switching period is divided into two main parts, the charging and discharging times of L. The first part is further subdivided depending on the number of inputs of the MIBDC in simultaneous operation:two divisions (D_{1eff} and D_{2eff}) in this case while the second part remains fixed as $(1 - \sum_{i=1}^{N} D_{ieff})$, indicating the discharging time of L. When the switches are turned ON, current flows from the source with the highest potential first or V_1 in this case, so L is charged with a slope of V_1/L during D_{1eff}. When the time D_{1eff} is elapsed, V_2 takes over to continue charging L with a slope of V_2/L during D_{2eff}. This continues up to D_{Neff} with a slope of V_N/L for any number of inputs. At the end of the charging time, $\sum_{i=1}^{N} D_{ieff}$, L is discharged with a slope of $-V_g/L$. Also, while the multiport section is in operation, the PS-FB section is also operating simultaneously as described in Figure 3.24. By applying volt-second balance of the resulting steady state CCM waveform in Figure 3.24, capacitor C, has a voltage as defined by (3.27) and the input-output voltage is described by (3.28).

$$V_g = \left[\left(1-\sum_{i=1}^{N} D_{ieff}\right) \Big/ \left(1-\sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3.27}$$

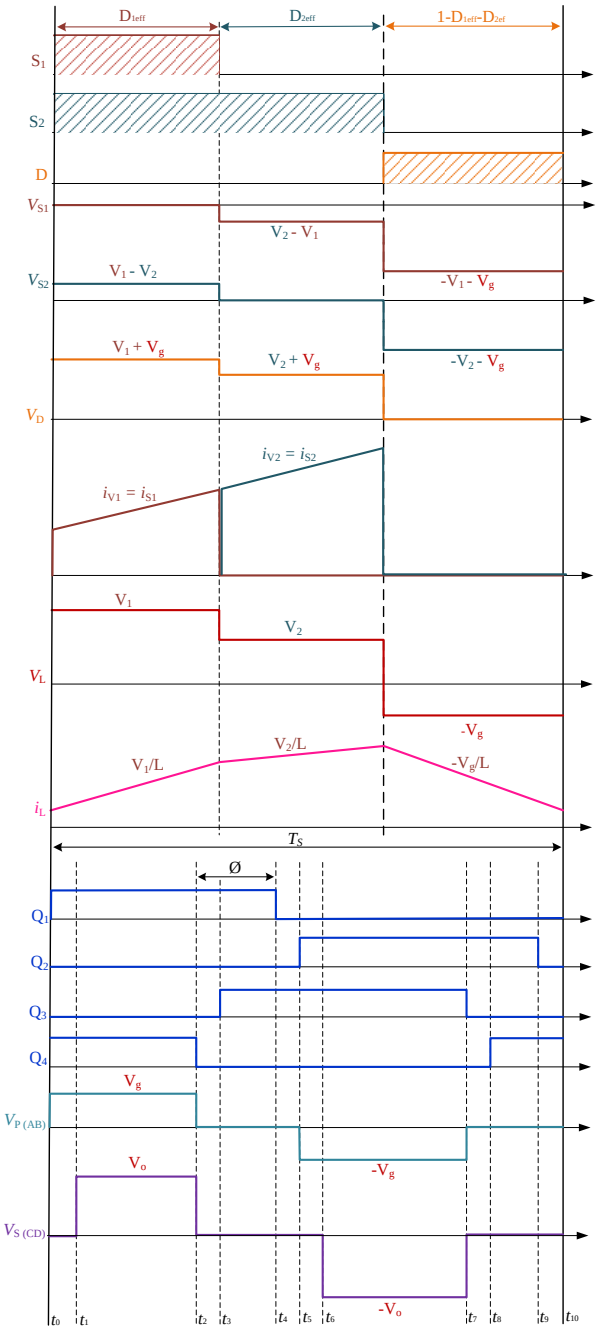


Figure 3. 24: Steady state key waveforms of the phase-shifted full-bridge based T_E.

$$V_o = \left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff}\right)\right] 2\phi n = 2V_g \phi n \qquad (3.28)$$

Just like in $T_A - T_D$, for an effective commutation of the switches in multi-input mode, some principles need to be respected to achieve simultaneous power transfer to the load. When the voltages are unequal, the magnitude of the sources is arbitrarily arranged in order of decreasing magnitudes such that $V_1 > V_2 > \cdots > V_N$, the duty cycles of the PWM signals of controlling the input sources, e. g S_1 and

S_2, must be such that $D_1 < D_2 < \cdots < D_N$, and vice versa, where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ..., $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. However, if the source voltages are equal such $V_1 = V_2 = \cdots = V_N$, duty cycles of the PWM signals must be in such a way that $D_1 = D_2 = \cdots = D_N$ to achieve an equal power delivery from the sources. If the required power delivery from the sources is unequal, $D_1, D_2, \ldots, D_N$ can be determined in order of increasing magnitude of the required power delivery from the respective sources.

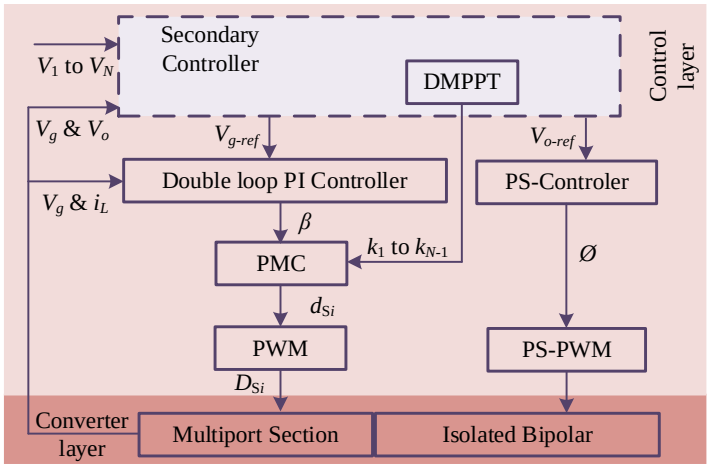


Figure 3. 25: Control structure of T_E.

Figure 3.25 shows the control structure of T_E. The control layer consists of the secondary controller (with the DMPPT controller), the double loop PI controller, the PMC, PS-controller and the respective PWM. The secondary controller sets the output voltage reference ($V_{g\text{-}ref}$) of the multiport section, depending on the required operating mode of T_E and the MPP of input sources. The MPP controller is also responsible for the proportion of power flow from the sources when operating in a simultaneous power flow mode. To do this, the MPP controller determines scaling factors k_1 to k_{N-1}, which are obtained by implementing an DMPPT algorithm for sources (V_1 to V_{N-1}). Figure 3.26 shows the flowchart of DMPPT, in which the classic perturb and observe (P&O) algorithm is implemented. The output of the DMPPT P&O algorithm is k_1 to k_{N-1}. V_O and i_L are used to determine the control variable α, which is the time required to charge the inductor(s). The PI gains of the double loop PI controllers are selected heuristically. The PMC based on the scaling instructions (k_1 to k_{N-1}.) from the DMPPT controller determines $D_{1eff} - D_{Neff}$ and the respective duty cycles according to (3.29). Further, the PS-controller provides the required PS ($\emptyset$) needed to keep the output voltage of the isolated bipolar section constant based on the target output voltage ($V_{o\text{-}ref}$).

$$\left.\begin{aligned} D_{1eff} &= k_1\alpha \\ &\vdots \\ D_{N-1eff} &= k_{N-1}\alpha \\ D_{Neff} &= \alpha - \sum_{i=1}^{N-1} D_{ieff} \end{aligned}\right\} \quad , \quad \left.\begin{aligned} d_1 &= D_{1eff} \\ d_2 &= D_{1eff} + D_{2eff} \\ &\vdots \\ d_{N-1} &= \sum_{i=2}^{N-1} D_{ieff} \\ d_N &= \sum_{i=1}^{N} D_{ieff} \end{aligned}\right\} \tag{3.29}$$

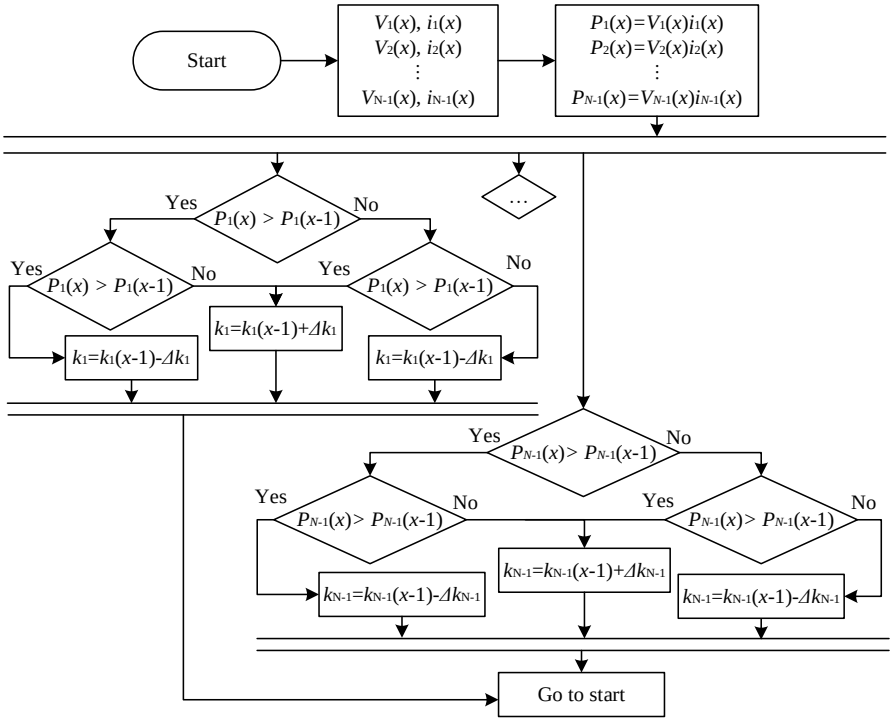


Figure 3. 26: Flowchart of DMPPT controller of T_E.

3.6 Grid integration

This section presents the attempts to verify the integration of energy sources and storages to both dc and ac grids in this dissertation. Firstly, the reliability of bipolar dc transmission to critical unipolar dc distribution systems is studied. Further, previously proposed MLIs are used to verify the integration of energy resources from unipolar and bipolar MPCs to ac grids in subsections 3.6.1 to 3.6.3, respectively.

3.6.1 Bipolar DC to Critical Unipolar DC

One key advantage of bipolar dc power systems over the unipolar counterparts is the increased reliability of dc power transmission to critical distribution units. This is demonstrated by the ability to continue to supply power to the critical unit in the

event of a failure or open circuit fault in any of the lines of the bipolar system. Figure 3.27 presents the schematic of a bipolar to unipolar dc-dc converter required to achieve this. This bipolar to unipolar dc-dc converter is essentially a cascade of two synchronous buck converters and its operation is similarly so. The switching pattern of the converter is presented in Table 3.3 for the healthy state and fault states. This converter configuration can be used for any of the MPCs with bipolar symmetric outputs in T_D and T_E to achieve reliable dc power transmission. The input-output voltage relationship of the converter is described by (3.30), which is basically the same as a traditional buck converter's. The input voltage (V_{in}) in this case depends on the state of the bipolar dc, under healthy state and failure in the neutral line, V_{in} is equivalent to V_o while it is equivalent to $V_o/2$ in the other two fault states.

$$V_{dc} = V_{in} D \tag{3.30}$$

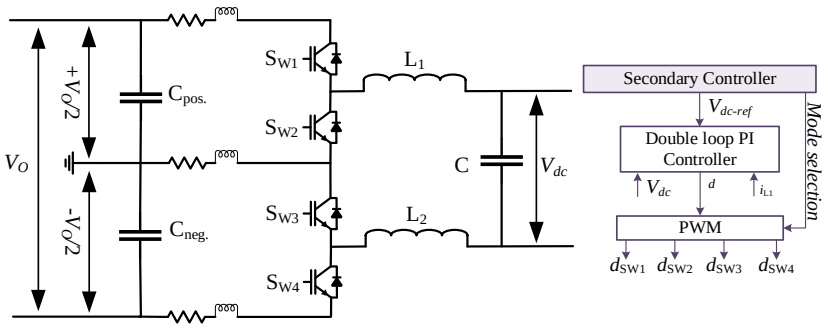


Figure 3. 27: Schematic of bipolar to unipolar dc-dc converter for critical loads.

Table 3. 3: Conduction of devices in the bipolar to unipolar dc-dc converter for critical power transmission and distribution.

State	T_1	T_2
Healthy state	S_{W1} S_{W4}	D_{W2} D_{W3}
Failure in positive line	S_{W4}	D_{W2} D_{W3}
Failure in negative line	S_{W1}	D_{W2} D_{W3}
Failure in neutral line	S_{W1} S_{W4}	D_{W2} D_{W3}

3.6.2 Unipolar MPC to AC

Figure 3.28 presents the integrated multiport dc and multilevel converter configuration for integrating multiple sources and converting unipolar dc to ac. This configuration consists of a modification to T_A so as to achieve a unidirectional three-input MPC highlighted in blue, the dc bus output highlighted in purple and the MLI (previously proposed in [79]) sections, alongside the ac output highlighted

in green. This configuration allows for easy integration of different energy sources with varying voltage levels to dc and ac links independently or simultaneously. The modified T_A section consists of one inductor, two diodes and N+1 number of RBSs, where N is the number of input ports to the modified T_A. It can operate in up to seven different unidirectional modes of which four are simultaneous power flow from two or more sources (V_1 & V_2, V_2 & V_3, V_1 & V_3, V_1, V_2 & V_3 respectively). The other three modes represent independent power flow from the three sources (V_1 – V_3) to the dc link. The independent and simultaneous power flow, from the sources of the modified T_A when its operation and steady state CCM waveforms in Figures 3.29 and 3.30 are examined closely, is the same as that of T_A. Therefore, the equations (3.1 and 3.2) describing the relationship between the input and output voltage of T_A applies to the modified T_A as well for independent and simultaneous power flow, respectively.

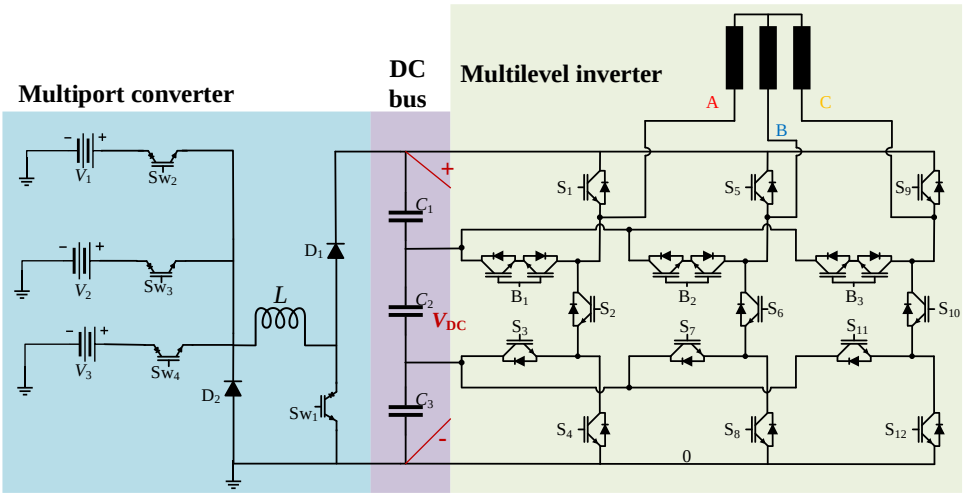


Figure 3. 28: Schematic of the integrated multiport converters system.

In Figure 3.28, the MLI topology is highlighted in green, consisting of twelve unidirectional switches (S_1-S_{12}) and three bidirectional switches (B_1-B_3). To simplify the gate-drive circuits, the common-emitter structure is adopted to configure the bidirectional switches. The dc-link of the MLI topology is configured using three dc-link capacitors. The inverter switches are controlled to produce four unipolar voltage levels of 0, E/3, 2E/3, and E in the pole voltages V_{A0}, V_{B0}, and V_{C0}. Seven-level bipolar voltages can be generated in the line voltages V_{AB}, V_{BC}, and V_{CA} by subtracting the adjacent pole voltages. For example, V_{AB} is synthesized by subtracting V_{B0} from V_{A0}, producing a seven-level voltage of -E, -2E/3, -E/3, 0, E/3, 2E/3, and E. The operating modes and modulation strategies of the MLI topology is sufficiently addressed in [79].

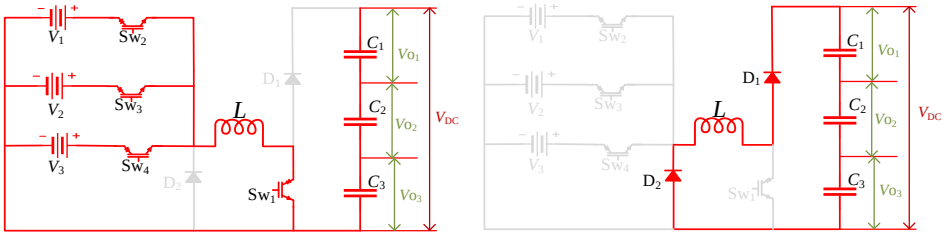


Figure 3. 29: Path of current flow of the modified T_A in steady state CCM under simultaneous power transfer for inductor charging and discharging.

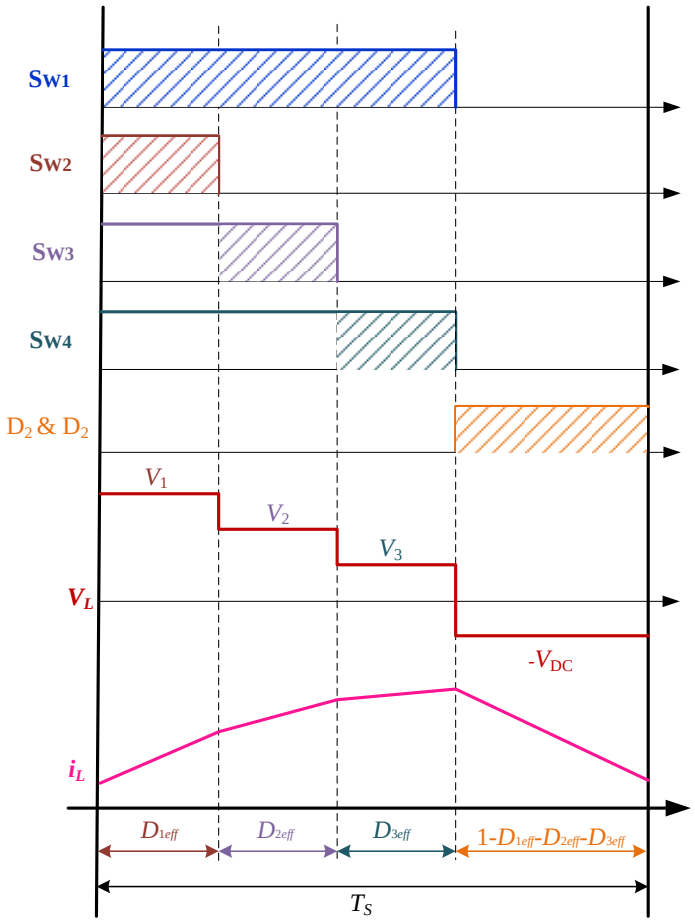


Figure 3. 30: Steady state CCM waveforms of the modified T_A under simultaneous power transfer from the three sources to the dc link.

The capacitor voltage imbalance is common in four-level inverter topologies, where three capacitors are connected in series to divide the unipolar dc-link voltage into three equal parts as shown in Figure 3.28. A generalized mechanism for investigating the capacitor voltage imbalance in the four-level topologies was provided in [85]. The three capacitor currents I_{C1}, I_{C2}, and I_{C3} in the dc link of the proposed configuration are not equal, causing a voltage imbalance. The current of the middle capacitor I_{C2} is larger than the currents of other capacitors I_{C1}, and I_{C3},

which are equal. Consequently, the C_1 and C_3 discharge less energy than C_2. Specifically, C_2 discharges faster to zero while the full dc-link voltage V_{dc} is equally shared between C_1 and C_3. Since the capacitor voltages are not balanced because of the over-discharge of C_2. Therefore, by regulating the voltage of C_2, the other capacitors C_1 and C_3 can be balanced. Subsequently, the three capacitor voltages V_{C1}, V_{C2}, and $V_{C3,}$ are equal when V_{C2} is regulated at $V_{dc}/3$. To this end, a control-based voltage balance scheme is used in [79], referred to as the variable-carrier scheme (VCS). The VCS method consists of the modulation signal generation block, carrier signal block, and a PI controller. These three parts are used to generate modulation signals with a third-harmonic injection variable and fixed carrier signals, which are used to regulate C_2 voltage to $V_{dc}/3$.

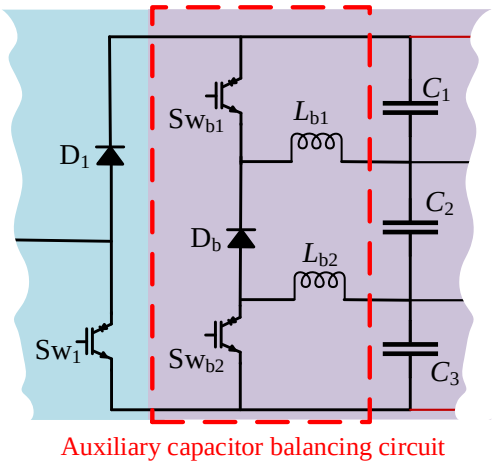


Figure 3. 31: Schematic of the auxiliary circuit for capacitor balancing.

However, a simpler solution was implemented in this dissertation with the use of an auxiliary capacitor balancing circuitry to keep the voltage of the three capacitors balanced as shown in Figure 3.31. The circuit based balancing technique consist of using two inductors (L_{b1}, L_{b2}) and three switches (one diode, D_b and two MOSFETs, S_{Wb1}, S_{Wb2}). S_{Wb1} and S_{Wb2} are controlled using the same pulse signal, when they are turned ON, the two inductors charged and then discharged through D_b. By this action, the voltage of C_2 is prevented from degrading to 0. A proportional controller selected heuristically and used to determine the duty cycle of S_{Wb1} and S_{Wb2} so that the voltage of C_2 is regulated to $V_{dc}/3$ while both C_1 and C_3 are naturally balanced at $V_{dc}/3$ too under these conditions.

3.6.3 Bipolar MPC to AC

Furthermore, T_{D4} was integrated with the MLI proposed in [96] as shown in Figure 3.32. The inputs to the MLI were replaced by the bipolar outputs of the MBDC to create a multi-input MLI. The MLI switches were operated with low frequency modulation as discussed in [96] with three phase *RL* loads connected in wye configuration at the outputs of the inverter. Thus, the applicability of the bipolar MPCs for MLIs and other applications that could potentially cause unbalanced loads at the poles of the bipolar dc bus could be validated.

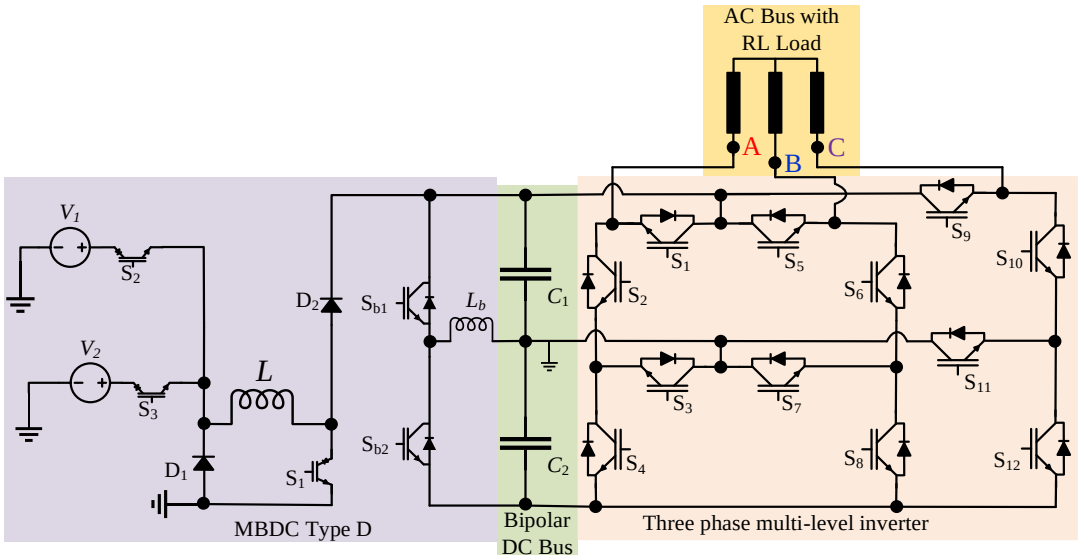


Figure 3. 32: Integrating T_{D4} with the multilevel inverter proposed in [96].

3.7 Voltage transformation factor (V_{TR})

The new MPCs in this dissertation can operate in a parallel configuration with multiple voltages involved, thus a novel voltage gain is proposed in this section. The voltage gain of the MPCs is a little different from the conventional single input converters, since they can operate in a parallel configuration with multiple voltages involved [93]. This is because the input voltages are introduced with respect to their effective duty cycles (D_{ieff}). During simultaneous power transfer from the sources to the dc bus, the effect of different input voltages on the output voltage does not solely depend on the duty cycles but also on the effective duty cycle of the other input sources. Therefore, the gain relationship of MPCs, capable of simultaneous power transfer from the inputs, is best defined as a voltage transformation factor (V_{TR}). This is a relationship between the output voltage and its input voltages considering the duty of the switches controlling each respective input port.

3.7.1 V_{TR} for T_A

For T_A, V_{TR} is defined by (3.31). The obtainable values of V_{TR} are 10.0 and 1.11 if the converter operates at 90% and 10% effective duties. Although V_{TR} for T_A is similar to the gain of a conventional boost converter, it is vital to note that the input voltages, being compared to the output voltage, is not the full input voltages, but the sum of the input voltages scaled by ON time of their respective switches ($\sum_{i=1}^{N} V_i D_{ieff}$).

$$V_{TR} = V_o \Big/ \left[\sum_{i=1}^{N} D_{(i)eff} V_i \right] = 1 \Big/ \left[1 - \sum_{i=1}^{N} D_{(i)eff} \right] \tag{3.31}$$

3.7.2 V_{TR} for T_B

For T_B, V_{TR} is defined by (3.32 – 3.34), for gain due to cluster 1 and 2 supplying the dc link and the interaction between cluster 1 and 2 respectively. Although V_{TR} for T_B is like the gain of a conventional boost converter, it is vital to note that the input voltages, compared to the output voltage, is the sum of the input voltages scaled by ON time of their respective switches ($\sum_{i=1}^{N} V_i D_{ieff}$).

$$V_{TR-1} = V_o \Big/ \left[\sum_{i=1}^{j} D_{(i)eff} V_i \right] = 1 \Big/ \left[1 - \sum_{i=1}^{j} D_{(i)eff} \right] \tag{3.32}$$

$$V_{TR-2} = V_o \Big/ \left[\sum_{i=j+1}^{N} D_{(i)eff} V_i \right] = 1 \Big/ \left[1 - \sum_{i=j+1}^{N} D_{(i)eff} \right] \tag{3.33}$$

$$V_{TR} = V_3 or V_4 \Big/ \sum_{i=1}^{j} \left(D_{(i)eff} V_i \right) = 1 \Big/ 1 - \sum_{i=1}^{j} D_{(i)eff} \tag{3.34}$$

3.7.3 V_{TR} for T_C

V_{TR} for T_C is derived from the output voltage equation and is expressed as (3.35). It's V_{TR} can be up to 10n at a duty cycle ($\sum_{i=1}^{N} D_{ieff}$) of 90%. This points to the potential for high gain, depending on the turns ratio (n) of the coupled inductor.

$$V_{TR} = \frac{V_{dc}}{\sum_{i=1}^{N} V_i D_{ieff}} = \frac{1}{1 - \sum_{i=1}^{N} D_{ieff}} n \tag{3.35}$$

3.7.4 V_{TR} for T_D

The V_{TR} for the MBDCs in T_D is expressed in (3.36). Using this equation, the maximum V_{TR} obtainable when $\sum_{i=1}^{N} D_{ieff} = 0.9$, are 80, 40, and 20 for T_{D3}, T_{D2}

and T_{D5}, and T_{D1} and T_{D4}, respectively. Further, when $\sum_{i=1}^{N} D_{ieff}$ is at the minimum of 0.1, the resulting gains V_{TR} are about 8.89, 4.44 and 2.22 for T_{D3}, T_{D2} and T_{D5}, and T_{D1} and T_{D4}, respectively. At $V_{TR} > 2$, T_D is operating in the boost mode, and vice versa for the buck mode, this proves the high gain capabilities of the MBDCs in T_D.

$$V_{TR} = \frac{V_o}{\sum_{i=1}^{N} V_i D_{ieff}} = \underbrace{\frac{2}{1-\sum_{i=1}^{N} D_{ieff}}}_{T_{D1}\&T_{D4}} = \underbrace{\frac{4}{1-\sum_{i=1}^{N} D_{ieff}}}_{T_{D2}\&T_{D5}} = \underbrace{\frac{8}{1-\sum_{i=1}^{N} D_{ieff}}}_{T_{D3}} \tag{3.36}$$

3.7.5 V_{TR} for T_E

For T_E, V_{TR} is expressed as (3.37). A high gain of up to $20\emptyset n$ can be achieved at an effective duty cycle (D_{ieff}) of 90%. Thus, the phase shift, $\emptyset$, and turns ratio, n, can be used to further increase the converter gain if higher gain is required.

$$V_{TR} = V_o \Big/ \left(\sum_{i=1}^{N} V_i D_{ieff} \right) = (2\phi n) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff} \right) \tag{3.37}$$

Chapter 4

4 Results and discussions

This chapter presents the results from numerical verification in MATLAB/Simulink and experimental validation of the new MPC topologies proposed in this dissertation. The experimental validation was carried out both on an in-house high-fidelity hardware-in-the-loop (HIL) platform and a reconfigurable experimental test bench. Some results are selected based on results presented in papers I to VIII and discussed in the following sections but more details of the results can be found in respective papers. Furthermore, a summarized comparison of the proposed MPC topologies and other existing MPC topologies in literature are presented in this dissertation to highlight the novel features of the proposed MPCs.

4.1 In-house test setup

Figure 4.1 shows the experimental setup for validating the proposed MPC topologies, highlighting the HIL and reconfigurable experimental test bench respectively. The in-house real-time HIL validation platform consists of OPAL-RT's OP5700 running a 64bit virtex-7 FPGA and is controlled from Imperix's B-box 3.0, a kintex grade FPGA controller. A host PC is also used to run the HIL software, and the oscilloscope is used for monitoring and capturing experimental results. The proposed MPC topologies are experimentally validated on reconfigurable hardware rig, consisting of the high and low switching frequency reconfigurable switch banks, passive component (inductors, capacitors and single-phase transformers) banks, Imperix B-box 3.0 controller, oscilloscope, dc power supplies and loads. The high frequency switch bank is made up of the PEB-SIC 8024 configurable switch legs from Imperix, which is made from CREE's C2M0080120D SiC power MOSFETs. The low frequency switch bank consists of twenty-four IGBT modules (SEMIKRON, SKM300GA12E4) with their gate-drivers (SEMIKRON, SKHI 10/12 R). The experimental test bench more specifically also includes programmable DC voltage sources (Chroma, 62024P-100-50), low-power DC source (Rohde & Schwarz, HMP4040) for the gate drive

circuits of the low frequency switch bank, dSPACE MicroLabBox controller, digital oscilloscope (Yokogawa, DL850EV), current and voltage probes.

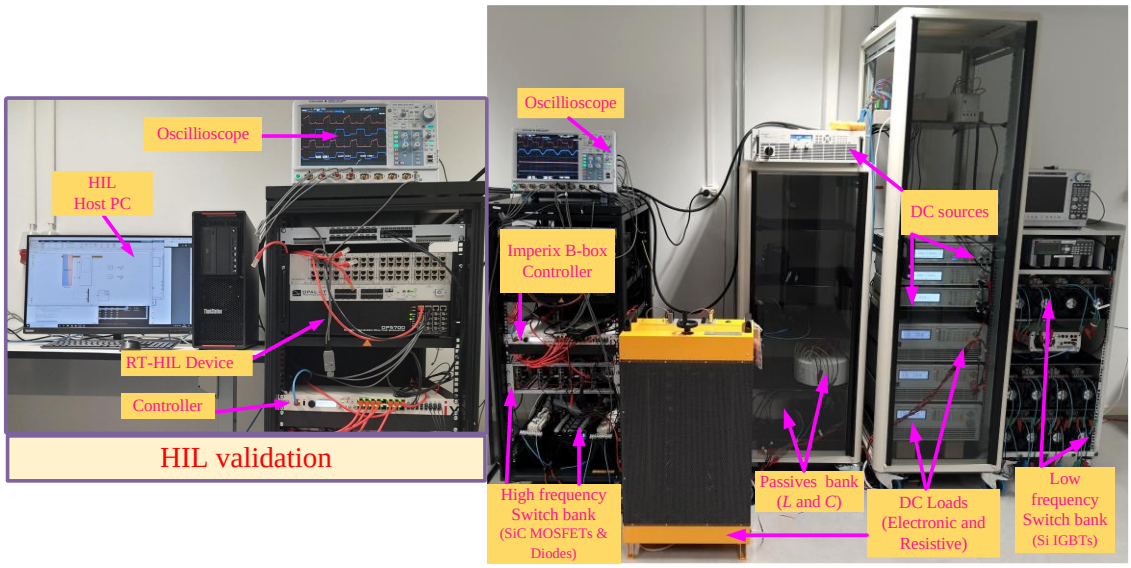


Figure 4. 1: The in-house experimental and validation setups.

4.2 Key results for T_A

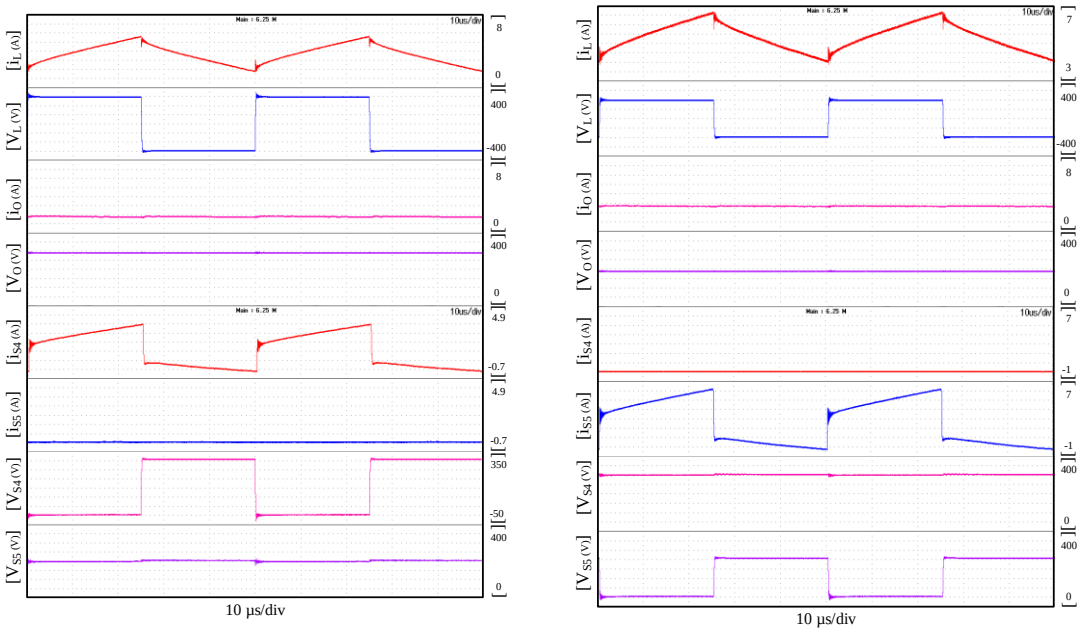
T_A is numerically verified and experimentally validated in the different operation modes. Since operations in modes A-D are conventional in buck-boost converters and sufficiently addressed in literature, the results presented are mostly for mode E, demonstrating the simultaneous flow of energy from two sources. Table 4.1 presents the selected components and parameters used in the validation of T_A.

Table 4. 1: Parameters used in the validation of T_A.

Parameter	Value
Switching frequency (F_{SW})	20 – 150 kHz
Source 1, V_1	300 V
Source 2, V_2	200 V
Output power (P_O)	5 kW
Output voltage (V_O)	200 – 400 V
L, Hammond – 195E50	2.5 mH/50A/8mΩ
C, KEMET – ALS70A472NF500	4.7 mF/500V/59mΩ
S_{1a} – S_{5b}, CREE – C2M0080120D	1200V/36A/80mΩ

Figure 4.2 presents the results of open loop validations of T_A in modes A and B, respectively. In both cases, the load is 500 W with V_1=300V, V_2=200 V while the respective duty cycle of the switch is 0.5, i.e. D_1=0.5 D_2=0, in mode A and D_1=0 while D_2=0.5 in mode B. In Figure 4.2 (a), Δi_L is about 4 A with an average i_L of

3.8 A, and i_O is about 1.8 A while the output voltage, V_O is about 290 V, which is a 10 V drop from the calculated of 300 V. In Figure 4.2 (b), the inductor ripple, ΔI_L, is about 3 A with a higher average i_L than in Figure 4.2 (a) at about of 5.5 A, since i_O is also higher in Figure 4.2 (b) at about 2.7 A due to the lower output voltage, V_O, of about 191 V, which is a 9 V drop from the calculated of 200 V. The voltages (V_{S4} & V_{S5}) and currents (i_{S4} & i_{S5}) of the switches controlling the input sources (S_4 & S_5) are also presented in Figure 4.2.



(a) (b)

Figure 4. 2: Experimental results with V_1=300 V, V_2=200 V, under 500W load where V_L & i_L: inductor voltage & current, i_O & V_O: output current & voltage, and i_{S4}, i_{S5}, V_{S4} & V_{S5}: S_4 & S_5 current & voltage, for (a) Mode A, D_1=50% and D_2=0 and (b) Mode B, D_1=0 and D_2=50%.

The experimental tests on the SiC switch bank were performed to validate the HIL results in detailed in paper I and II. Figure 4.3 presents the results of experimental validation in open-loop operations. In Figure 4.3 (a), V_1 = 300 V, V_2 = 200 V, D_1 =30% and D_2 = 60% while V_O is about 360 V, or about 9 V and 15 V drop from the respective HIL and calculated results. Δi_L is about 4 A, like the HIL result, but i_L is about 7.4 A, or an increase of about 2 A from the HIL result and i_O is about 2.7 A. In Figures 4.3 (b & c), the source voltages are V_1 = V_2 = 200 V, but the unequal duty cycles are considered in Figure 4.3 (b) while equal ones are shown in Figure 4.3 (c). In both cases, V_O is about 286 V, which is about 10 V and 14 V drop from the respective HIL and calculated results. Δi_L is about 3.4 A, and i_L is about 5.9 A with i_O of about 2 A. The expected differences are within acceptable

limits and are due to the non-idealities (e.g. parasitic impedances) in the experimental setup that was unaccounted for in the simulation.

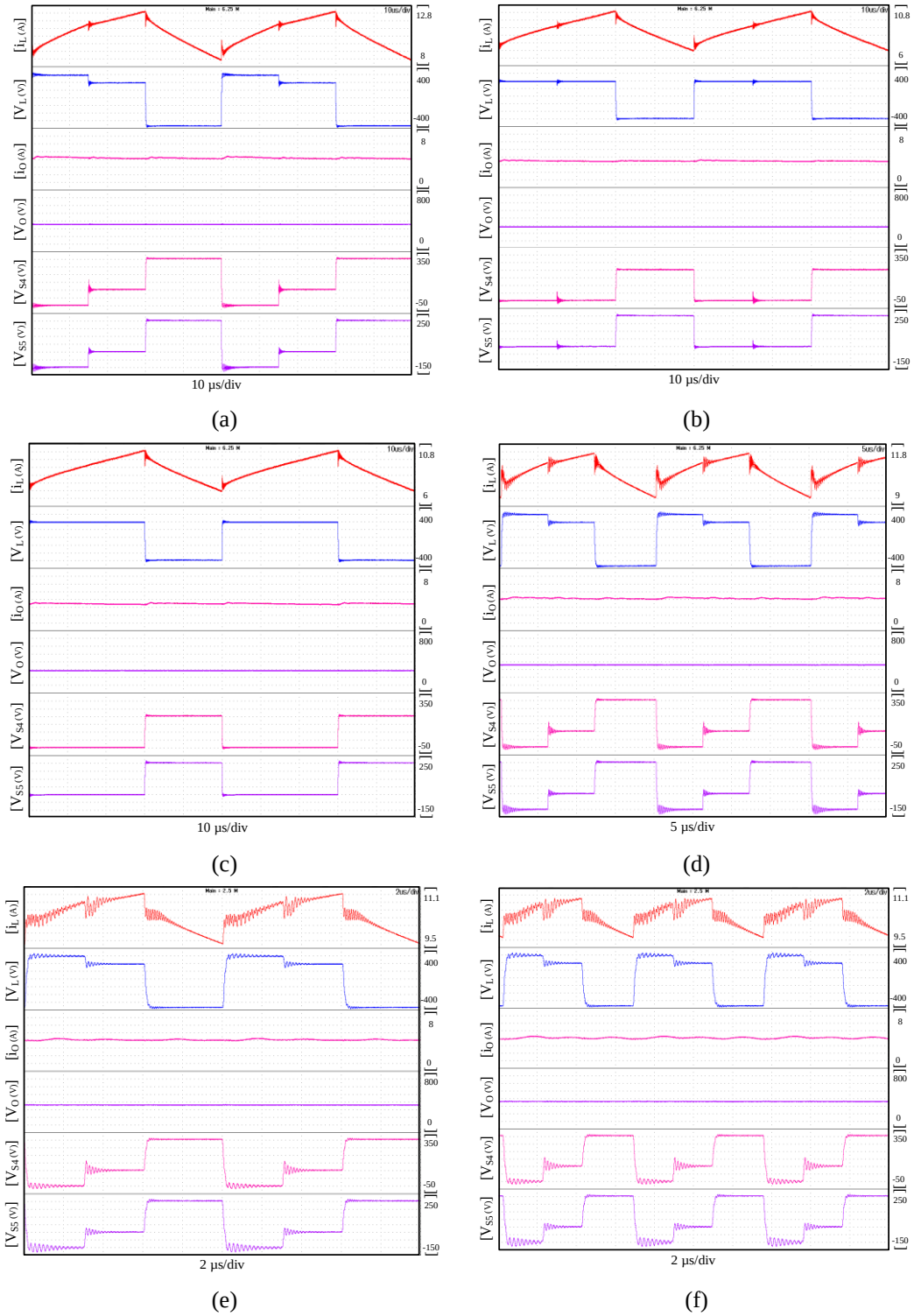


Figure 4. 3: Mode E experimental results where V_L & i_L: inductor voltage & current, i_O & V_O: output current & voltage, and V_{S4} & V_{S5}: voltage of S_4 & S_5, for (a) V_1=300 V, V_2=200 V, D_1=30%, D_2=60% and load=1.5 kW, (b) V_1=V_2=200 V, D_1=30%, D_2=60%, and load=1 kW, (c) V_1=V_2=200 V, D_1=D_2=60%, and load=1 kW. F_{SW}= 20kHz in (a)–(c) while in (d)–(f) V_1=300 V, V_2=200 V, D_1=30%, D_2=60% and load=1 kW, but F_{SW}= 50kHz, 100kHz & 150kHz.

To demonstrate the effect of high F_{SW} on the proposed MPC, it was operated using the same parameters in Figure 4.3 (a), but F_{SW} is changed to 50 kHz, 100 kHz and 150 kHz and the results are presented in Figures 4.3 (d-f), respectively. It is observed that as F_{SW} increases, Δi_L reduces from about 4 A at 20 kHz to about 1.7 A at 150 kHz. Similarly, i_L reduces from about 7.4 A to about 7.2 A. Further, as F_{SW} increases, V_O increases from about 360 V at 20 kHz to about 367 V at 150 kHz. Thus at 150 kHz, V_O is only about 2 V and 8 V less than the V_O obtained in the HIL and calculation.

Figure 4.4 shows V_{TR} obtained from analytical calculations, HIL simulations and experimental tests for different combinations of duty cycles D_1 and D_2, where F_{SW} is 20 kHz, V_1= 50 V and V_2 = 25 V. V_1 and V_2 are chosen such that at 90% duty cycle, the limits of the test equipment are not violated. D_1 is kept constant at 30% duty while D_2 is varied. It is observed that when $D_2 < D_1$, V_{TR} remains constant. This is because $V_1 > V_2$, thus D_{2eff} = 0. The effect of V_2 appears only when $D_2 > D_1$. Similarly, when D_2 is kept constant at 60%, V_{TR} remains constant when $D_1 < D_2$ despite the magnitude of V_1 is greater than V_2. The reason is that D_{1eff} keeps increasing as D_1 is increased while D_{2eff} reduces proportionately as D_{1eff} increases, thus keeping $\sum_{i=1}^{N} D_{(i)eff} V_i$ constant. This changes when $D_1 > D_2$ and at this point, D_{2eff} = 0. Figure 4.4 shows a good agreement among the results from analytical calculation, HIL simulations and experimental tests despite the expected losses. Further, there is a multi-fold increase in V_{TR} with the change in duty cycle from 80% to 90%.

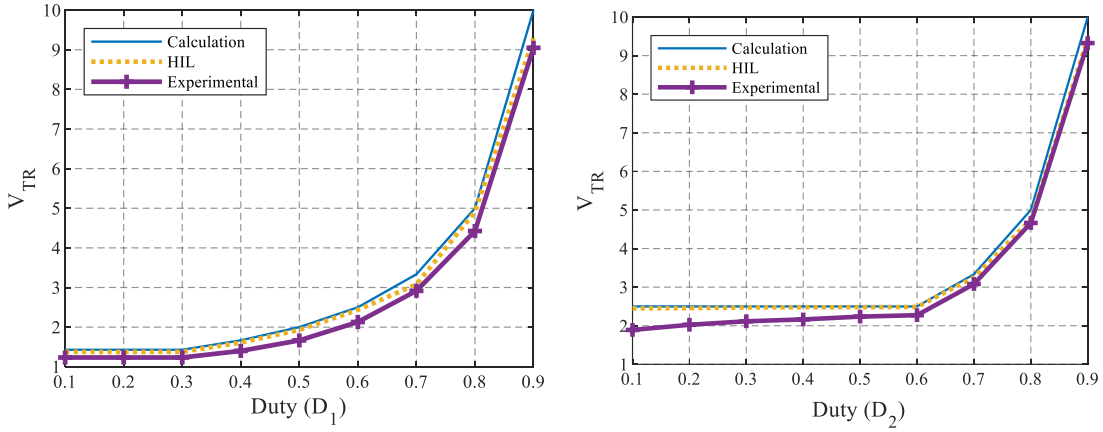


Figure 4. 4: V_{TR} comparison in mode E, with F_{SW}=20kHz, V_1=50 V, V_2=25 V, D_1=0.3 and D_2=0.6.

Figure 4.5 shows the HIL results for closed loop performance of T_A under perturbations in the input voltages and load current. HIL results of T_A under closed

loop operations to prove its robust operation despite of using a SISO controller. The double-loop PI controller for T_A is designed based on the Ziegler-Nichols tuning method as discussed earlier in Chapter 3. The step response of the output voltage is also presented, where the time constant is about 20 ms. The rise time is 30 ms and the settling time is about 50 ms with a steady state error of about 1 V. T_A's controller can reject the disturbances in the input voltages from 300 V to 225 V and 200 V to 150 V, respectively, for V_1 and V_2. The load current is also stepped from 6 A to 12 A, and vice-versa. The controller can maintain the output voltage in less than 15 ms while the dip remains less than 4 V under the disturbances. These results indicate how a simple controller is sufficient to control the output voltage.

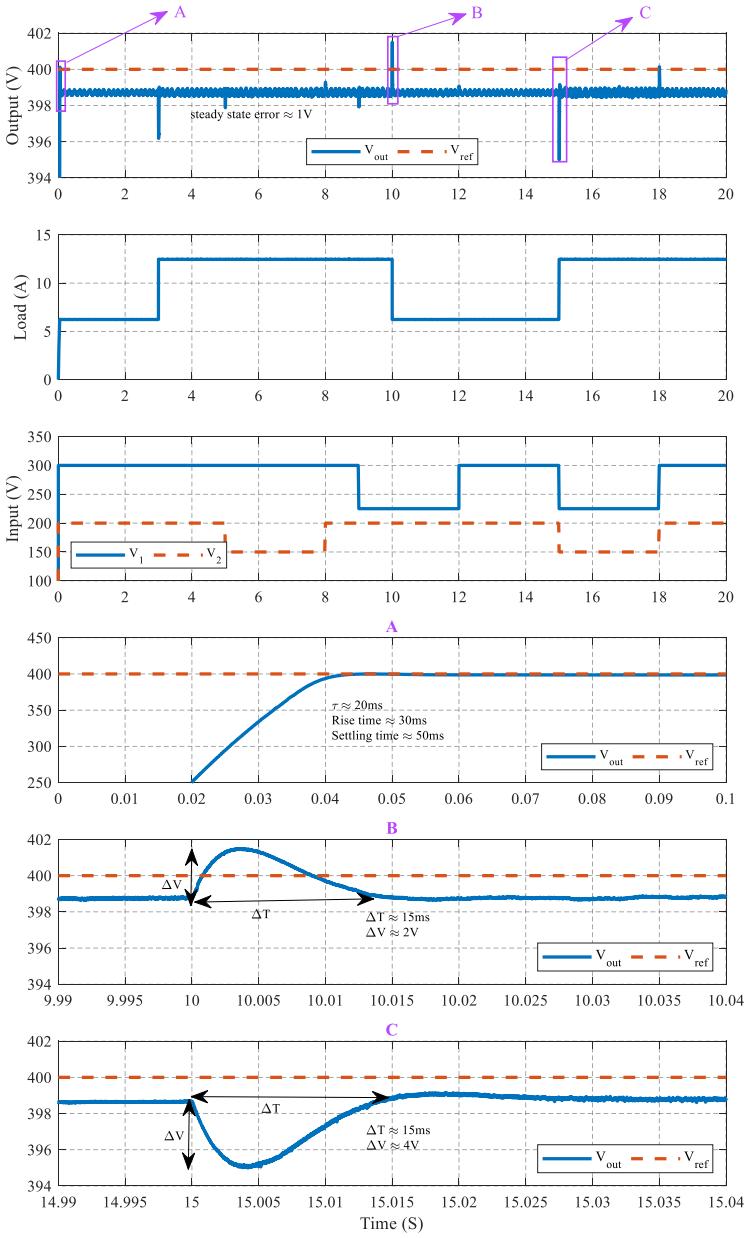


Figure 4. 5: Closed loop performance under voltage and current perturbations.

The efficiency of T_A in the experimental setup, is presented in Figure 4.6, showing the effect of varying F_{SW} on efficiency at varying load conditions. Figure 4.6 (a) is conducted when V_1=300 V, V_2=200 V with D_1=0.3 and D_2=0.6 thereby yielding an output voltage of about 360 V. In Figure 4.6 (b), when V_1=V_2=200 V with D_1=D_2=0.6, the output voltage is about 290 V. It is observed that as the load is increased, efficiency also increases. The converter prototype was designed for operation at 5 kW, but the available in-house load is only 2.5 kW. A significant improvement in the efficiency is observed on increase in F_{SW}, highlighting the benefits derived from using WBG devices as it has up to 96% efficiency with F_{SW} of 150 kHz at 2.5 kW load in Figure 4.6 (a) and up to 95% efficiency in Figure 4.6 (b). The power losses (P_L) in MPC can be estimated using (4.1), consisting of the inductor winding (P_{indW}) and core (P_{indC}) losses [97], capacitor losses (P_{cap}), MOSFET switching and conduction losses [98], where T_S is the switching period, R_{ESRL} is the inductor's equivalent series resistance (ESR), $\hat{i}_L$ is the inductor average current, Δi_L is the inductor ripple current, $K, \beta \,\&\, \alpha$ are Steinmetz parameters, R_{ESRC} is the capacitor ESR, V_{DS} is the MOSFET drain to source voltage, i_{DS} is the MOSFET drain to source current, t_{on} & t_{off} is the MOSFET on and off time, R_{DSon} is the MOSFET on state resistance and D is its respective duty cycle.

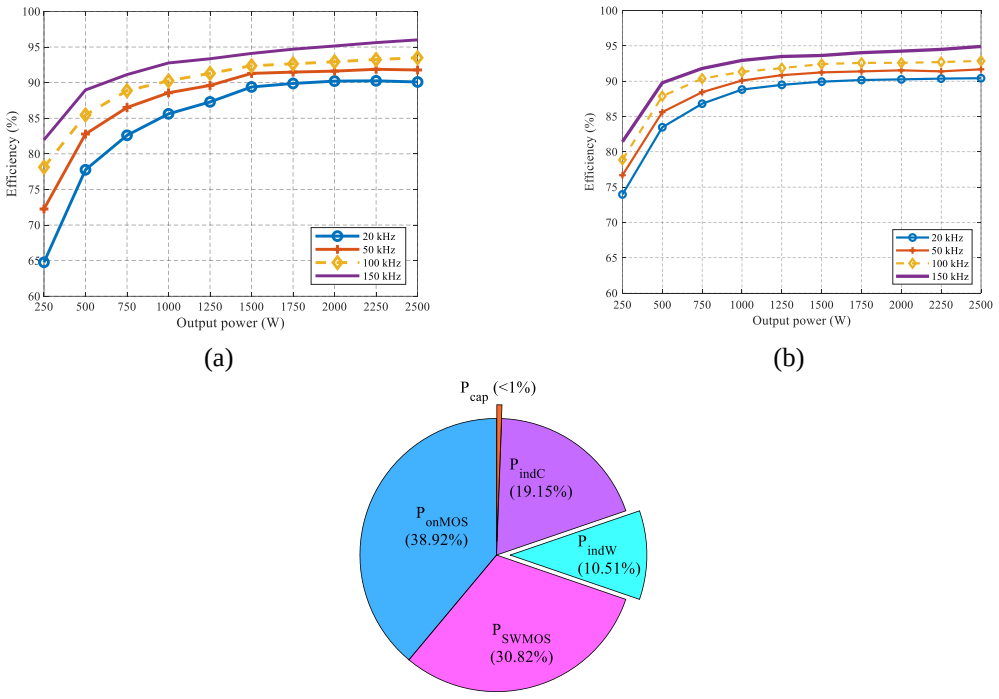


Figure 4. 6: Experimental efficiency analysis of the MIC under varying F_{SW} for (a) D_1 = 0.3, D_2 = 0.6, V_1 = 300 V & V_2 = 200 V, (b) D_1 = D_2 = 0.6 & V_1 = V_2 = 200 V and (c) theoretically obtained loss distribution at 2.5 kW load and F_{SW}=150 kHz.

$$P_L \approx \left\{ \underbrace{\frac{1}{T_S}\int_0^{T_S} R_{ESRL}\left(i_L{}^2 + \frac{\Delta i_L{}^2}{12}\right)}_{P_{indW}} + \underbrace{K\Delta i_L^{\beta} F_{SW}^{\alpha}}_{P_{indC}} + \underbrace{R_{ESRC}\left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}_{P_{cap}} + \underbrace{\frac{1}{2}V_{DS} i_{DS} F_{SW}\left(t_{on}+t_{off}\right)}_{P_{SWMOS}} + \underbrace{R_{DSon} i_{DS}^2 D}_{P_{onMOS}} \right\} \quad (4.1)$$

Figure 4.6 shows that increasing F_{SW} reduces Δi_L, lowering the losses in inductor and capacitor based on (4.1) thus increasing efficiency. However, at a point, the effect of Δi_L is less obvious although Δi_L reduces with the increase in F_{SW}, the switching losses and conduction losses at some point overturn the gains of reduced Δi_L. Thus, it is necessary to find an optimal F_{SW} so that it does not negatively affect the MPC's efficiency. Further, the loss distribution presented in Figure 4.6 (c) is obtained by (4.1). It shows an average break-down of the losses in the different components of the proposed MPC under 2.5 kW load at 150 kHz switching frequency. The losses in the capacitor (P_{cap}) account for less than 1% of the total losses under this condition. The losses in the inductor accounts for almost 30% of the total losses of which about 10% is in the winding (P_{indW}) and the rest is due to the core (P_{indC}). The bulk of the total losses comes from the switches, accounting for almost 70% of the losses in the MPC. The conduction losses (P_{onMOS}) account for almost 40% of the total loss, which is noticeably higher than the switching losses. This is because the configuration of FBSs used in the experimental verification is as shown in Figure 3.3 (a). Thus, when a switch is turned ON, it is conducting through the diode of the other pair as well, therefore, its losses are also considered. As the WBG technology matures and the adoption of GaN (which has better characteristics than SiC) based switches increase, the losses in the switches will drop due to the reduction in the switching times (t_{on} and t_{off}) and the on-state resistance (R_{DSon}).

Table 4. 2: Parameters used in the validation of T_B.

Parameter	Value	Unit
Inductance (L_1/L_1)	1000/1000	µH
Output capacitor (C)	4.7	mF
Voltage sources (V_1/V_2/V_3/V_4)	100/50/150/75	V
Output voltage (V_o)	200	V
Load resistor	1000	Ω
Switching frequency (F_{sw})	20	kHz

4.3 Key results for T_B

T_B was verified in simulation and validated on the in-house HIL platform. Table 4.2 presents the selected components and parameters used. Open loop verifications were performed by operating T_B in various operation modes at different duty cycles, with some results presented in Figure 4.7. This was done to ensure that the MPC's performance in simulation and HIL verification matched the expected analytical results.

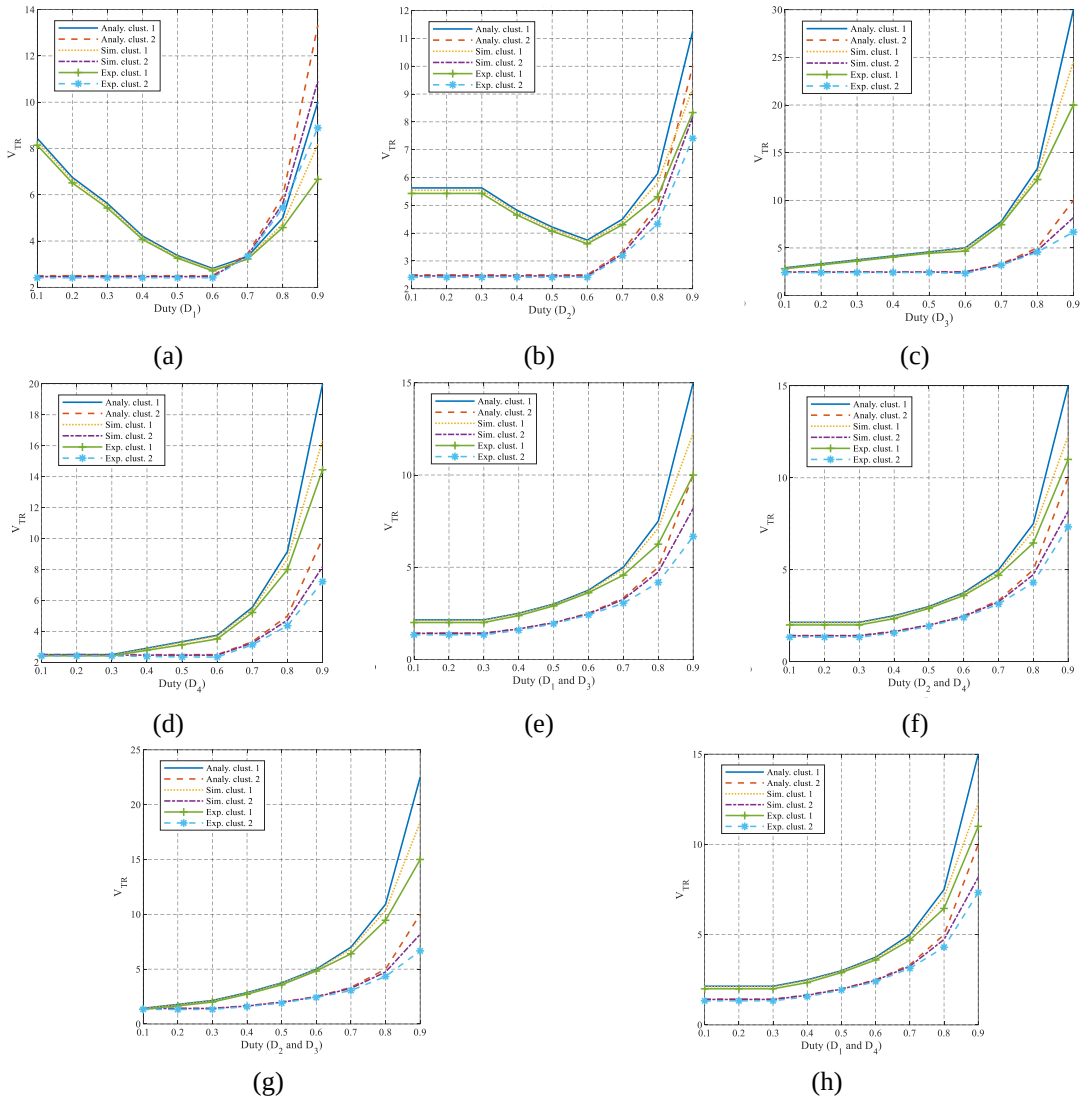


Figure 4. 7: Verification of the MPC with the obtained V_{TR} per cluster from analytical calculation, detailed simulation, and HIL experimental results for (a) D_2=D_3=0.3, and D_4=0.6, (b) D_1=D_3=0.3, and D_4=0.6, (c) D_1=0.3, and D_2=D_4=0.6, (d) D_1=D_3=0.3 and D_2=0.6, (e) D_1=D_3=0.3, (f) D_2=D_4=0.3, (g) D_2=D_3=0.3 and (h) D_1=D_4=0.3.

Notably, in Figure 4.7 (a), D_2 and D_3 are fixed to 0.3 and D_4 is fixed at 0.6 while D_1 is varied from 0.1 to 0.9. Since the voltage in cluster 1 is less than that of the inputs in cluster 2 for in this case, a downtrend is observed in V_{TR} until the duty of 0.6 from which point the uptrend starts for both clusters. Similarly, in Figure 4.7

(b), D_1 and D_3 are fixed to 0.3 and D_4 is fixed at 0.6 while D_2 is varied from 0.1 to 0.9. Again, a downtrend is observed between the D_2 of 0.3 and 0.6 due to the voltages in cluster 1 being less than that of cluster 2. Further, in all the cases considered, cluster 1 has a visibly higher V_{TR} than cluster 2 because their voltages are much lower than of the inputs in cluster 1. V_{TR} of cluster 2 will also be visibly higher than that of cluster 1. Overall, from the results in Figure 4.7, in all the cases considered, the trends are all congruent for analytical calculation, simulation and HIL verification despite the expected losses in the detailed simulation and HIL verification at high (>0.8) duty cycles.

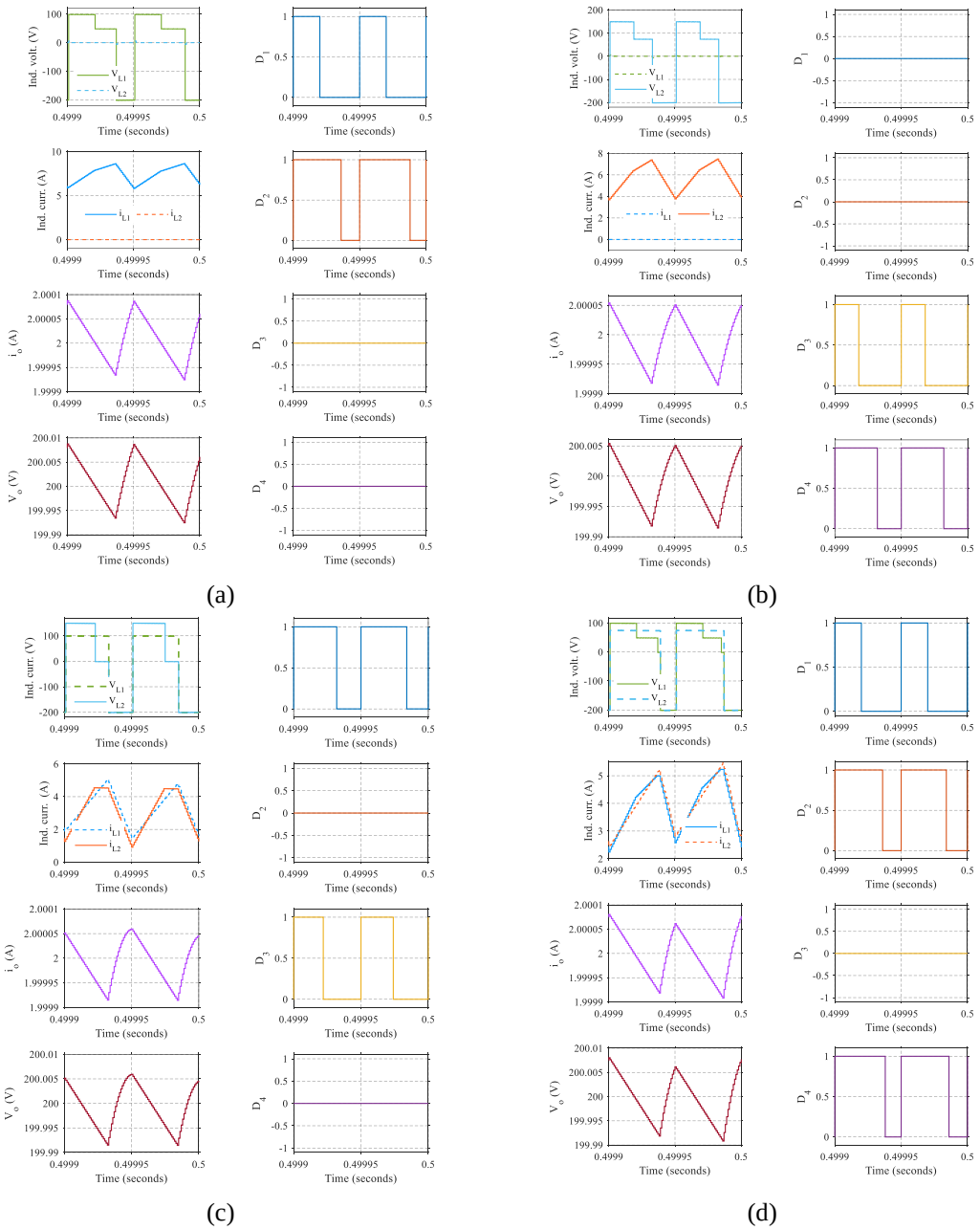


Figure 4. 8: Closed loop verification results of the MPC operation when the dc link is supplied form (a) V_1 and V_2 (b) V_3 and V_4 (c) V_1 and V_3 and (d) V_1, V_2 and V_4.

Closed loop verifications were also performed on T_B under the various modes of operations. The results presented in Figures 4.8 and 4.9 verify some of T_B's operation under simultaneous power transfer, showing the waveforms for inductor voltages (V_{L1} & V_{L2}) and currents (i_{L1} & i_{L2}), output current (i_o) and voltage (V_o), and the duty cycles controlling the input sources (D_1, D_2, D_3 & D_4), respectively. Figures 4.8 (a) – (d) and 4.9 present the results of simultaneous power transfer from the inputs to the dc link, exclusively from cluster 1; cluster 2; V_1 and V_3; V_1, V_2 and V_4; V_1, V_3 and V_4; and from all inputs, respectively. Noticeably, since cluster 1 and 2 are exclusively supplying power to the dc in Figures 4.8 (a) and (b) respectively, the respective inductor voltage and current for the cluster not supplying the dc link is equal to zero. Further, when power is transferred simultaneously from both clusters as in Figures 4.8 (c) – Figures 4.9, the inductor current from either one of the clusters plateaus when the inductor stops charging while waiting for charging to complete in the alternate inductor. In all the cases, V_o was set to a target of 200 V and hence the average i_o was about 2 A with acceptable ripples in i_L, i_o and V_o.

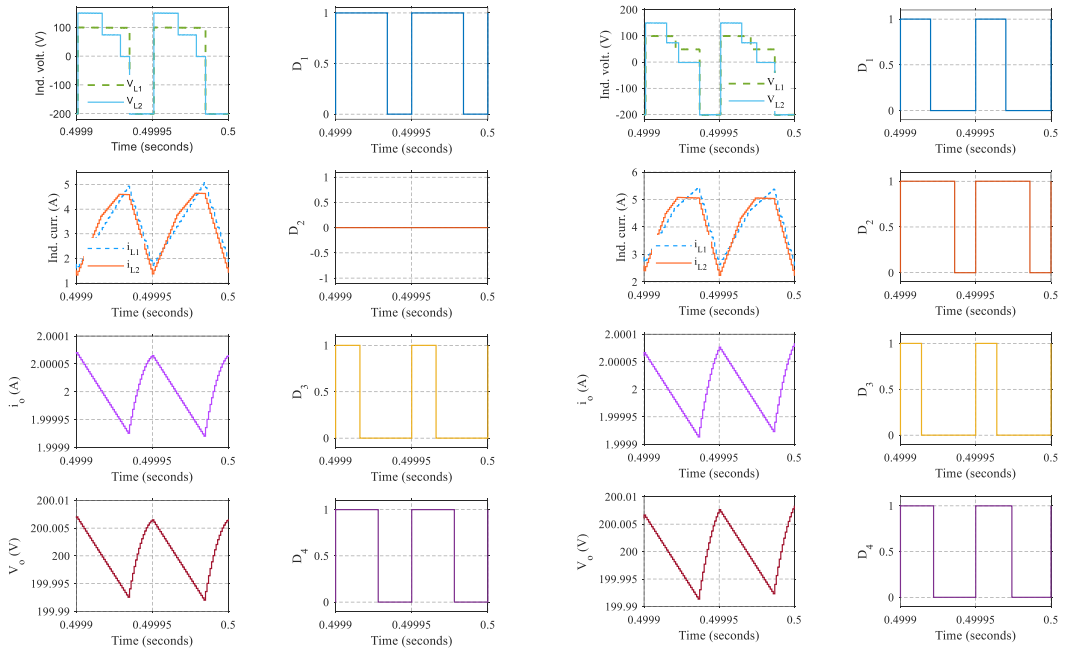


Figure 4. 9: Closed loop verification results of T_B's operation when the dc link is supplied from (a) V_1, V_3 and V_4 and (b) All four inputs.

4.4 Key results for T_C

T_C was also numerically verified in simulation and validated through HIL implementation. The validation and the values of the different component's

parameters are presented on Table 4.3. The verification and validation were implemented in open loop with three different scenarios. The first scenario is selected to have $V_1>V_2$ and $D_1<D_2$ and the other two scenarios have equal voltages but $D_1<D_2$ in the second scenario and $D_1=D_2$ in the third case. The HIL implementation results are presented in Figures 4.10 - 4.12, respectively, for the three scenarios while more details for simulations results are in paper III. In these results, the currents (i_{V1} and i_{V2}) from each of the sources are presented as well as the voltages across the switches (S_{W1}, V_{SW1}; S_{W2}, V_{SW2}; D, V_D), voltage and current in the primary (V_P and i_P), secondary (V_S and i_S) winding and the dc bus (V_{dc} and i_{dc}). The current in the magnetizing inductance (i_{mag}) is presented only in the simulation results due to the difficulty of measuring it in actual implementation.

Table 4. 3: Parameters used in the validation of T_C.

Parameter	Value	Unit
Magnetising inductance (L_m)	680	µH
Output capacitor (C)	4.7	mF
Voltage sources (V_1/V_2)	200/100	V
Clamp capacitor	47	µF
Clamp resistor	1000	Ω

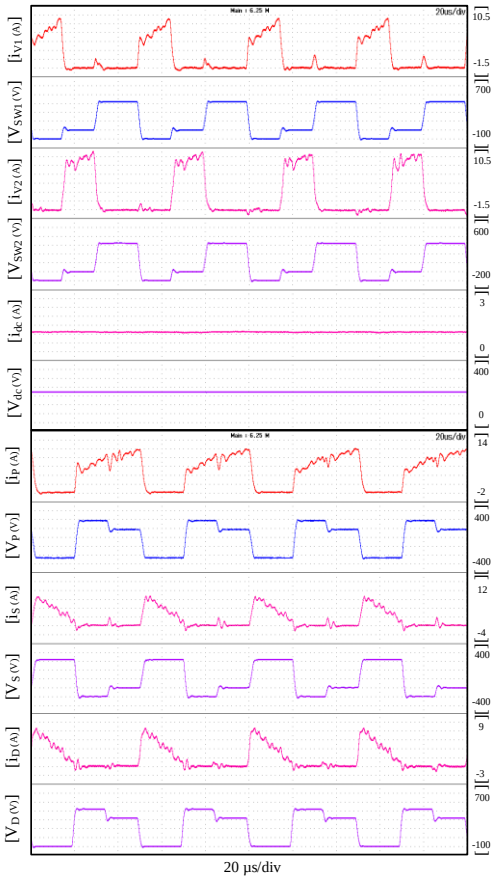


Figure 4. 10: HIL results for V_1=200 V, V_2=100 V, D_1=0.3 and D_2=0.6.

In the first scenario, results are presented in Figure 4.10, V_1=200 V, V_2=100 V, D_1=0.3, D_2=0.6. Since the input voltages are different, the current from the sources is time multiplexed so during the first 30% of the switching period (T_S), only V_1 is charging L_m since D_1=0.3, and in the second 30% of T_S only V_2 is charging L_m since D_2=0.6 hence D_{2eff}=0.3. The values of V_{dc} and i_{dc} are about 223 V and 1.4 A with the ripple of V_{dc} being less than 1 mV in simulations. In the HIL implementations, V_{dc} and i_{dc} are about 220 V and 1.2 A, thus validating the analytical result of 220 V for V_{dc}.

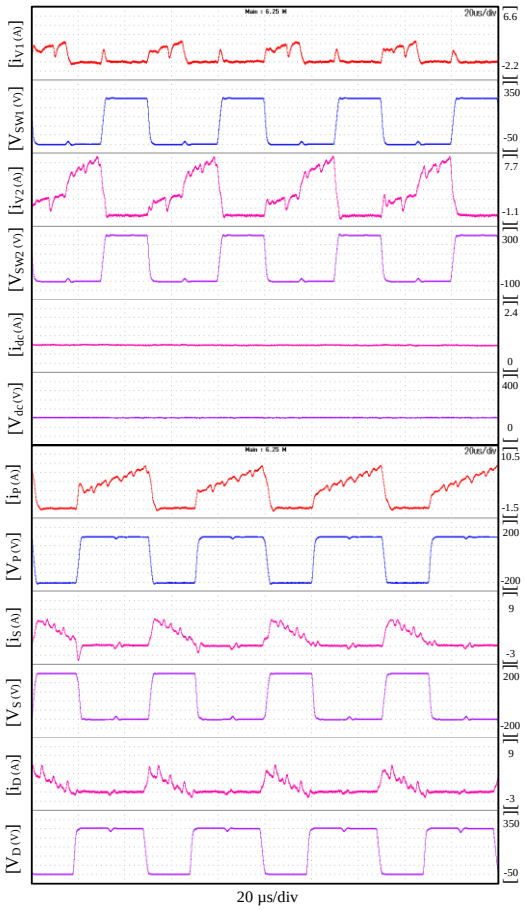


Figure 4. 11: HIL results for V_1=V_2=100 V, D_1=0.3 and D_2=0.6.

Similar characteristics are noticed in the second scenario presented in Figure 4.11, but in this case, V_1=V_2=100 V. Since the voltages are now equal, both V_1 and V_2 are charging L_m at the beginning of T_S, delivering equal amounts of energy. Since D_1<D_2, at the end of D_1, V_2 continues to charge L_m till the end of D_2, thus V_1 is delivering less energy to the dc bus than V_2. The values of V_{dc} and i_{dc} are about 148 V and 0.9 A, respectively, with the ripple of V_{dc}, being less than 1 mV in simulation

while in the HIL implementation V_{dc} and i_{dc} are about 145 V and 0.9 A, respectively. Again, these results validate analytical result of 150 V for V_{dc}.

The results of the third scenario are presented in Figure 4.12. This scenario is like the second except that D_1=D_2=0.6. The values of V_{dc} and i_{dc} are like those obtained in the second scenario. The major difference in the third scenario is that since V_1=V_2=100 V and the duty cycles are equal, both sources are delivering equal amounts of energy to the dc bus.

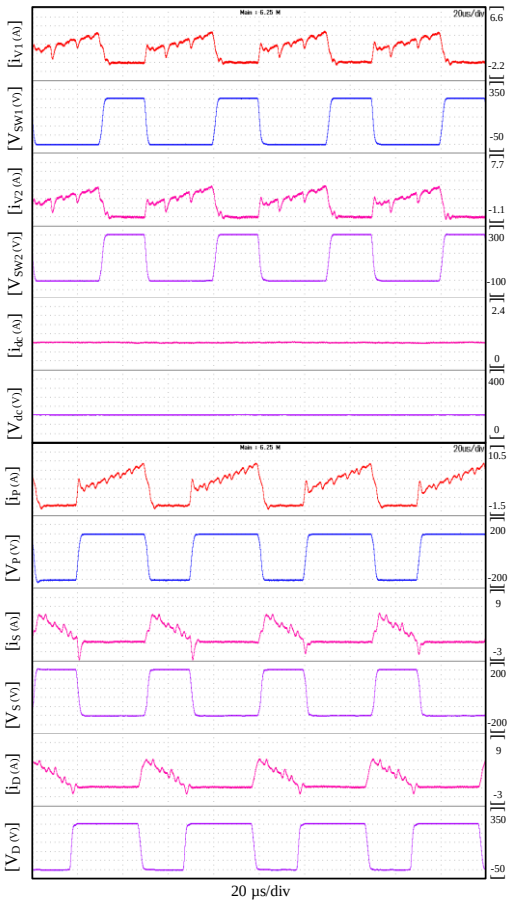


Figure 4. 12: HIL results for V_1=V_2=100 V and D_1=D_2=0.6.

Further, in Fig. 4.13, the V_{TR}-duty cycle relationship of the proposed MPC is compared across analytical calculations, detailed simulation, and HIL validation. The MPC's performance in simulation and HIL implementation closely matches the analytical calculation. Since the turns ratio of the coupled inductor used is 1, the highest V_{TR} obtained in all three cases was 10. At V_{TR}<2, the MPC is bucking the input voltages while it is boosting when V_{TR}>2. This result validates the buck-boost and the high gain characteristic of the proposed MPC.

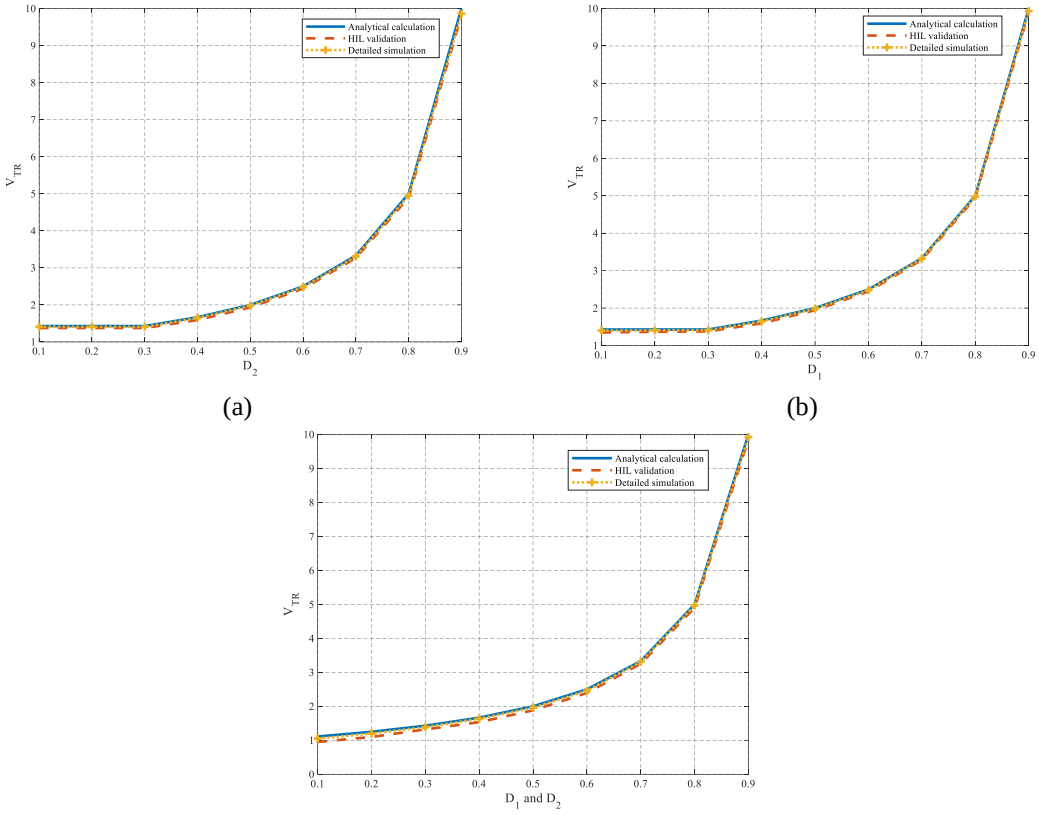


Figure 4. 13: Obtained V_{TR} where (a) V_1 = 200 V, V_2 = 100 V and D_1 = 0.3 (b) V_1 = V_2 = 100 V and D_2= 0.3 and (c) V_1 = V_2 = 100 V.

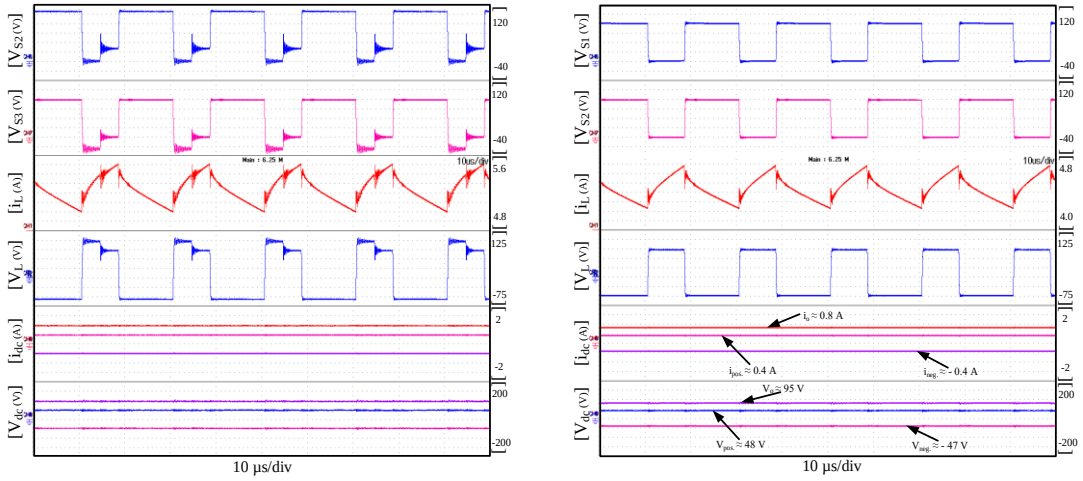
Table 4. 4: Parameters used in the validation of T_D.

Parameter	Value
Switching frequency (F_{SW})	50 kHz
V_1	100 V
V_2	75 V
L, Hammond – 195E50	2.5 mH/50 A/8 mΩ
$L_b = L_1 = L_2$, Hammond – 195C50	1 mH/50 A/5 mΩ
$C_1 = C_2$, KEMET – ALS70A472NF500	4.7 mF/500 V/59 mΩ
Diodes, SemiQ – GHXS050B065S-D3	650 V/50 A
MOSFETs, CREE – C2M0080120D	1200 V/36 A/80 mΩ

4.5 Key results for T_D

The MBDC topologies in T_D were numerically verified in simulations using Matlab's Simulink. Further, T_{D4} and T_{D5} were verified on the in-house experimental test setup using the circuit parameters presented in Table 4.4. To achieve the RB capability required in S_1 to S_3 in T_{D4} and T_{D5}, each SiC MOSFET was connected in series to a SiC diode since the RB WBG devices are not commonly available on the market at this time. Although all five MBDCs proposed

were tested in simulations, only results for T_{D4} and T_{D5} are presented here since only these two topologies were validated on the experimental test platform, and other results can be found paper IV. Further, although the MBDCs in T_D are capable of independent power flow from the sources, only results for simultaneous power flow are presented since the independent power flow operation is like the conventional single input converters, which are sufficiently addressed in literature.

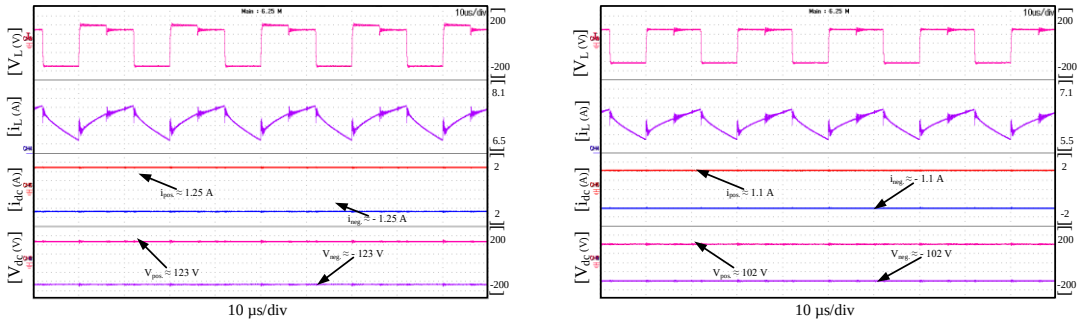


(a) (b)

Figure 4. 14: Verification results for operating T_{D4} when (a) V_1=100V, V_2=75V, d_1=20% and d_2=40% and (b) V_1=V_2=75V and d_1= d_2=40%.

To validate the operation of T_{D4}, two different scenarios of different and equal input voltages are tested in this section. The results of the first scenario are presented in Figure 4.14 (a). In this scenario, the input voltages are unequal with V_1 = 100 V, V_2 = 75 V, so the duty cycles applied to S_2, S_3 are d_1 = 20%, d_2 = 40% such that D_{1eff} = D_{2eff} = 0.2. A resistive load was used in the verification and was set to 100 Ω for all three levels of the bipolar dc bus. $\pm V_O/2$ and V_O are about ±55 V and 109 V while the current is ±0.5 A and 1 A, respectively. This is about 3 V and 7 V drop, while the output currents are ±80 mA and 160 mA lower than the simulation results under similar conditions. Similarly, i_L and Δi_L are about 5.8 A and 0.3 A for the simulation while the experimental ones are not so far apart at about 5 A and 0.5 A, respectively. Other parameters presented include the V_L, the current and voltages of the switches and the inductor of the bipolar dc bus. In the second scenario, V_1 = V_2 = 75 V, and the duty cycles applied to S_2, S_3 are d_1 = d_2 = 40% such that D_{1eff} = D_{2eff} = 0.4. The load is also 100 Ω for all three levels of the bipolar dc bus. $\pm V_O/2$ and V_O are about ±48 V and 95 V while the current is ±0.4 A and 0.8 A, respectively in the results of experimental implementation in Figure

4.14 (b). Further, the inductor current and its ripple, i_L and Δi_L are about 4.45 A and 0.5 A in the experimental implementation, respectively. In both scenarios, the experimental results closely match within 5% with those of simulation and analytical calculations. Further, because the input voltages are different in the first scenario, V_2 only starts to supply the output by charging the inductor after S_2 has been turned off. This is indicated in the switch current and voltage (i_{S2}, i_{S3}, V_{S2} and V_{S3}) controlling the input sources V_1 and V_2, respectively as shown in Figure 4.14 (a). While S_2 is conducting, the voltage of S_3 is negative, at about –25 V, which is V_2–V_1, because of its reverse current blocking action. Further, while S_3 is conducting, the voltage of S_2 is about 25 V, which is V_1–V_2, also due to its reverse blocking action. In the second scenario, since both voltages and duty cycles are equal, V_1 and V_2 are supplying equal currents to the load. Furthermore, the bipolar dc bus is kept balanced by applying a duty cycle of 50% to S_{b1} and S_{b2} in both scenarios. Further, T_{D4} is tested for operation under higher duty cycles (d_1=30% and d_2=60%) to prove its high gain characteristics with results presented respectively in Figure 4.15 for unequal (V_1>V_2) and equal (V_1=V_2) input voltages. Under these conditions, the performance of the MBDC is desirable and acceptable as compared to analytical results.

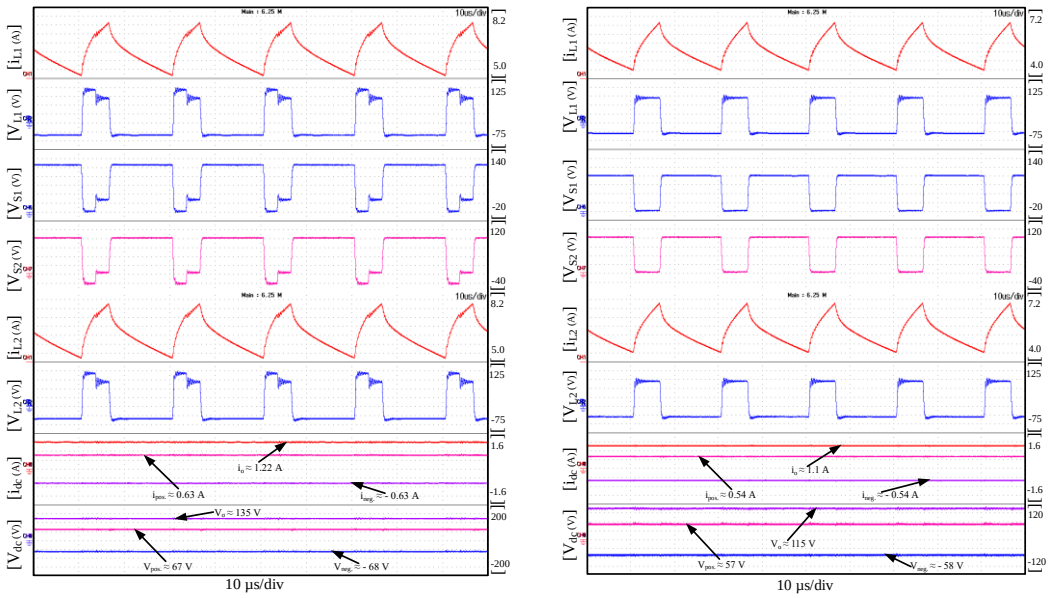


(a) (b)

Figure 4. 15: Experimental verification of T_{D4} at high duty of d_1=30% and d_2=60% for (a) V_1=100V, V_2=75V, and (b) V_1=V_2=75V.

T_{D5} was also validated under two different scenarios like in T_{D4}: different and equal input voltages. In the first scenario of T_{D5} in Figure 4.16 (a), V_1 = 100 V, V_2 = 75 V are just like in T_{D4}, but in this case, the duty cycles applied to S_2 and S_3 are d_1 = 15% and d_2 = 30% such that D_{1eff} = D_{2eff} = 0.15. The resistive load across each pole of the dc bus was set to 100 Ω. The output voltages obtained in the experimental implementation are about ±68 V and 135 V, which are about 10% drop from the simulation results of ±75 V and 150 V, respectively, for $\pm V_O/2$ and V_O. The output

currents in simulations are ±0.75 A and 1.5 A, and about ±0.63 A and 1.22 A in the experimental implementation. Further, the currents and voltages of L_1 and L_2 are equal (i.e., $i_{L1} = i_{L2}$ and $V_{L1} = V_{L2}$) in the simulation and experimental results: $i_{L1} = i_{L2} \approx 6.45$ A, $\Delta i_{L1} = \Delta i_{L2} \approx 0.5$ A in simulations, and $i_{L1} = i_{L2} \approx 6.2$ A, $\Delta i_{L1} = \Delta i_{L2} \approx 2.4$ A in the experiments. In the second scenario of T_{D5} with experimental results presented in Figure 4.16 (b), $V_1 = V_2 = 75$ V and $d_1 = d_2 = 30\%$ such that $D_{1eff} = D_{2eff} = 0.3$, the load at the poles of the bipolar dc bus was set to 100 Ω. The output voltages of the three levels are about ±58 V and 115 V with output currents of about, ±0.54 A and 1.1 A, respectively. Like the first scenario, the currents and voltages in the inductors are equal, i.e., $i_{L1} = i_{L2}$ and $V_{L1} = V_{L2}$. The experimental output voltages are about 10% less than those in the simulations, which are slightly higher than those obtained for T_{D4} because of the increased losses due to higher component count and higher current flowing through the inductors to achieve the higher voltage gain. Although T_{D5} has a higher gain than T_{D4}, avoiding the potential for increased losses at higher duty cycles must be taken into consideration. Other parameters such as S_{b1}, S_{b2} and L_b behave in T_{D5} as earlier discussed for T_{D4}. In short, the experimental results are congruent with the expected characteristics discussed in Chapter 3 of this dissertation.

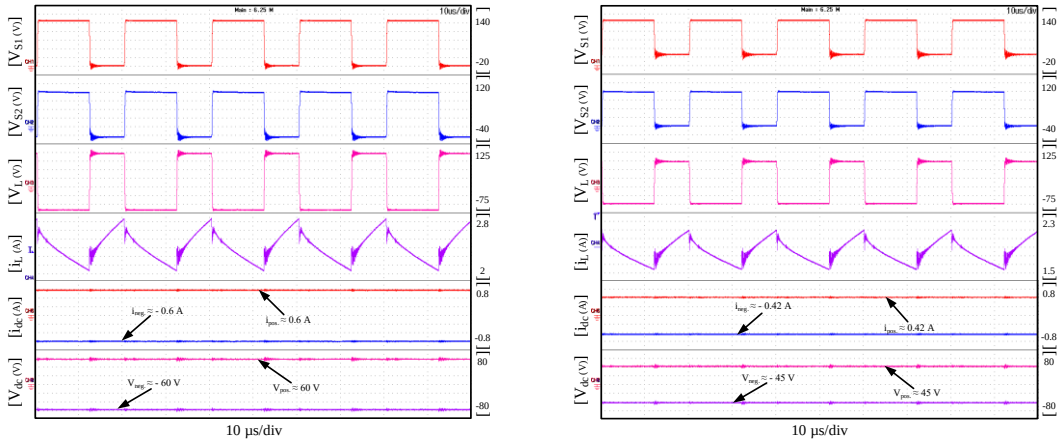


(b) (c)

Figure 4. 16: Verification results for operating T_{D5} when (a) V_1=100V, V_2=75V, d_1=20% and d_2=40% and (b) V_1=V_2=75V and d_1= d_2=40%.

The experimental verification of arbitrary independent power flow from both sources was performed for T_{D4} and the results are presented in Figure 4.17. In

Figure 4.17 (a), only the first input source, V_1, is supplying energy to the bipolar dc link thus d_1=40% and d_2=0, such that D_{1eff}=0.4 and D_{2eff}= 0. V_1=100 V, V_2=75 V and the load at the poles of the bipolar dc bus was set to 100 Ω. Under these conditions, the bipolar output voltages and currents are about ±60 V and ±0.6 A, respectively, while i_L and Δi_L are about 2.4 A and 0.6 A, respectively.
Similarly, in Figure 4.17 (b), only the V_2 is supplying energy to the bipolar dc link, thus d_1=0 and d_2=40% such that D_{1eff}=0 and D_{2eff}=0.4, and the loads were also set to 100 Ω. The input sources and output loads are the same as earlier when only V_1 is supplying (V_1=100 V, V_2=75 V and 100 Ω). In these conditions, the bipolar output voltages and currents are about ±45 V and ±0.42 A, while i_L and Δi_L are about 1.8 A and 0.55 A, respectively. This proves the performance of the MBDCs under arbitrary independent power flow.

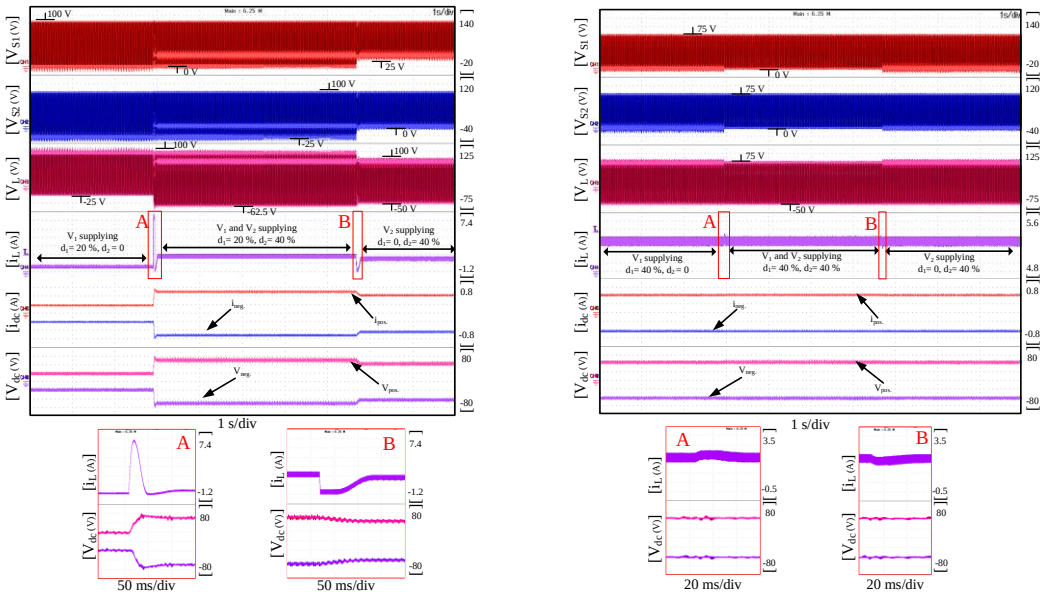


(a) (b)

Figure 4. 17: Experimental verification of independent power flow from the input sources for (a) V_1 only supplying when V_1=100V, V_2=75V, d_1=40% and d_2=0, and (b) V_2 only supplying when V_1=100V, V_2=75V, d_1=0 and d_2=40%.

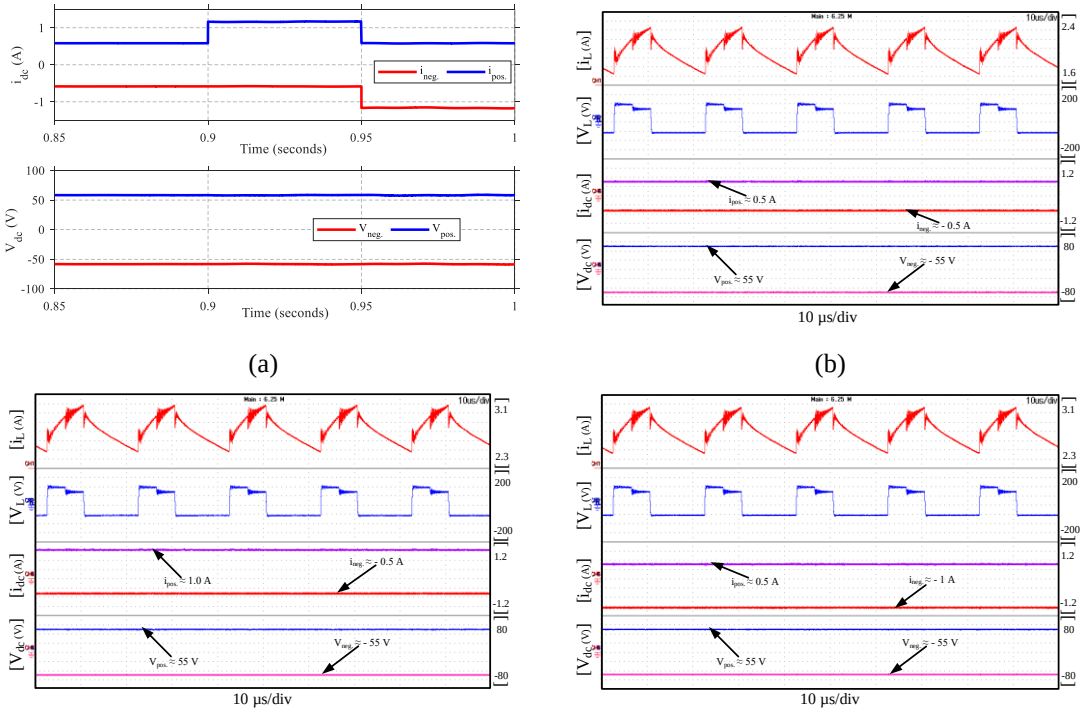
Further, T_{D4} was verified for transition between the independent and simultaneous power flow from both sources during operation with results presented in Figure 4.18. In Figure 4.18 (a), V_1=100 V and V_2=75 V, and for the first 3 seconds, only V_1 is supplying the dc link with d_1=20% and d_2=0, during which the output voltages and currents are about ±20 V and ±0.2 A, respectively. During the next 5 seconds, both V_1 and V_2 are supplying the dc link with d_1=20% and d_2=40%. Therefore, the output voltages and currents increased to about ±55 V and ±0.5 A, respectively. Finally, in the last few seconds, only V_2 is supplying the dc link with d_1=0 and d_2=40%, thus the voltages and currents at the output decrease to about ±45 V and ±0.4 A, respectively. Similar tests are performed when the input

voltages are equal i.e., V_1=V_2=75 V, being presented in Figure 4.18 (b). Under this condition, the voltages and currents at the output are about ±45 V and ±0.4 A, respectively. These results demonstrate a seamless transition between independent and simultaneous modes of power transfer from the inputs to the bipolar dc link.



(a) (b)

Figure 4. 18: Experimental verification of operating mode transition for (a) V_1=100 V, V_2=75 V, and (b) V_1=V_2=75 V.



(a) (b)

(c) (d)

Figure 4. 19: Verification results for operating T_{D4} under unbalanced loads when V_1=100V, V_2=75V, d_1=20% and d_2=40% for (a) simulation result, (b) experimental for $R_{pos.}$=$R_{neg.}$=100Ω, (c) experimental for $R_{pos.}$=50Ω, $R_{neg.}$=100Ω and (d) experimental for $R_{pos.}$= 100Ω, $R_{neg.}$=50Ω.

To validate the self-balancing characteristics of T_D, T_{D4} was operated with different loading conditions of the positive and negative poles. The simulation and experimental results are presented in Figure 4.19. For both cases V_1 = 100 V, V_2 = 75 V, d_1 = 20%, d_2 = 40% and the duty of 50% was applied to S_{b1} and S_{b2}, alternately. It was observed that although the load is increased on one pole, the output voltages remain balanced, being the key feature of the proposed MBDCs. The bipolar dc bus voltage balancing does not require a closed loop control to keep the output voltage balanced on both poles under these disturbances.

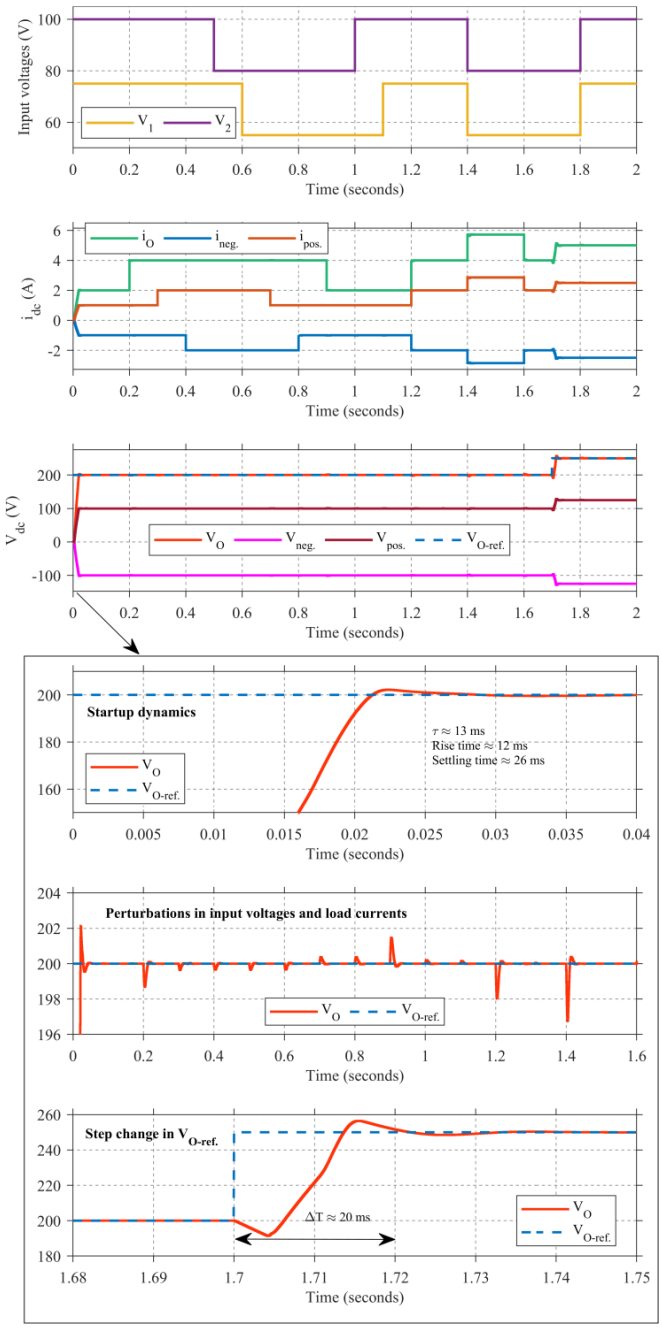
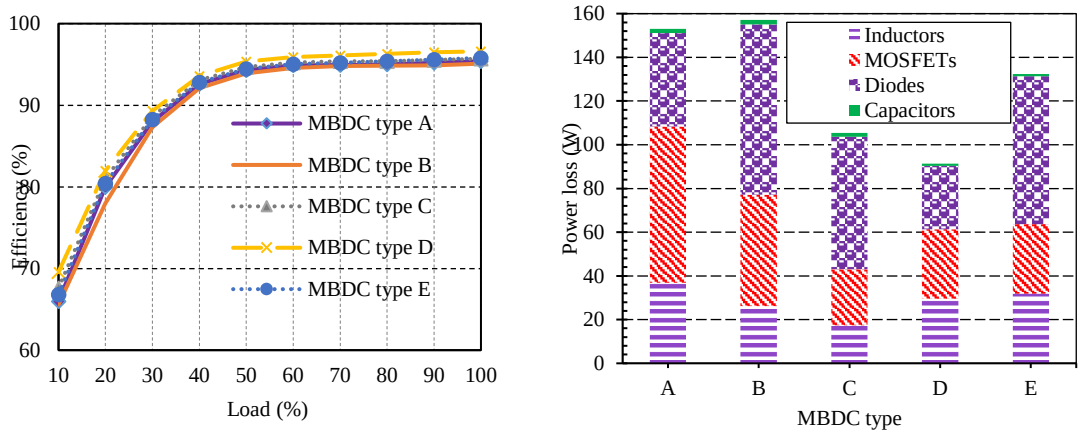


Figure 4. 20: Closed loop performance of T_{D1} under perturbations in the input voltages, load currents and output reference voltage.

Furthermore, the closed loop performance of T_D was examined with results for T_{D1} presented in Figure 4.20. Under various changes, in the load currents, input and output voltages, a set of heuristically selected PI gains for the double loop PI controller is sufficient to achieve desirable characteristics. The rise time is less than 15 ms, settling time is less than 30 ms and overshoot is less than 2 V at converter start-up. Under all the different perturbations, the controller can track the reference voltage with minimal perturbations on the output voltage. This result further proves the ability of the GVD based MBDCs to keep the voltages at the respective poles balanced under unbalanced loads, without the need for a dedicated controller.



(a) (b)

Figure 4. 21: Efficiency analysis (a) at different loading conditions and (b) loss distribution at 2 kW load with V_O = 200 V and $V_1 = V_2$ = 100 V.

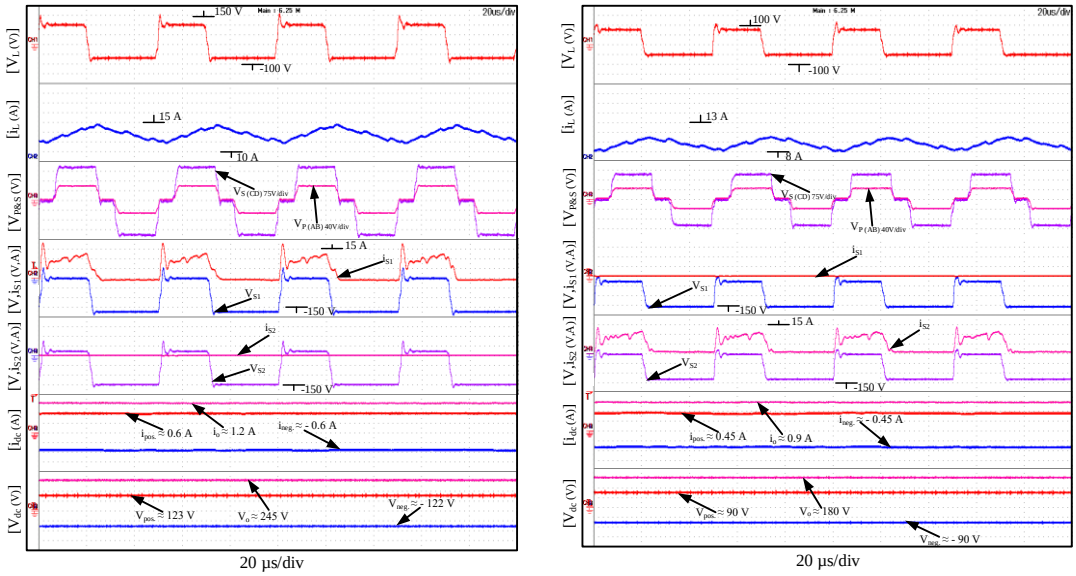
The power losses (P_L) in T_D can also be estimated using (4.1), and based on (4.1), the efficiency at different loading conditions and loss distribution in the components of the proposed family of MBDCs was computed and presented in Figure 4.21, respectively. This loss distribution was computed at 2 kW load with the positive and negative poles ($\pm V_O/2$) having 600 W each, and the full dc link (V_O) was 800 W. Both input sources were equal at 100 V, and V_O of the converter was regulated to 200 V. T_{D1} and T_{D2} exhibit the most losses under these conditions due to the losses in the diodes. T_{D3} shows remarkably lower losses since it requires fewer active switches and diodes than T_{D1} and T_{D2}, respectively. However, due to the ultra-high gain of T_{D3}, high currents flow through the switches and the voltage stress on its active switches are high. T_{D5} also experiences more than 100 W of losses due to the diodes in the switched inductors. Comparatively, T_{D4} and T_{D5} have lower losses than T_{D1} and T_{D2}, respectively, showing that the use of the SBC based bipolar outputs have lower losses than the use of the GVDs.

4.6 Key results for T_E

T_E was quantitatively verified in simulation and on the HIL platform and the values of the various component's parameters are listed in Table 4.5. Open loop operation was carried out in 5 scenarios, the first two representing independent power flow from the two sources (V_1 and V_2) to the dc link, respectively. The last three open loop scenarios represent operation of T_E in simultaneous power flow from both sources with equal and unequal voltage levels, respectively. And lastly, the converter was operated in a closed loop to examine the natural symmetry capability of the converter's bipolar outputs. Figure 4.22 presents the open loop verification of operating T_E with only the first voltage source, V_1, and the second voltage source, V_2, supplying the bipolar dc link, respectively. For both scenarios, V_1 is set to 100 V, V_2 is 75 V and the results presented include inductor current (i_L) and voltage (V_L), primary (V_P) and secondary (V_S) turns voltage of the transformer, input currents, voltages of S_1 (i_{S1}, V_{S1}), S_2 (i_{S2}, V_{S2}), the dc link (i_{dc} and V_{dc}), and the voltage across the switches of the PS-FB section, $V_{Q1} - V_{Q4}$ and $V_{Da} - V_{Dd}$. In Figure 4.22 (a), the results of V_1 alone supplying are presented. To achieve this, the duty cycle, D_1, of the switch, S_1, controlling the first voltage source, V_1, is set to 0.4 while that of S_2, D_2 is set to 0. The load across each pole and the full dc link was set to 200 Ω each. The results presented in Figure 4.22 (a) are congruent with numerical solutions with $\pm V_o/2$ and V_o at about ±123 V and 245 V, respectively, and $\pm i_o/2$ and i_o at about ±0.6 A and 1.2 A. In Figure 4.22 (b), the results of independent power flow from V_2 are presented. D_1, the duty cycle of S_1 was set to 0, while that of S_2, D_2 was set to 0.4. The load across each of the voltage levels was also 200 Ω each. Again, the results in Figure 4.22 (b) show good agreement with numerical solutions with $\pm V_o/2$ and V_o being about ±90 V and 180 V, respectively, and $\pm i_o/2$ and i_o at about ±0.45 A and 0.9 A, respectively.

Table 4. 5: Parameters used in the validation of T_E.

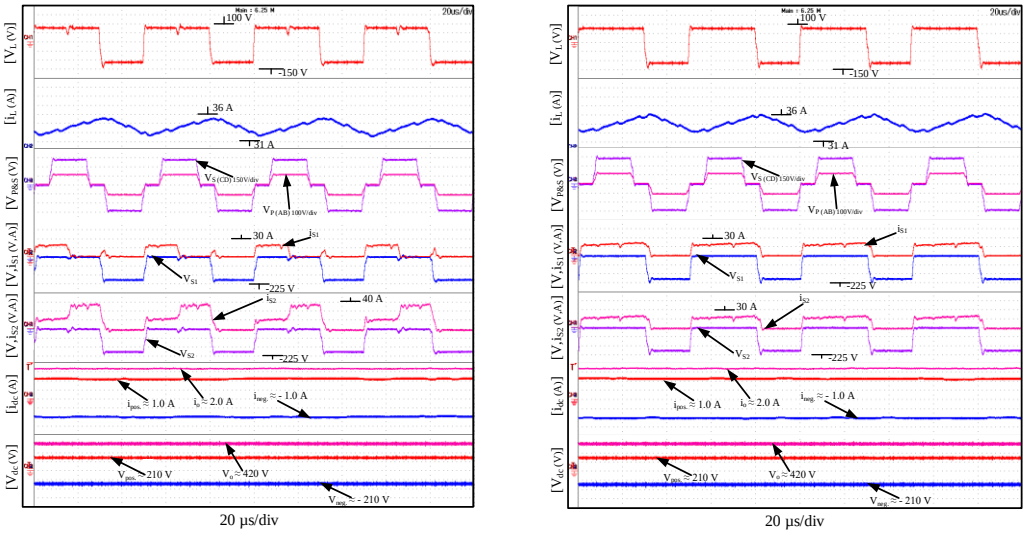
Parameter	Value	Unit
Inductor (L)	1	mH
Capacitors (C=$C_{pos.}$=$C_{neg.}$)	4.7	µF
Voltage sources (V_1/V_2)	100/75	V
Transformer turns ratio (n)	2	
Phase shift ($Ø$)	27	degrees
Switching frequency (F_{SW})	20	kHz



(a) (b)

Figure 4. 22: Results of supply to the dc bus where V_1=100V, V_2=75V, from (a) only V_1, thus D_1=0.4 and D_2=0 and (b) only V_2 thus D_1=0 and D_2=0.4.

Figure 4.23 presents the results of the last three scenarios of open loop operation, i.e. simultaneous power transfer from the two inputs to the bipolar dc link. Figures 4.23 (a) and (b) have the same output characteristics since they have the same effective duty, $\sum_{i=1}^{N} D_{ieff}$, of 0.6 and equal input voltages with V_1=V_2=75 V. Hence, the results in Figures 4.23 (a) and (b) are both, also consistent with the numerical solutions with $\pm i_o/2$ and i_o being about ±1.0 A and 2.0 A, respectively and $\pm V_o/2$ and V_o at about ±210 V and 420 V, respectively. The main difference with both scenarios is that D_1 was set to 0.3 and D_2 to 0.6 in Figure 4.23 (a) such that D_{1eff}=0.3 and D_{2eff}=0.6, so since both voltages are equal, while S_1 is ON, S_2 is also ON and both sources are charging the inductor, L, and then when D_1 goes OFF, only D_2 is charging L. Thus, the average i_{S2} is larger than from i_{S1}, while in Fig. 4.23 (b), D_1=D_2=0.6 and so since they have equal voltages, both sources are charging the inductor with currents i_{S1}=i_{S2} during the inductor charging. This is an indication of how the duty cycle is used to control the energy delivered by the respective sources. In the case of the fifth scenario in Figure 4.23 (c), where the voltages are different such that V_1 = 100 V and V_2 = 75 V, the inductor charging must be time multiplexed to achieve simultaneous power transfer from both sources to the load. In this case, D_1 was set to 0.3 and D_2 to 0.6 such that D_{1eff}=D_{2eff}=0.3. Also, the results in Figures 4.23 (c) are consistent with numerical solutions with $\pm V_o/2$ and V_o being ±245 V and 490 V, respectively, and the dc link currents at $\pm i_o/2$ and i_o being ±1.2 A and 2.4 A, respectively.



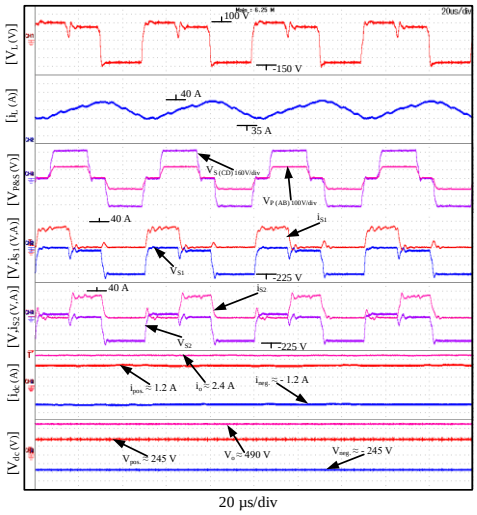


Figure 4. 23: Results when both sources are supplying the dc bus where (a) V_1=V_2=75V, D_1=0.3 and D_2=0.6, (b) V_1=V_2=75V and D_1=D_2=0.6, and (c) V_1=100V, V_2=75V, D_1=0.3 and D_2=0.6.

Further, PI gains were heuristically selected to control T_E to achieve a constant output voltage of $\pm V_o/2$ and V_o of ±100 V and 200 V, respectively, and later stepped to ±125 V and 250 V respectively. Some of the closed loop dynamics are presented in Figure 4.24, specifically the load on the three voltages were randomly varied to examine the natural symmetry characteristics of T_E more closely. The control target was V_o while the positive and negative poles were left uncontrolled to freely balance the voltage across themself. The load on V_o was doubled from about 1 A to 2 A at 8s and V_o experiences a dip of less than 3 V after that the controller can bring it back to the target 200 V. And then the load on the positive pole was also doubled from 0.5 A to 1 A at 12s and the negative pole's load also doubled from 0.5 A to 1 A at 16s. In the load change for both positive and negative poles, a

voltage sag of less than 1 V was experienced on V_o but overall, the load changes on the poles of T_E does not lead to an imbalance in the output voltages, a testament of the natural symmetry of the converter. A further testament of T_E's controller is demonstrated in the startup dynamics, where minimal overshoot is observed with a rise time, time constant and settling time of 75ms, 25ms, and 0.25s respectively. A fast response to step change of 50ms is also observed at 58s. Furthermore, the value of k_1 is varied to demonstrate the ability of the MIBDC to use the MPPT to control the power delivered from the input sources without affecting the output voltages. All these perturbations do not impact the voltage (V_{dc}) or current (i_{dc}) of the critical load.

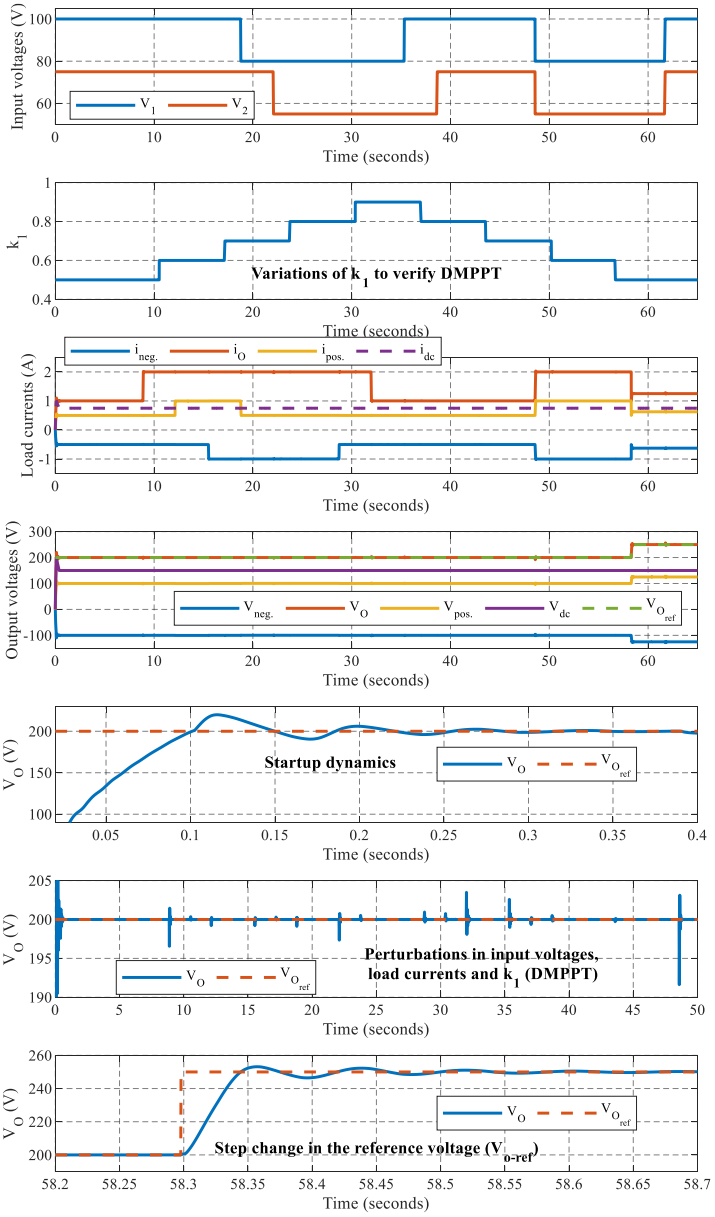


Figure 4. 24: Closed loop performance of the MIBDC under perturbations in the input voltages, load currents and output reference voltage.

Further, the converter operation under different mode transition is verified with results in Figure 4.25. The first column presents transitions in the input voltages (V_1 and V_2) from equal (80 V) to unequal (100 V & 75 V) and back to equal (80 V) voltages. The second and third columns represent transitions from V_2 alone supplying the dc link, simultaneous power flow from V_1 and V_2, and to V_1 alone supplying the dc link, under equal and unequal voltages, respectively. Under all these mode transitions the controller can maintain the output voltages at the target of 200 V and ±100 V.

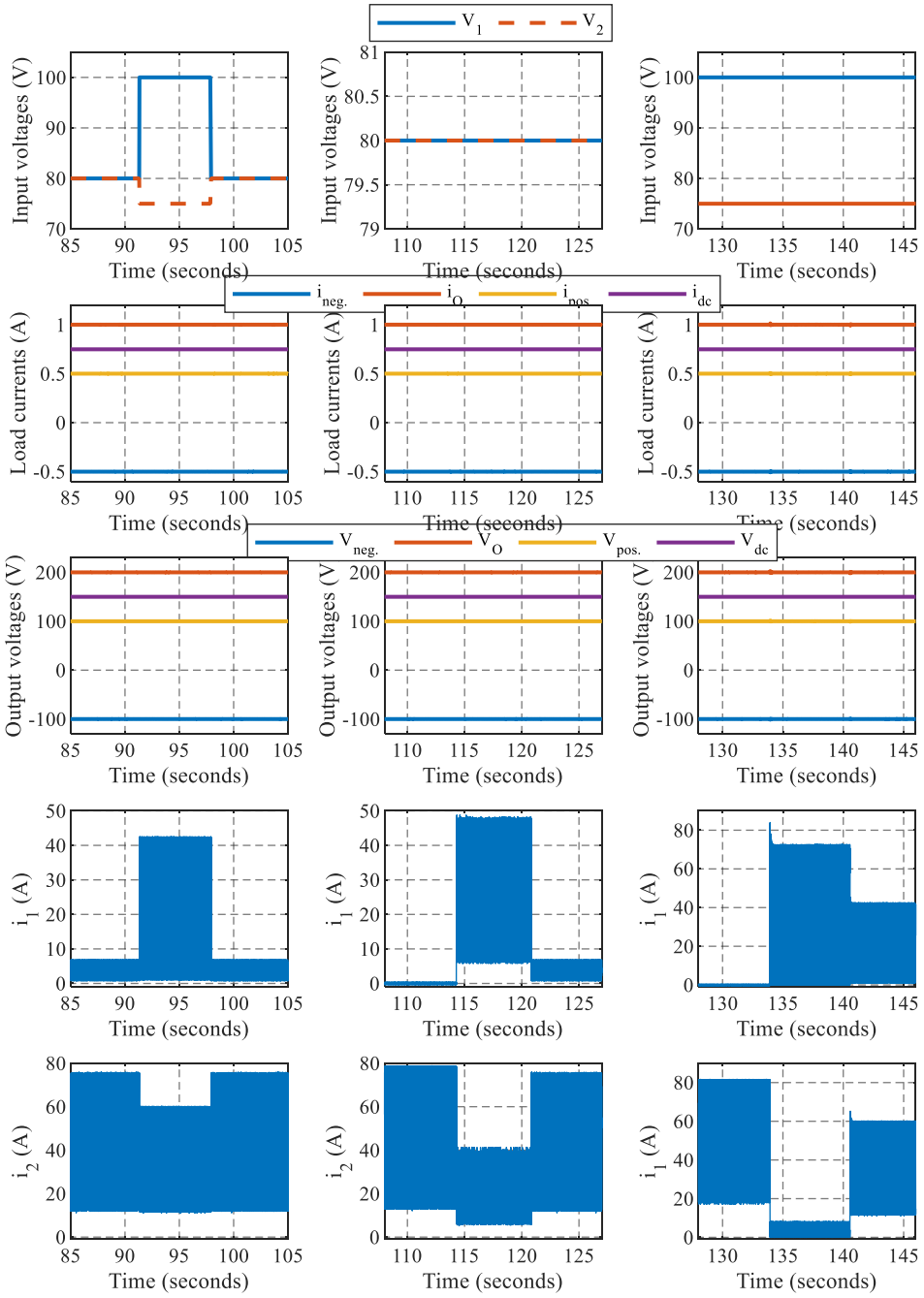


Figure 4. 25: Verification of operating mode transitions.

4.7 Key results for grid integration

Furthermore, the interaction of the MPC topologies proposed in this dissertation with both ac and dc grid systems under different scenarios were studied. Firstly, to prove the reliability of the proposed bipolar MPCs, the T_E in paper VIII was integrated with a bipolar to unipolar dc converter to facilitate reliable power transmission and delivery to mission critical dc systems. Further details of this can be found in Chapter 3 and paper VIII. In Figure 4.26, the operation of the bipolar to unipolar converter under different fault conditions in the poles of the bipolar dc transmission/distribution line is verified. As seen in Figure 4.26, open circuit faults [99] are introduced sequentially in the positive, negative, and neutral lines respectively. Under these faults, the converter can continue to deliver power to the mission critical load or distribution system with no significant impact on the quality of the voltage (V_{dc}) or current (i_{dc}). This, therefore, validates the stated reliability of bipolar dc transmission/distribution for mission critical systems and the applicability of the MPCs with bipolar outputs proposed in this dissertation.

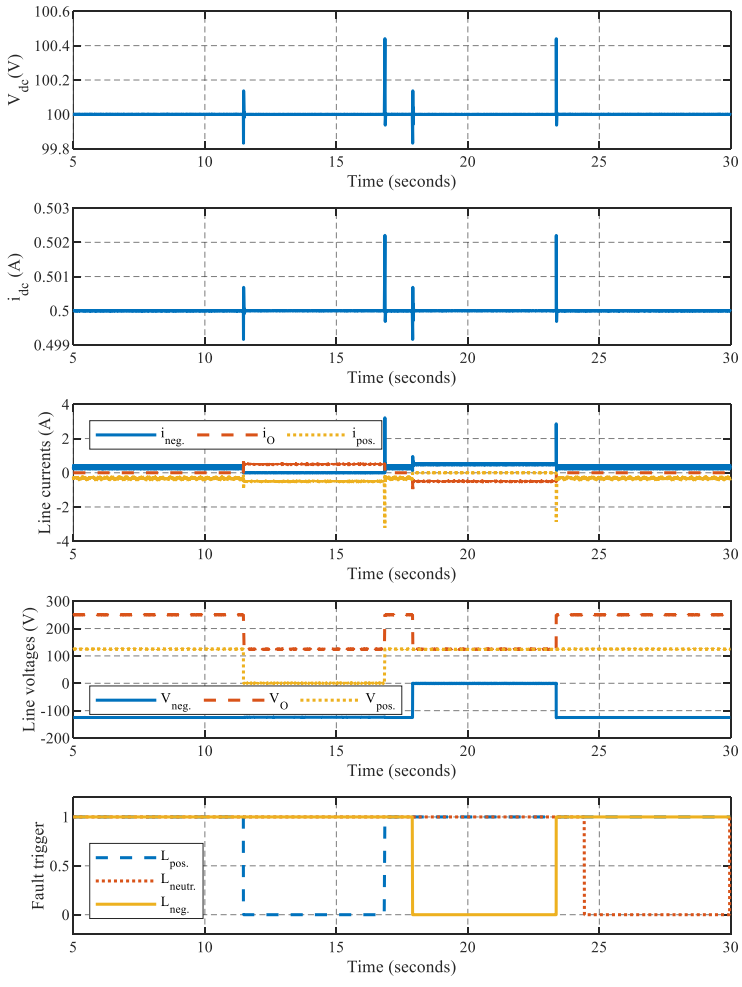
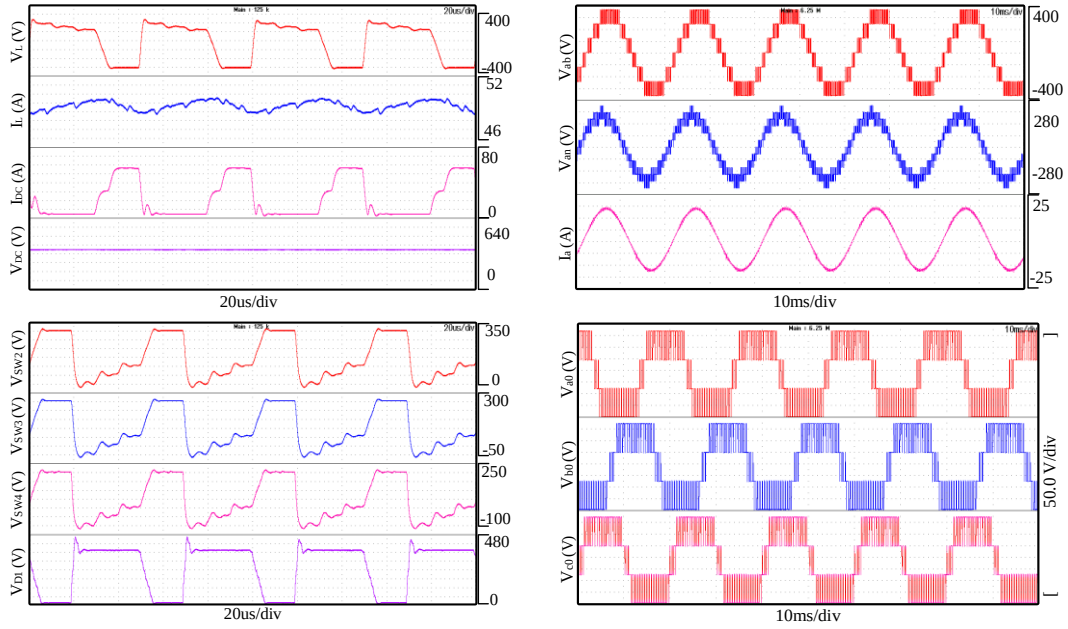


Figure 4. 26: Closed loop performance under line failures.

Table 4. 6: Parameters used in system verification.

Parameter	Value	Unit
Inductor (L)	4	mH
Inductor (L_{b1}=L_{b2})	0.1	mH
Output capacitor (C_1=C_2=C_3)	9.4	mF
Voltage sources (V_1/V_2/V_3)	300/250/200	V
AC load (R – L)	8.1 / 12.5	Ω / mH



(a) (b)

Figure 4. 27: Open loop HIL implementation results showing key waveforms of the integrated MPC-MLI operation when D_1 = 20%, D_2 = 40% and D_3 = 60% for (a) MPC operation and (b) MLI operation.

Further, in paper V, the modified T_A was integrated with an MLI to prove the interaction of the proposed unipolar MPCs for harvesting energy resources predominantly in dc to ac grid. The values of the different component's parameters for verifying this application are presented on Table 4.6. The verification was done in open and closed loop both in simulation and HIL implementation, and the key results are presented here. Further results are presented in paper V. Figure 4.27 presents the open loop results of operating the combination of the modified T_A and the MLI when the input voltages are V_1 = 300 V, V_2 = 250 V, and V_3 = 200 V. The respective duty applied to the switches S_{W2} to S_{W4} are D_1 = 20%, D_2 = 40% and D_3 = 60% (D_{SW2} to D_{SW4}) such that the effective duties, D_{1eff} = D_{2eff} = D_{3eff} =0.2. Under these conditions, the voltage stress of the switches (V_{SW2} to V_{SW4}), inductor (V_L) and the voltage of the dc link, V_{DC}, are presented in Figure 4.27 (a). The dc link voltage is about 372 V and split into three equal parts of 124 V across each of the three dc link capacitors (as shown in Figure 4.28) and are congruent with the results

obtained from the analytical simulation. Furthermore, the MLI stage is operated under level-shifted pulse width modulation (LS-PWM) scheme as described in [79]. The results of the MLI stage is presented in Figure 4.27 (b). The MLI stage was operated to achieve 50 Hz seven-level output voltages, (V_{ab} and V_{an}) and current (i_a) and the pole voltages (V_{a0}, V_{b0} and V_{c0}) at its' output. Again, the results of the MLI's simulation and HIL implementation are consistent. To verify the balancing of the voltage across the dc link capacitors, the control-based voltage balancing technique and circuit-based voltage balancing were implemented and the results for both techniques are in Figure 4.28, respectively. The PI parameters of the controller for the control-based balancing technique were heuristically selected as in [79]. From Figure 4.28 (a), the controller can achieve steady state with the voltage across C_2, V_{C2}, being controlled to about 121 V while C_1 and C_3 try to balance out the remaining 251 V naturally, with obvious oscillations. In the circuit-based capacitor balancing technique, a simple proportional controller is heuristically selected to control the active switches (Sw_{b1} and Sw_{b2}) of the auxiliary capacitor balancing circuit which have the same duty cycle. The result in Figure 4.28 (b) shows how effectively the auxiliary circuit-based technique achieves capacitor voltage balancing with better accuracy than the control-based technique in Figure 4.28 (a). V_{C2} is controlled to about 121 V while the remaining 251 V is balanced equally between C_1 and C_3, with oscillations as seen previously. Comparing the results of the control-based, and circuit-based balancing techniques, the later can more equally balance the voltage left over between C_1 and C_3 after controlling V_{C2} to a specified value. Further, less controller effort is required in the circuit-based topology, but of course requires additional components while the control-based technique requires a complex controller although not requiring any additional components. Thus, a trade-off between control complexity and component count is required for a choice to be made between both techniques. Additionally, the integrated converter system was operated with the MPC section in closed loop such that V_{DC} was controlled to 400 V using the closed loop strategy for MPCs described for T_A in paper II [93]. The PI control variables for controlling the modified T_A were heuristically selected, and desired dynamic performance characteristics are achieved. Figure 4.29 presents key measurements obtained from the integrated converter system under closed loop operation of the MPC section. Further, the control-based and circuit-based dc link capacitor voltage balancing techniques were further compared under closed loop operation and the results are presented in Figure 4.30. Again, the circuit-based

balancing technique performs slightly better in equally dividing the dc link voltage across the three capacitors without requiring the complex controller required in the control-based balancing technique. All these results validate the proposed integrated converter system for integrating RESs to both dc and ac grids.

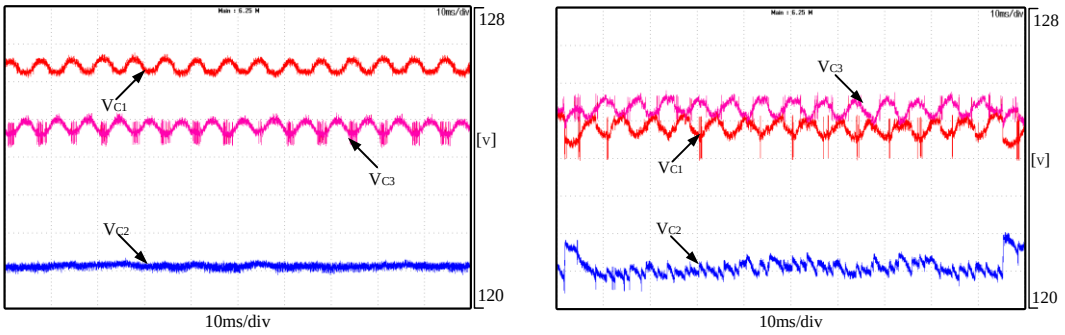


Figure 4. 28: Results of dc link capacitor voltage balancing for (a) control-based and (b) auxiliary circuit-based techniques.

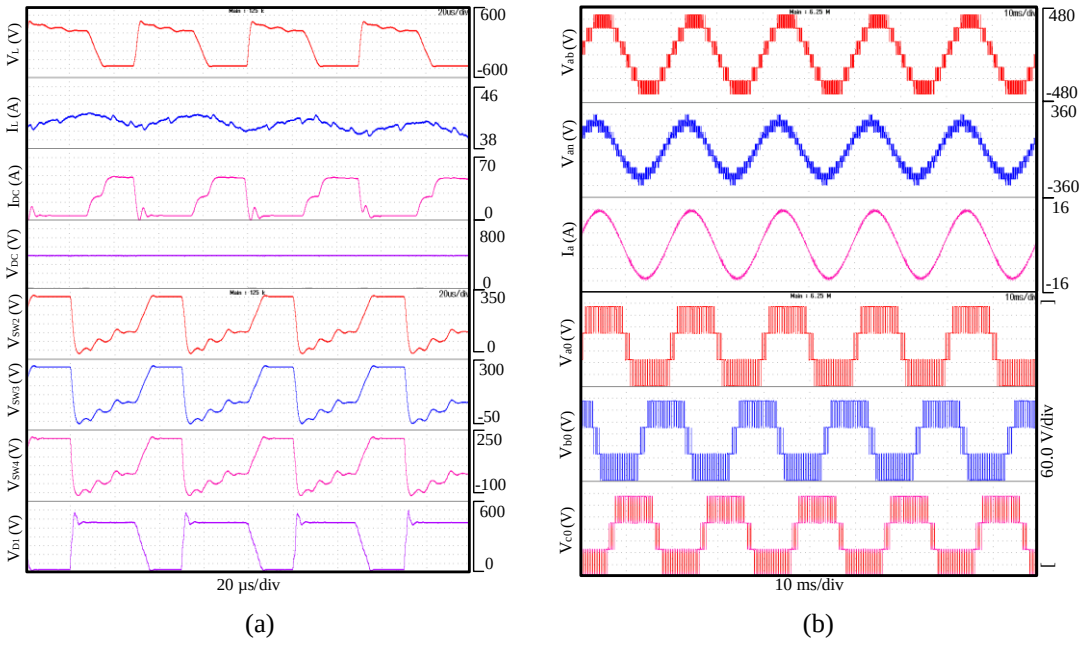
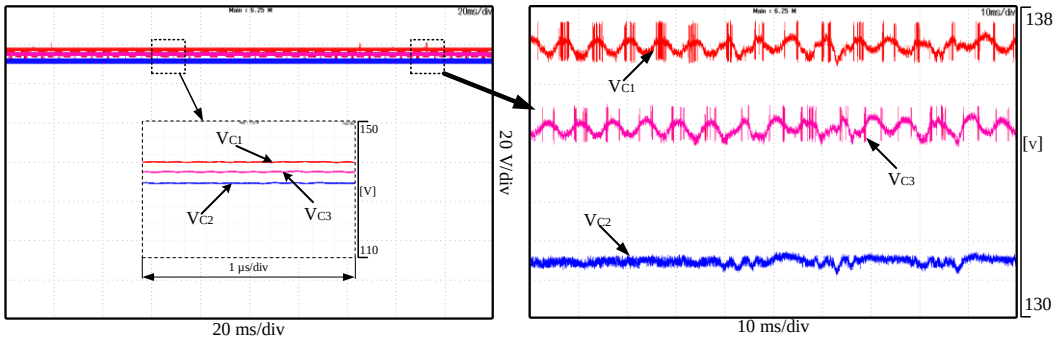


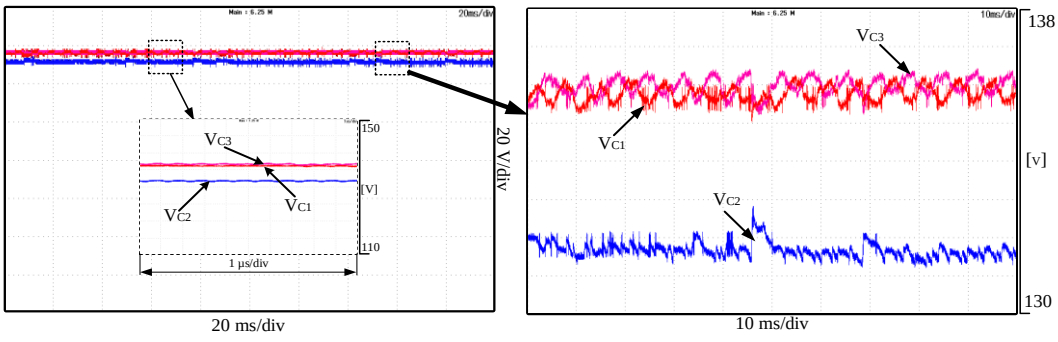
Figure 4. 29: Closed loop implementation results showing (a) key waveforms of the MPC operation and (b) output current and voltage waveforms and the pole voltages.

Lastly, to test the feature of bipolar MPC to ac conversion, T_{D4} was integrated with the MLI proposed in [96] as discussed earlier in Chapter 3. The inputs to the MLI were replaced by the bipolar outputs of the MBDC to create a multi-input MLI. The MLI switches were operated with low frequency modulation as discussed in [96] with three phase *RL* loads connected in wye configuration at the outputs of the MLI. The results of this implementation are presented in Figure 4.31, showing

the currents through the three phases to the loads and the voltages of the bipolar dc link, ac line, ac phase and the poles of the MLI. Although the currents through the phases are varied, the dc link voltage remains constant at about 115 V and ±57 V. The line and pole voltages also remain constant throughout the duration of the disturbance. As expected for wye connected loads, when the currents in all three phases are unbalanced, the phase voltages are disturbed. Further, the total harmonic distortion (THD) of the phase and line voltages were all about 16.83%, while the currents had a THD of about 1.67% all through the different conditions before adding filters. Thus, the applicability of the proposed MBDCs for MLIs and other applications that could potentially cause unbalanced loads at the poles of the dc bus is validated. The voltage balance is achieved without requiring closed loop control, or only 50% duty applied alternately to S_{b1} and S_{b2} was sufficient to keep the output voltages balanced.



(a)



(b)

Figure 4. 30: Results under closed operation of the MPC for (a) control-based and (b) auxiliary circuit-based dc link capacitor voltage balancing.

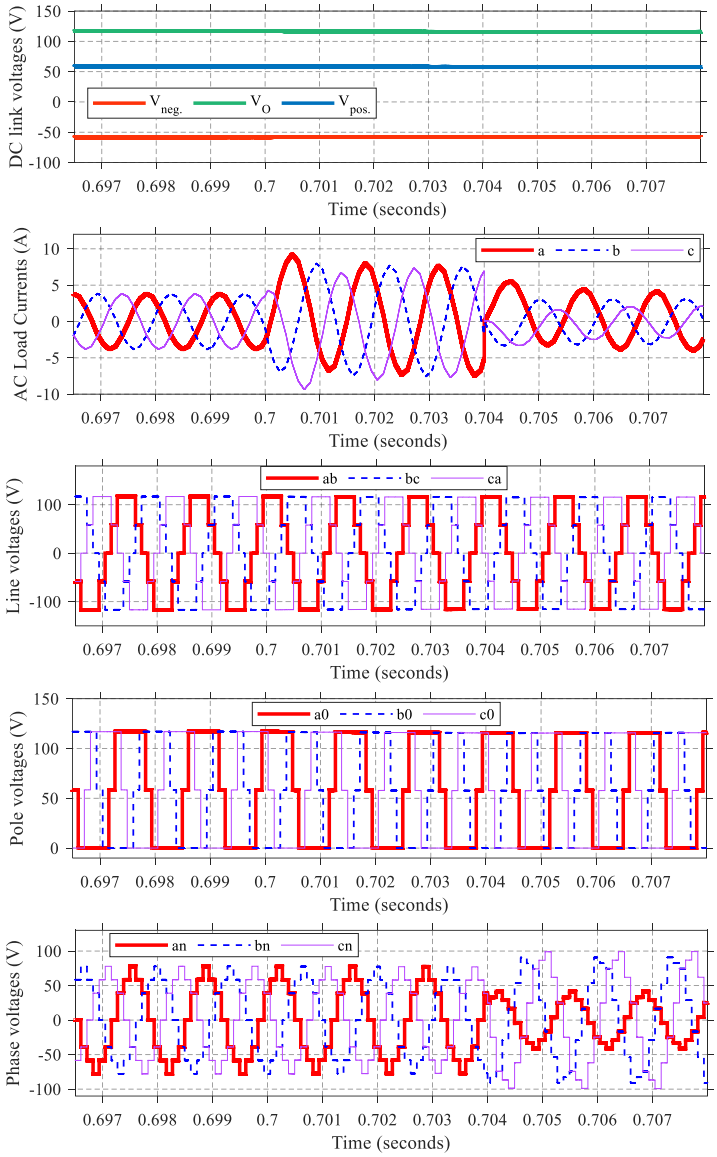


Figure 4. 31: Results of integrating T_{D4} with the MLI in [96] showing the bipolar DC link voltages and the ac stage voltages and current under different load conditions.

4.8 Comparison studies

The MPC topologies proposed in this dissertation are compared to other recently developed MPCs to further highlight the novelty of the proposed MPCs. The summary of these comparison studies are presented in this section, basically presenting the four category of MPC topologies proposed namely, non-isolated and isolated MPCs with unipolar and bipolar outputs respectively. This summarized comparison is based on the studies presented in papers I – IV and VI – VIII. T_A and T_B are compared together since they are both non-isolated and have unipolar outputs, while T_C – T_E is compared separately since their configurations and characteristics are different.

Table 4. 7: Comparison of T_A and T_B with existing non-isolated unipolar MPCs

Parameters		[37]	[36]	[38]	[39]	[32]	[42]	T_B	T_A
Part Count	S	2N	2N	2N+2	N+2	N+1	N+1	N+4	N+3
	D	2N	2N	2N+2	2N+2	N+1	1	0	0
	L	N+1	N	N	N	N	1	2	1
	C	N+1	N+1	1	1	1	N+1	1	1
	T	6N+2	6N+1	5N+5	4N+5	3N+3	2N+4	N+7	N+5
IPF		Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
PFP		No	No	Yes	No	No	No	Yes*	No
SPF		Yes, buck-boost	No	Yes, buck-boost	Yes, boost	Yes, boost	Yes, boost	Yes, buck-boost	Yes, buck-boost
Modular?		Yes	Yes	Yes	No	Yes	Yes	Yes	Yes
Bidirectional?		Yes	Yes	Yes	Yes	Yes	No	Yes*	Yes
Topology		Ćuk	buck-boost	buck-boost	buck, boost	buck, boost	boost	buck-boost	buck-boost
V_{TR}		(3.31)	NR	(3.31)	NR	(3.31)	(3.31)	(3.32)	(3.31)

N=Number of inputs, IPF=Independent power flow, PFP=PF between ports, S=Switch, D=Diode, L=Inductor, C=Capacitor, T=Total, SP=Same with proposed, NR=Not reported.

Firstly, Table 4.7 presents a comparison of T_A, T_B, with some recently developed non-isolated MPCs. It is arranged in descending order of the total component count. Other key parameters are the possibility of bidirectional power flow, simultaneous and independent power flow from the input sources and the topology of operation that is, buck, boost or both buck-boost. For this comparison, when the MPC topology is defined as, buck, boost, this means that the converter is bidirectional and so in one direction it bucks and boosts in the other direction of power flow. The basis for selecting the counterpart MPCs on Table 4.7 for the comparison is their similarity in structure. The MPCs in [36, 39] using a high component count can operate in buck/boost modes, but they do not allow for a simultaneous power transfer from the input ports, or power transfer between ports. The MPCs in [32, 37] require lower component counts as compared to [36, 39], but the power from the input ports can be simultaneously transferred only in the boost mode. The MPC in [42] seems to have competitively low component count as T_A and T_B, but the simultaneous power flow is only possible in boost mode as against the buck-boost simultaneous power flow possible in T_A and T_B. Further, it can be argued that since the current implementation of FBSs require two pairs of MOSFETs, the total component count of T_A and T_B should be higher. However, the T_A and T_B will still require less component count than required in [38], which is the closest competitor in terms of bidirectional buck-boost capabilities with simultaneous power flow possible in buck-boost mode. The MPC in [42] would

have a lower component count than T_A and T_B but it is not bidirectional and only allows for simultaneous power flow in a boost mode. All the compared MPCs have the same V_{TR} except for the MPCs in [36], which is not capable of simultaneous power transfer, and [32] for which the relationship between input and output voltages is not defined. Comparing T_A and T_B, although T_A has a lower component count than T_B, the MPC in T_B is more robust since it allows for power flow between the clusters of energy sources and storages. Further, while T_A can only be used to integrate energy storages to the dc link, T_B can be used to integrate both energy storages and renewable energy sources. Thus, an indication of how T_B improves upon T_A but with the obvious trade-off of two more components.

Table 4. 8: Comparison of T_C with existing isolated unipolar MPCs

Parameters		[22]	[70]	[23]	[24]	[29]	T_C
Part Count	S	6N	8	8	2N+8	N	N
	D	0	8	4	0	1	1
	L	2N-1	2	1	1	N	0
	C	3N-1	1	1	2	N+1	1
	Np	N	2	2	1	1	1
	Ns	N	2	1	1	1	1
	T	13N-2	23	17	2N+13	3N+4	N+4
No. of inputs		N	2	2	N	N	N
Modular?		Yes	No	No	Yes	Yes	Yes
Control		PS-PWM				PWM	PWM
Topology		MAB	Boost	MAB	DAB	Buck-Boost	Buck-Boost
V_{TR}		NR					(3.35)

S = switches, D= diodes, L = inductors, C = capacitors, N_P = number of primary windings, N_S = number of secondary windings, MAB = multi-active bridge, DAB = dual active bridge, NR=Not reported.

Secondly, the comparison of T_C to other isolated MPCs with unipolar outputs is presented on Table 4.8, in order of decreasing component count needed for two input sources, showing the number of possible inputs, component count, control strategy and operation topology. Further, the modularity, that is the possibility of increasing the number of inputs to the MPC without modifying the core of the magnetic component, is also compared. The MPC in [22] is modular, but it has the highest component count, resulting in reduced power density since each input source requires its own transformer. Thus, only the dc bus is shared by the sources and has a complex control strategy requiring PS-PWM. The MPCs proposed in [23, 70] require a lower component count than that of [22] for the same number of inputs, but they have a fixed number of input sources as well as complex control strategy. Further, the MPC in [70] can only operate in boost mode. The component count of the MPCs in [24, 29] is lower than that of [22, 23, 70]. Having no

restriction on the number of input ports, they both require a fixed magnetic component for any number of input ports but the control strategy in [24] is PS-PWM. T_C combines the advantages of [24, 29], by using a fixed magnetic component, without limitations on the number of input ports. Further, it requires a smaller number of components and still has a simple control strategy, thus underscoring its superiority over existing topologies.

Table 4. 9: Comparison of the T_D with existing non-isolated bipolar MPCs.

Parameters		[48]	[47]	T_{D1}	T_{D4}	T_{D2}	T_{D5}	T_{D3}
Part Count	S	2	3	N+1	N+3	N+1	N+3	N
	D	4	4	5	2	8	5	7
	L	1	3	1	2	2	3	2
	C	3	6	4	2	4	2	4
	T	10	16	N+11	N+9	N+15	N+13	N+13
No. of inputs		2	2			N		
IPF		*Partially	*Partially	Yes	Yes	Yes	Yes	Yes
PFP		No	$^{+}$Partially	No	No	No	No	No
SPF		Yes, boost		Yes, buck-boost		Yes, boost	Yes, boost	
Modular?		No	No	Yes	Yes	Yes	Yes	Yes
Output voltage symmetry		Complex closed loop	Inherently symmetrical		Open loop control	Inherently symmetrical	Open loop control	Inherently symmetrical
V_{TR}		$1/\left[0.5+\frac{1-\beta}{2}\right]$	$1/(1-\beta)$			(3.36)		

N=Number of inputs, IPF=Independent power flow, PFP=PF between ports, SPF=Simultaneous PF, S=Active switch, D=Diode, L=Inductor, C=Capacitor, T=Total, *=IPF is only possible from the second input port, $^{+}$=PFP is only possible from the first to the second input port and not vice versa, Sw.= Switching.

Thirdly, Table 4.9 presents the comparison of the MBDCs in T_D with the recently proposed non-isolated MBDCs in [47, 48]. The basis for selecting these MBDCs for comparison is that, to the best of our knowledge, they are the only existing non-isolated MBDCs in literature at the time of preparing this dissertation. Table 4.9 is arranged in the order of increasing voltage gain (expressed as V_{TR}) when the MBDCs are operating under simultaneous power flow from more than one input to the bipolar dc link. All the MBDCs in T_D have a higher V_{TR} than their counterparts with T_{D3} having the highest V_{TR}. T_{D1} and T_{D4}, having the lowest V_{TR} among the MBDCs in T_D, are two times higher than the V_{TR} obtainable in [47], with [48] offering the overall lowest V_{TR}. The bipolar output voltages proposed in T_{D1} to T_{D3} as well as [47] are inherently symmetrical, and thus do not need a control system keep the voltages balanced. While a complex closed loop system is required in [48], a simple open loop control of 50% duty cycle is required in T_{D4} and T_{D5}.

Further, the modularity of the converters should be taken into comparison, since this proves the possibility of expanding the number of input ports without modifying the structure of the MBDCs. All the MBDCs in T_D are modular, and thus their number of inputs can be increased arbitrarily, but both MBDCs in [47, 48], have the maximum number of two inputs. Finally, the independent power flow (IPF) can be carried out arbitrarily from any of the inputs of the proposed MBDCs to the outputs, but the existing MBDCs can achieve IPF in the second input alone. Although the MBDC in [48] has the lowest total component count, it also features the lowest V_{TR}, while the MBDCs in T_D have competitive number of components with the significantly higher V_{TR}.

Lastly, Table 4.10 presents the comparison of T_E with the recently proposed isolated MPCs with bipolar outputs in [49, 50]. The basis for selecting these MIBDCs for comparison is that, to the best of my knowledge, they are the only existing MIBDCs in literature. Table 4.10 is arranged in the order of increasing part count, when considering two inputs to the MIBDCs. The proposed MIBDC in [49] has the lowest part count by just 1 but its' output voltage is not inherently symmetrical. Therefore, a further controller is required to maintain the voltage symmetry on the bipolar outputs. For two inputs, the MIBDCs proposed in this paper has the same part count and symmetrical characteristics as the MIBDC in [50], but it has a key advantage of modularity such that the number of input ports can be arbitrarily increased just by introducing one additional reverse blocking switch. Further, the MIBDCs proposed in [49, 50] both have a limitation on number of inputs and low voltage gain, in which the MIBDCs in this paper are triumphant. Finally, IPF can be carried out arbitrarily from any of the inputs of the proposed MIBDCs to the outputs, but the existing MIBDCs can achieve IPF from the second input alone.

Table 4. 10: Comparison of T_E with existing isolated bipolar MPCs.

Parameters		Part Count						No. of inputs	IPF	SPF	Modular?	Output voltage-symmetry	Soft switching
		S	D	L	C	Tx	T						
[49]		6	2	3	2	1	14	2	No	Yes	No	Asymmetrical	ZCS+ZVS
[50]		6	4	2	2	1*	15	2	No	Yes	No	Symmetrical	ZCS+ZVS
T_E	DAB	N+8	0	1	3	1*	N+13	N	Yes	Yes	Yes	Symmetrical	ZCS+ZVS
	FB	N+4	4										

N=Number of inputs, IPF=Independent power flow, PFP=PF between ports, SPF=Simultaneous PF, S=Active switch, D=Diode, L=Inductor, C=Capacitor, Tx=Transformer, T= Total, *=IPF is only possible from the second input port, $^{+}$=PFP is only possible from the first to the second input port and not vice versa, Sw.= Switching.

Chapter 5

5 Concluding remarks

5.1 Conclusions

This dissertation focuses on proposing MPC topologies for hybrid energy systems to fill the gap in the pre-existing MPC topologies, which are characterized by high component count, low voltage gain, and a rather complex control mechanism. Reducing component count while increasing voltage gain and reducing control complexity have become a crucial matter in the development of new MPCs. Within this framework, five (T_A to T_E) novel MPCs were proposed in this dissertation. The novel MPCs proposed broadly cover the four different categories of MPCs namely, isolated (T_C) and non-isolated (T_A and T_B) MPCs with unipolar outputs and the isolated (T_D) and non-isolated (T_E) MPCs with bipolar outputs. The proposed MPCs were theoretically analyzed, verified numerically and validated experimentally in the in-house experimental test bench.

Non-isolated MPCs have gained popularity due to their reduced size, cost-effectiveness, and ease of miniaturization. However, as highlighted in Section 2.2, pre-existing non-isolated MPCs have certain limitations. Some can only allow power flow from input ports with simultaneous power flow in boost mode only. Others require additional inverter legs and inductors for each additional input port, increasing board footprint and cost. Although some non-isolated unipolar MPCs have lower component counts, they can only transfer power simultaneously in boost mode. These inadequacies underscored the need for the novel non-isolated MPC topologies that exhibit reduced component count, being capable of simultaneous and individual power transfer, and power flow between input ports. In the non-isolated MPC developed as T_A, inductor time-multiplexing was used to achieve simultaneous power flow from the inputs of the MPC. In addition to this, a SISO controller was adapted for output voltage control as opposed to the conventional use of a MIMO control structure, which has a higher complexity. Further, a novel voltage transformation factor to compare the voltage gain of MPCs during simultaneous power transfer was introduced during the development of T_A. To improve upon the features of T_A, T_B was developed with a key feature of

hybridising both energy sources and storages and the ability to independently transfer power from the energy sources to the storage.

The existing isolated unipolar MPCs discussed in Section 2.2 have a limitation on the number of input sources and require a complex control strategy that necessitates phase shifted pulse width modulation (PS-PWM). Some of these MPCs are limited to being capable of operating only in boost mode. While some of these MPCs require a fixed magnetic component for any number of input ports, the semiconductor component count is high, and the control strategy is complex, needing PS-PWM to regulate the dc link voltage. Therefore, it was crucial to develop an isolated MPC with a unipolar output, without restrictions on the number of input ports, by using a fixed magnetic component for galvanic isolation, requiring a simplified control strategy, and reducing the number of components even further. The isolated unipolar MPC, T_C, in this thesis being a flyback based MPC, solves the problem of component count by requiring a fixed core for any number of inputs. This was achieved by taking advantage of the possibility to time multiplex the charging of its magnetizing inductance. By so doing, only few semiconductor components are required such that only one switch is required to introduce a new input port to the MPC. This MPC can be implemented for energy harvesting in PV farms and other renewable energy systems.

From the study of literature in Section 2.3, there are far fewer non-isolated MPCs with bipolar outputs as compared to the unipolar counterparts. Nevertheless, these few MPCs have limitations such as being restricted to only two inputs and being unable to facilitate arbitrary independent power flow from either of the input sources to the bipolar dc bus. This is apart from their low voltage gain and high component count feature and the need for complex control to achieve balanced symmetric output voltages. Therefore, it was crucial to develop and validate non-isolated MPCs with bipolar outputs that have a high voltage gain, low control complexity or natural bipolar symmetry, and modularity such that the number of input ports can be expanded without restriction. As a solution to these limitations, T_D, a family of five (T_{D1}-T_{D5}) novel non-isolated MPCs with bipolar symmetric outputs were developed and validated for integrating multiple renewable energy sources to bipolar dc grids. These MPCs have key merits of high voltage transformation factor (i.e. high voltage gain) and naturally symmetrical bipolar outputs or requiring a simple open-loop PWM control of 50% duty cycle to keep the output voltages balanced. Further, the number of input ports can be arbitrarily

increased to accommodate more renewable energy resources, which was impossible in pre-existing non-isolated bipolar MPCs.

In addition to the limitations of non-isolated bipolar MPCs earlier discussed in Section 2.3, they pose safety risks due to the lack of magnetic isolation. Hence, isolated MPCs with bipolar outputs, which offer magnetic isolation and soft switching are a good candidate to solve this problem as discussed in detail in Section 2.4. However, they also have limitations in terms of a fixed number of inputs and surprisingly low voltage gain just like their non-isolated counterparts. Furthermore, there are few isolated MPCs with bipolar symmetric outputs proposed in literature compared to their unipolar counterparts, just like the case of the bipolar non-isolated MPCs. Moreover, they require complex control to maintain symmetric output voltages under unbalanced loads and do not allow for arbitrary independent power flow from input ports to the bipolar dc bus. Therefore, to address these limitations, T_E, a novel isolated MPC with bipolar symmetric outputs based on dual active bridge and phase-shifted full bridge topologies was developed. The operation of this MPC in independent and simultaneous power transfer from the sources to the dc link in open and closed loop was demonstrated. Further, the features of reliability under critical unipolar loads and natural symmetry of the dc link under unbalanced loads, which are two very vital features of bipolar converters, were demonstrated and verified. This isolated bipolar MPC can be implemented for energy harvesting in PV farms and other renewable energy systems with DC voltage sources.

Finally, the growing use of renewable energy sources (RESs) has caused a shift from centralized to distributed generation systems. AC power systems are still prevalent in many conventional power systems, so the conversion of dc power generated from RESs to ac power is necessary. The traditional two-level inverter is commonly used but has several drawbacks, such as high switching losses and total harmonic distortion (THD). To address these issues, multilevel inverters (MLIs) have become a popular solution due to their appealing features, including low switching losses, low THD, and smaller filter components. However, many existing MLI topologies assume constant dc inputs, being impractical in applications as RESs, have varying output voltage during operation. Some MLI topologies have been proposed to pre-process the power from RESs to provide boosting features to the AC output, but they have limitations, including restrictions on the number of RESs that can be integrated, high component count, power losses, higher system cost, and low power density. Moreover, the introduction of multiple

RESs can create the issue of dc link capacitor voltage balancing, which requires a complex control system to achieve balanced dc link voltage across the capacitors. To this end, some of the MPCs proposed in this dissertation were integrated with existing MLIs to achieve seamless conversion of dc to ac power. Specifically, a modified version of T_A was used to integrate RESs directly to an ac grid by converting unipolar dc to ac as detailed in Section 3.6.2. Two methods of capacitor balancing were examined: one based on introducing an auxiliary circuit and the other by modifying the controller of the MLI. Both methods achieved desirable results as there were no significant differences in their performance in adequately balancing the dc link capacitor voltage. Furthermore, the bipolar MPCs proposed in this dissertation presented the opportunity to adequately balance the dc bus without requiring a complex control system for balancing DC link capacitor voltage. Consequently, T_{D4}, was integrated with another existing MLI as detailed in Section 3.6.3. This was done to achieve seamless integration of RESs to ac grid without requiring additional auxiliary circuit or complex controller to balance the dc link capacitor voltage. Lastly, the integration of RESs for critical loads in dc grids was demonstrated by integrating a bipolar to unipolar dc converter as detailed in Section 3.6.1. This was done to achieve constant supply of energy to critical dc loads in the event of failure or open circuit faults in any line of the bipolar dc lines.

5.2 Limitations and future work

This dissertation has two key limitations: maturity of the component market (that is, market maturity of materials) and the experimental implementation. An improvement in these key areas could further foster the adoption of these MPC topologies and could also provide opportunities for further research in MPC topologies.

On the aspect of the market maturity of the devices or materials, the MPCs introduced in this research utilize some power electronic switch components such as the reverse blocking and bidirectional (four quadrant) switches. Development of monolithic reverse blocking and fully bidirectional switches has been fairly slow as compared to other type of switches. Although a lot of research has been carried out in their regard, market-ready options are quite limited. To mitigate this limitation, multiple switches were combined to achieve the desired switching characteristics. This could have a negative impact on the MPC's overall efficiency, therefore, it is imperative that the use of monolithic devices be explored in the future. Further, on the aspect of material, T_C is based on the traditional flyback

topology, which has a power density limitation based on the core material implemented in the isolation (that is, the coupled inductor or flyback transformer). This power limitation hampers the implementation of T_C for high power (> 500 W) applications, thus, improving the quality of core material will further enhance the features of T_C and more importantly, open their range of applications.

Due to the limited time and resources available, the experimental implementation of the MPCs was carried out on a reconfigurable switch bank thanks to our flexible in-house validation setup. This is instead of building a product ready prototype for each MPC topology, which would have been time and resource consuming such that only one MPC could have been proposed and validated. This limitation meant that the efficiency of the MPCs could not be adequately assessed and other tests such as the electromagnetic interference (EMI) characteristics could also not be investigated. Future work could focus on building product level prototypes to further investigate some of these characteristics.

Further, verification of all the MPC topologies (T_A to T_E) has been carried out within a laboratory environment. There is need to further validate these topologies under field applications to stress test the topologies and more adequately assess their performance characteristics. Additionally, these topologies have been validated experimentally for power applications less than 2.5 kW. It could be interesting to see the benefits of the proposed MPCs sustained for much higher power (> 10 kW) applications.

On the aspect of application, while T_A and T_B can be used for energy storages, with T_B being cable of integrating energy sources as well, T_C to T_E can only be used for energy source integration. This is because T_C to T_E are unidirectional MPCs. Further, while power flow between clusters is possible in T_B, the possibility of power flow between input ports is a challenge in T_A. Moreover, although there is no limit to the number of input ports to all the proposed MPCs, the verification of these MPCs was done with only two inputs in most cases. Except for T_B which was verified for four inputs but with two inputs per cluster. Further tests could be carried out to examine their performance with an arbitrarily larger number of inputs.

Overall, these limitations did not negatively impact the viability of the proposed MPCs but rather, present a unique opportunity for key industry and research stake holders to further provide solutions that could be vital to the future of MPCs and dc converters at large.

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Appendices

Paper I:
Four Quadrant Switch Based Multiple-Input DC-DC Converter

This paper has been published as:

I. N. Jiya, H. Van Khang, N. Kishor and R. Ciric, "Four Quadrant Switch Based Multiple-Input DC-DC Converter," *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia),* Singapore, Singapore, 2021, pp. 2199-2204, doi: 10.1109/ECCE-Asia49820.2021.9479432.

Four Quadrant Switch Based Multiple-Input DC-DC Converter

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***Abstract*-- In this paper, a novel non-isolated multiple input dc-dc converter (MIC) is proposed. The MIC uses four-quadrant switches, only one inductor and capacitor. It is capable of bidirectional operation in non-inverting buck-boost configuration and can accommodate the simultaneous transfer of energy from more than one source of different voltage levels to the DC bus. This MIC is analysed for two inputs in this paper. As compared to existing MICs in literature, the proposed converter utilizes less number of inductors and requires only one switch to integrate any extra energy storage. Different operation modes of the proposed MIC are numerically verified and validated on a high-fidelity hardware-in-the-loop (HIL) device.**

Index Terms—Bidirectional DC-DC power converter, buck-boost, four quadrant switch, multiple input converter.

I. INTRODUCTION

Energy storage seems to be the biggest challenge in the advancement towards renewable or green energy solutions. Thus hybridisation of energy storage has been the theme of many of the research in this field [1]; as it is an effective and economic solution towards improving the performance of renewable energy systems. The application of hybridised energy storage systems cannot be overemphasized. It finds relevance in a wide area of applications ranging from DC micro grids, energy storage backup for communication systems to electric vehicles of any kind. Implementation of efficient and effective utilisation of renewable energy technologies arguably cannot be achieved devoid of DC-DC converters [2]. Using single input converters to integrate multiple energy sources results in the bulkiness, unnecessary complex configuration, and high cost [3]. To address these problems, both isolated and non-isolated multiple input converters (MICs) have

been proposed in literature as a promising solution to deal with high penetration of diverse renewable energy resources [4], [5].

Some of the major advantages of MICs with isolation is the galvanic isolation, which is required for certain hybrid power systems and high voltage gains [6]. Isolated MICs are usually complex to control and bulky due to the galvanic isolation through magnetic components [7]. The non-isolated MICs present some peculiar advantages over the magnetically connected MICs, for example, the reduced size and ease miniaturization, resulting in reduced cost and complexity.

Although more efficient non-isolated MICs have been proposed as in [8], they either trade off part counts for robustness and complexity or vice-versa. Developing highly efficient and robust MICs is very important in hybrid energy storages to facilitate energy source and storage hybridisation [9]. Further, the wide band gap (WBG) technologies such as SiC and GaN switches present new opportunities for the design of MICs [10].

In this research, a new multiple input dc-dc converter is proposed to balance among component count, robustness, and complexity through bidirectional devices. The proposed MIC is capable of bidirectional operation in non-inverting buck-boost configuration and can transfer simultaneously multiple energy resources of different voltage levels to the DC bus while requiring fewer components as compared to other existing converters in literature. The operation of the converter is numerically verified and validated using high-fidelity real-time simulator or hardware-in-the-loop (HIL).

II. PROPOSED MIC TOPOLOGY

Fig. 1 presents the proposed bidirectional MIC, consisting of one inductor, one capacitor and fully controllable bidirectional switches (FBSs). FBSs, also known as AC switches, bilateral switches, four-quadrant switches, or matrix switches, can

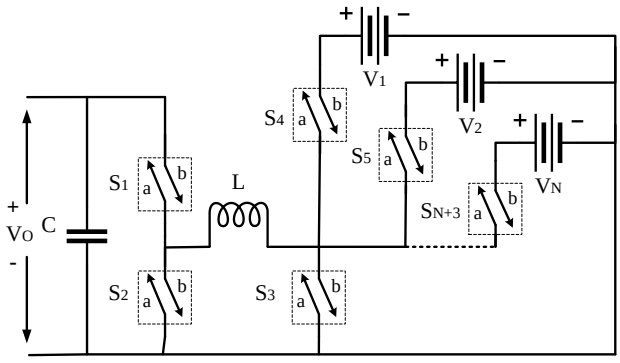


Fig. 1. The proposed MIC for integrating multiple energy storage devices into the microgrid using a single inductor and four-quadrant switches for N-number of inputs.

control ON-state current and OFF-state voltage bidirectionally [11]. FBSs consist of two gates which direct the flow of current through the switch. To achieve the ideal switching FBSs, two unidirectional switches (MOSFET or IGBTs with their respective anti-parallel diodes) are connected in anti-series configuration. However, new monolithic FBSs, using two reverse blocking IGBTs (RB-IGBTs) connected in anti-parallel can eliminate two discrete anti-parallel diodes as required in the conventional FBS [12]. The FBSs make the proposed MIC robust and allow for bidirectional power flow between the DC bus and the energy storage systems. This MIC is also capable of bucking and boosting the input voltage in all operation modes. Conventional MICs require n inductors required for *N* input sources and two additional switches [13], but the proposed MIC utilizes only one inductor and capacitor for any input sources. It needs only one additional FBS when introducing an input port.

Five operation modes of the proposed MIC are analysed in this section. The switching pattern for these modes are presented on table I. The first four modes (A-D) describe the interaction between the DC bus and the two energy storage devices V_1 and V_2. While mode E represents the situation in which both energy storages V_1 and V_2, are supplying the DC bus simultaneously. The operation of the converter in modes A to D is illustrated in Fig. 2, and the associated continuous conduction mode (CCM) waveforms in steady state is shown in Fig. 3. The switching period T_s is divided into two, T_1 and T_2, for the inductor charging and discharging periods, respectively, in four operation modes. These modes are basically the standard non-inverting buck-boost converter. Using the volt balance analysis on the steady state waveform of the converter presented in Fig. 3, it can be observed that this converter can operate in the buck or boost modes depending on the duty ratio '*D*' applied across the switches. Where *D* is the ratio of the inductor charging time to the total switching period, that is $D = \frac{T_1}{T_S}$. Therefore, the conventional equations (1 – 4) describing the relationship between the input and

TABLE I
CONDUCTION SEQUENCE OF THE SWITCHES IN EACH MODE OF OPERATION

Modes	T_1	T_2
A	S_{4b} S_{2b}	S_{1a} S_{3a}
B	S_{5b} S_{2b}	S_{1a} S_{3a}
C	S_{1b} S_{3b}	S_{4a} S_{2a}
D	S_{1b} S_{3b}	S_{5a} S_{2a}
E	S_{4b} S_{5b} S_{2b}	S_{1a} S_{3a}

output voltage of the basic buck-boost converter applies to this converter as well for modes A to D respectively.

$$V_O = \frac{T_1}{T_2} V_1 = \frac{D}{1-D} V_1 \tag{1}$$

$$V_O = \frac{T_1}{T_2} V_2 = \frac{D}{1-D} V_2 \tag{2}$$

$$V_1 = \frac{T_1}{T_2} V_O = \frac{D}{1-D} V_O \tag{3}$$

$$V_2 = \frac{T_1}{T_2} V_O = \frac{D}{1-D} V_O \tag{4}$$

In mode E, both energy storages V_1 and V_2 are simultaneously supplying the DC bus as illustrated in Fig. 4. This mode is required when the power requirement by the DC bus cannot be satisfied by only one energy storage. In such cases two or more energy storages are required to supply the required energy simultaneously. Within this mode, the inductor charging period, T_1 is further subdivided into two or more, depending on the number of simultaneous input sources. This study analyses two inputs for the proposed MIC. During time T_1, switches S_{4b}, S_{5b} and S_{2b} are all switched ON. However, in the first subdivision of T_1, the voltage across the inductor is the highest source voltage V_1, therefore the inductor charges with a gradient of $\frac{V_1}{L}$. When the first subdivision period of T_1 is over, S_{4b} is turned OFF while S_{5b} and S_{2b} remain ON. In the second subdivision of T_1, the voltage across the inductor becomes V_2 while the inductor continues to charge with a gradient of $\frac{V_2}{L}$. This process will continue for a MIC with more than two inputs in the decreasing order of the magnitude in their input voltages. When the inductor charging period is over, S_{5b} and S_{2b} are turned OFF, being immediately followed by the discharging period T_2. During T_2, the inductor L discharges through the capacitor C to the DC bus by switching ON S_{1a} and S_{3a}, so the voltage across the inductor becomes $-V_o$, while the inductor discharges with a slope of the sum of the input voltages during their respective ON time divided by the inductance, which is the sum of the effective voltages across the inductor multiplied by the inverse inductance of the inductor. The effective voltage across the inductor from each energy storage is given by the product of the effective ON time of that energy storage and its voltage magnitude. As shown in Fig. 5, this effective voltage is $D_{1eff}V_1$ for the first subdivision of the inductor charging time and $D_{2eff}V_2$ for the

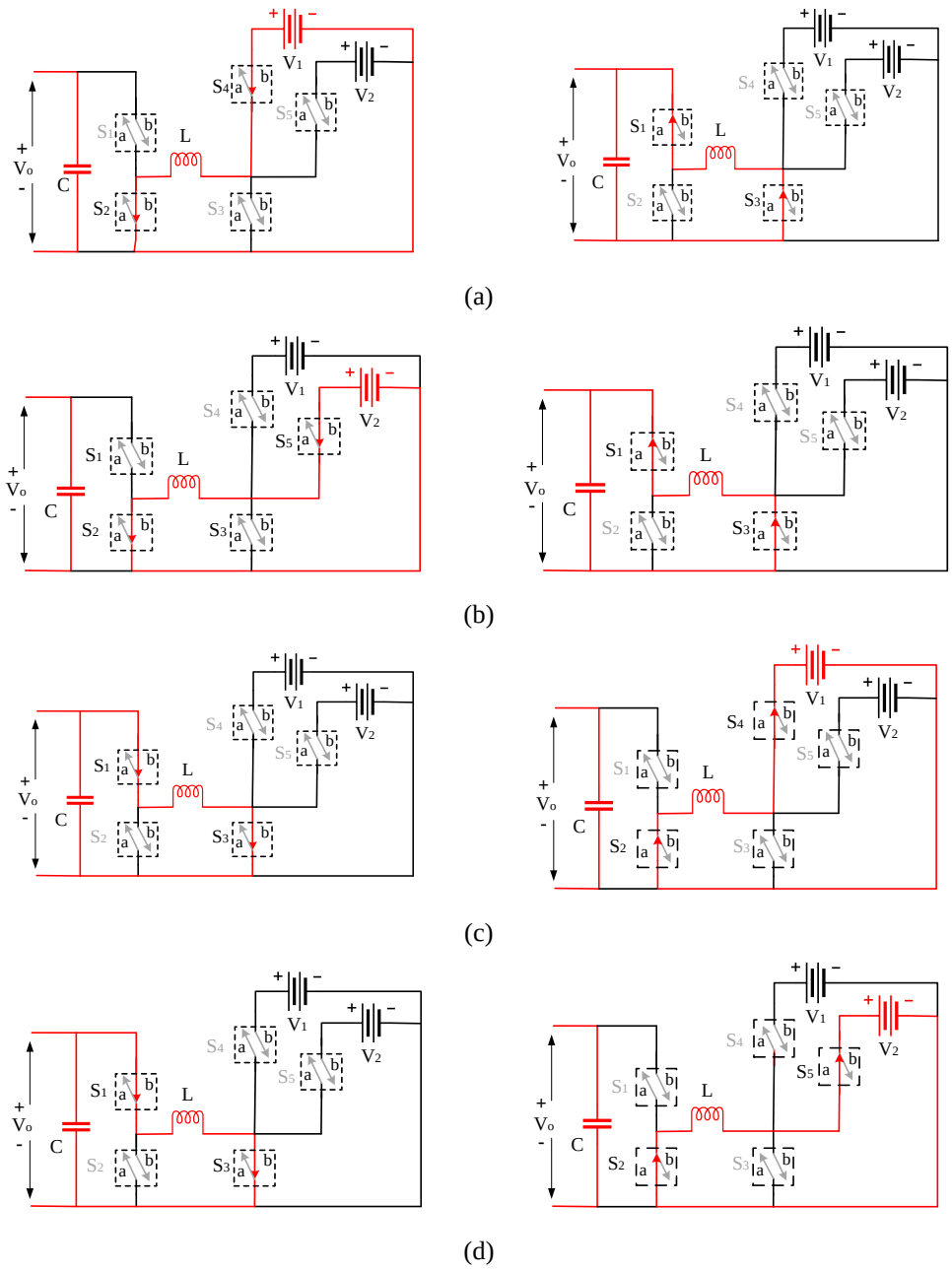


Fig. 2. Illustration of the path of current flow in the converter during the charging and discharging action of the inductor for operation in (a) Mode A, (b) Mode B, (c) Mode C and (d) Mode D.

second subdivision. Therefore, the inductor will discharge with a gradient of $\left(D_{1eff}V_1 + D_{2eff}V_2\right)/L$ during T_2.

For an effective commutation of the switches in mode E, some principles need to be respected in order to achieve simultaneous power transfer to the load. Scenario 1 is denoted as mode E_1 in Fig. 5 when the voltages are unequal. If the magnitude of the sources is arbitrarily arranged in order of increasing magnitudes such that $V_1 > V_2 > \cdots > V_N$ for N input ports, the duty cycles of the PWM signals of controlling the input sources, e. g S_{4b} and S_{5b} in the two input converter, must be

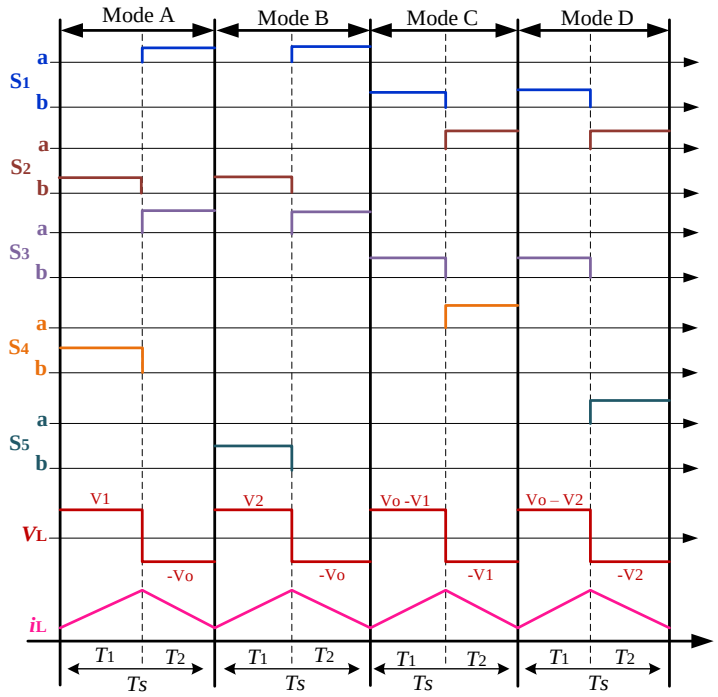


Fig. 3. Steady state waveforms of the MIC operation in CCM for modes A to D.

in such a way that $D_1 < D_2 < \cdots < D_N$, and vice versa, where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, … , $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. However, if the source magnitudes are equal or $V_1 = V_2 = \cdots = V_N$ for N input ports as denoted by mode E_2 in Fig. 6, duty cycles of the PWM signals must be in such a way that $D_1 = D_2 = \cdots = D_N$ in order to achieve equal power delivery from the sources. If the required power delivery from the sources is unequal, $D_1, D_2, \ldots, D_N$ can be determined in order of increasing magnitude from the respective sources.

Furthermore, by applying the volt-second balance to the steady state waveform in Fig. 6, the relationship between the input sources and the output voltage is given by (5) and (6) for N number of input sources and a two input MIC respectively. But if the magnitudes of the input sources are equal such that the converter is operating in mode E_2, and the duty cycles are equal, the relationship between the input and output voltage is given by (7). However, if the voltage of sources are equal but the duty cycles unequal, the relationship between input and output voltage is given by (8), where: $V_{in} = V_1 = V_2$ $D_{max} = max.(D_1, D_2)$.

$$V_O = \frac{\sum_{i=1}^{N}\left(D_{(i)eff} V_i\right)}{1 - \sum_{i=1}^{N} D_{(i)eff}} \tag{5}$$

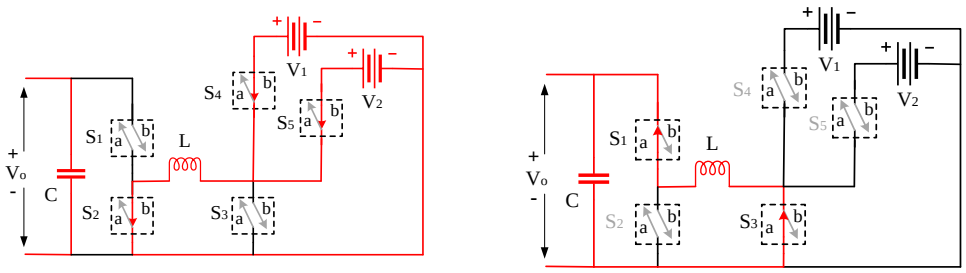


Fig. 4. Path of current flow in the MIC during the charging and discharging of the inductor for simultaneous power transfer from V_1 and V_2 to the DC bus.

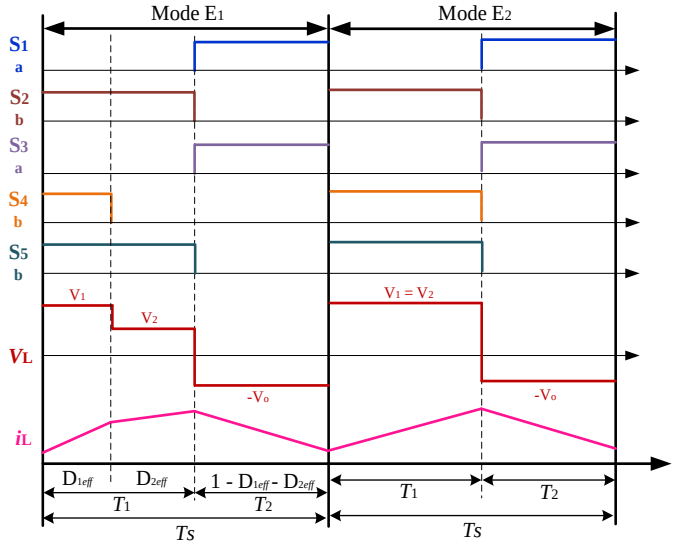


Fig. 5. Steady state waveform of the MIC operation in mode E (simultaneous power transfer from V_1 and V_2 to the DC bus) when V_1 is greater than V_2, and when V_1 and V_2 are equal.

$$V_O = \frac{D_{1eff}V_1 + D_{2eff}V_2}{1 - D_{1eff} - D_{2eff}} \tag{6}$$

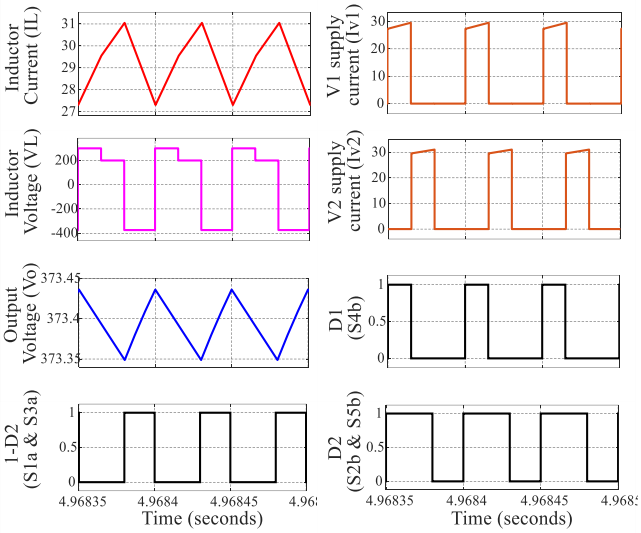
$$V_O = \frac{T_1}{T_2}V_{in} = \frac{D}{1-D}V_{in} \tag{7}$$

$$V_o = \frac{D_{\max}}{1 - D_{\max}} \cdot V_{in} \tag{8}$$

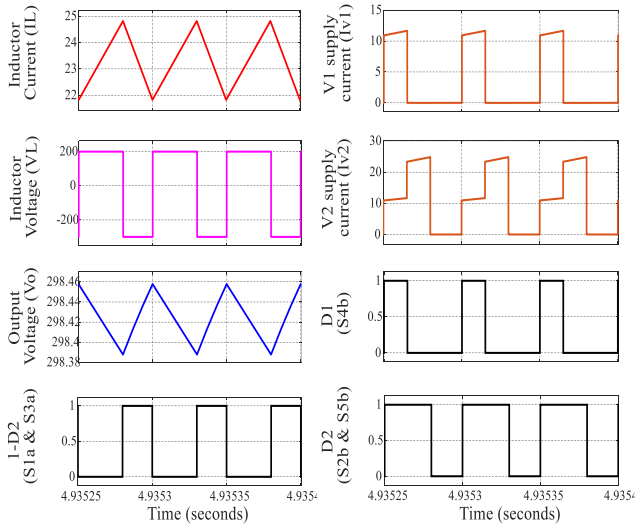
III. RESULTS

The proposed MIC topology was verified in simulation and validated by HIL real-time simulator using OPAL-RT's OP5700 device running a 64bit virtex-7 FPGA. It was controlled from an Imperix's B-box 3.0 also a kintex grade FPGA controller. A design was done for a 5 kW MIC, the parameters of L and C for the verification and validation are 2 mH and 4 mF, respectively.

Open loop simulations were performed by operating the MIC in all operation modes at different duty cycles. More interestingly, the converter was operated in mode E, which represents the simultaneous power flow from both energy storages to the DC bus. Two different scenarios were considered in this study. The first scenario result is presented in Fig. 6 (a) when both energy storages had different voltage levels, being controlled using two different duty cycles to allow for the simultaneous power flow. The second scenario is characterized by the two energy storages having equal voltage levels. In this scenario, the duty cycles, D_1 and D_2, of the switches controlling the energy storages are 0.3 and 0.6, respectively, as in the first scenario.



(a)

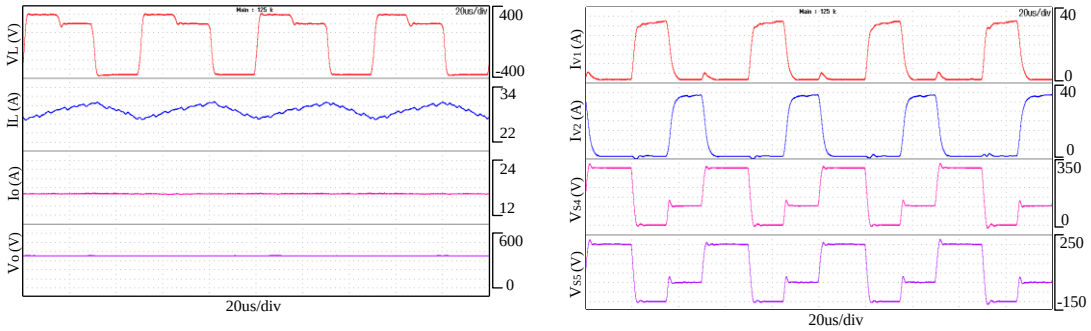


(b)

Fig. 6. Simulation results for mode E with (a) V_1=300V, V_2=200V, (b) V_1=V_2=200V, and D_1=30% and D_2=60% in both cases.

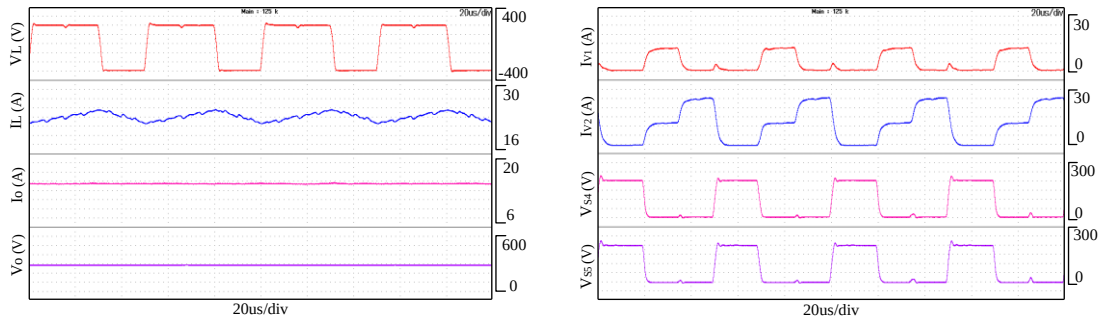
Both input voltages and duty cycles are unequal as shown in Fig. 6 (a), so the energy supplied by both energy storages are unequal. Although the voltages of V_1 and V_2 in Fig. 6 (b) are equal, the duty cycles are different, so less energy is supplied by V_1. It is seen from these scenarios that the duty cycle not only affects the output voltages but also the current supplied by the respective sources, and consequently the energy delivered by the sources. The filter components, *L* and *C*, are also selected to generate the output voltage ripple being less than 20 mV while the inductor ripple current is also under 20%.

Figs. 7 and 8 show the results of HIL tests at the same conditions as in simulations. The voltages across the switches S_4 and S_5 are presented, which control the energy flow from the energy storages. The ripple of the output voltage is about 1 V, and the inductor ripple current is at about 25%. Fig. 7 (b) shows the supplied currents I_{V1} and I_{V2} from energy storages V_1 and V_2, respectively, matching well with the simulation results in Fig. 6 (a). Although both V_1 and V_2 are equal as shown in Fig. 8 (b), the duty of V_{S5} is greater than that of V_{S4}, so the average current supplied by V_1 is 5.6 A, which is less than the average current supplied by V_2 at about 10.2 A.



(a) (b)

Fig. 7. Experimental results in mode E: V_1=300V, V_2=200V, D_1=30% and D_2=60% with (a) Inductor voltage, V_L, Inductor current, I_L, Output current, I_O, Output voltage, V_O and (b) Current supplied by V_1, I_{V1}, Current supplied by V_2, I_{V2}, Voltage across S_4, V_{S4}, Voltage across S_5, V_{S5}.



(a) (b)

Fig. 8. Experimental results in mode E, V_1=V_2=200V, D_1=30% and D_2=60% with (a) Inductor voltage, V_L, Inductor current, I_L, Output current, I_O, Output voltage, V_O, and (b) Current supplied by V_1, I_{V1}, Current supplied by V_2, I_{V2}, Voltage across S_4, V_{S4}, Voltage across S_5, V_{S5}

Fig. 9 shows voltage transformation ratios $V_{TR} = V_O \Big/ \left(\sum_{i=1}^{N} D_{(i)eff} V_i \right)$ obtained from analytical calculations, simulations, and HIL tests for different combinations of V_1, V_2 and their respective duty cycles D_1 and D_2. Fig. 9 (a) presents the V_{TR} in mode A, showing that at duty cycles below 50%, V_{TR} is less than 2 and vice-versa. This proves that the proposed MIC is bucking when the V_{TR} of the MIC is less than 2 and boosting when V_{TR} is greater than 2. In Fig. 9 (b), D_1 is kept constant at 30%

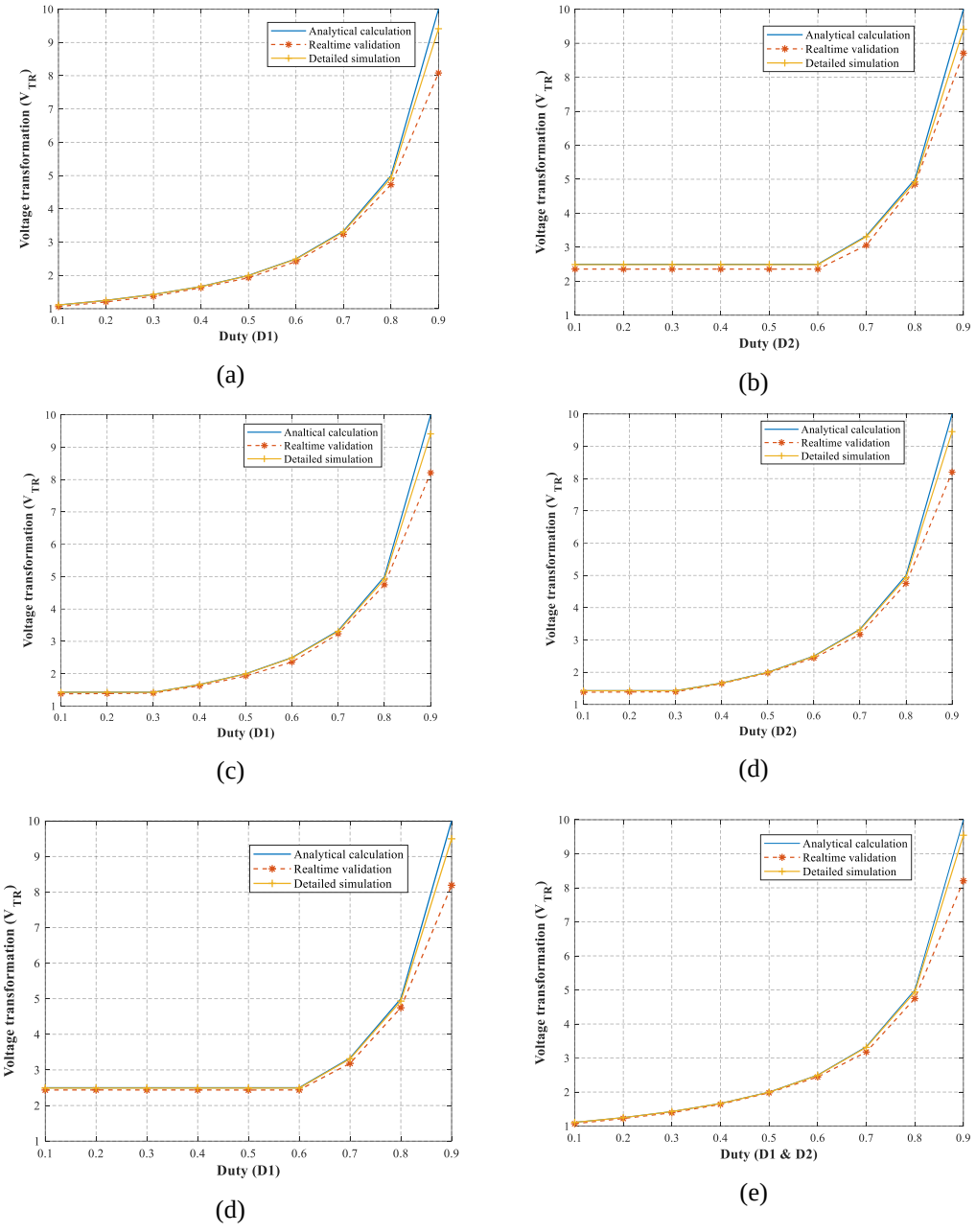


Fig. 9. Obtained V_{TR} from analytical calculation, simulation and experimental validation results for (a) Mode A with V_1 = 300V (b) D_1 = 0.6, V_1 = 300 V and V_2 = 200 V (c) D_2 = 0.3, V_1 = 300 V and V_2 = 200 V (d) D_1 = 0.3, V_1 = V_2 = 200 V (e) D_2 = 0.3, V_1 = V_2 = 200 V and (e) D_1 = D_2, V_1 = V_2 = 200 V.

duty while V_1 is 300 V and V_2 is 200 V. It is observed that when D_2 is smaller below D_1, V_{TR} is constant. This is because the magnitude of V_1 is greater than that of V_2, resulting in $D_{2eff} = 0$. The effect of V_2 only appear when $D_2 > D_1$. Similarly, as shown in Fig 9 (c), when D_2 is kept constant at 60%: V_1 = 300 V and V_2 = 200 V as before. It was noticed that the V_{TR} remains constant when $D_1 < D_2$ despite the magnitude of V_1 is greater than V_2. The reason is that D_{1eff} keeps increasing as D_1 is increased while D_{2eff} is reduced proportionately as D_{1eff} increases, thus keeping $\sum_{i=1}^{N} D_{(i)eff} V_i$ constant. This condition changes when $D_1 > D_2$ and at this point, $D_{2eff} = 0$. As shown in Fig. 9 (d) and (e), $V_1 = V_2 = 200$ V while D_2 and D_1 are alternated at 30% and 60%. Here, V_{TR} is constant when the varying duty is less than or equal to the constant duty, despite the magnitudes of V_1 and V_2 are equal, resulting in keeping the value of $\sum_{i=1}^{N} D_{(i)eff} V_i$ constant when the varying duty was less than the fixed duty. All the cases in Fig. 9 prove that the results from simulations and HIL tests closely match those of the analytical calculation. The discrepancy of the results comes from power losses in the switches and other circuit components.

IV. CONCLUSIONS

A novel multiple input dc-dc converter has been proposed in this research. The proposed MIC uses four quadrant switches, capitalizing on its benefit of full bidirectional controllability to achieve bidirectional buck-boost power flow. It also utilizes fewer passive components, only one inductor and one capacitor for any number inputs. The proposed MIC has been analysed for two inputs having the simultaneous power flow in buck-boost mode. The proposed MIC was numerically verified and validated in open loop operations on an FPGA based HIL device. The applicability of this MIC is not limited to multiple energy storage hybridization in DC microgrids but can also be adapted for hybrid energy storage systems in other applications such as electric vehicles, electric ships, and other systems.

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Paper II:
Novel Multisource DC-DC Converter for All-Electric Hybrid Energy Systems

This paper has been published as:

I. N. Jiya, A. Salem, H. Van Khang, N. Kishor and R. Ciric, "Novel Multisource DC-DC Converter for All-Electric Hybrid Energy Systems," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 12, pp. 12934-12945, Dec. 2022, doi: 10.1109/TIE.2021.3131871.

Novel Multisource DC-DC Converter for All-electric Hybrid Energy Systems

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***Abstract*—In this paper, a novel non-isolated multiple input dc-dc converter (MIC) is proposed for all-electric hybrid energy storage systems. The proposed MIC is capable of bidirectional operation in non-inverting buck-boost configuration and can accommodate the simultaneous energy transfer from multiple sources of different voltage levels to the DC bus. As compared to counterparts, the proposed MIC utilizes a smaller number of inductors and requires only one bidirectional switch to integrate any extra energy storage. Within the framework, a novel voltage transformation, operation modes and control method are presented in detail. The performance and key features of operation with varying voltage levels and duty cycles of the proposed MIC are numerically verified through a high-fidelity hardware-in-the-loop (HIL) platform and experimentally validated on an in-house test rig.**

Index Terms—Bidirectional DC-DC converter, multi-source converter, four quadrant switch, hardware-in-the-loop (HIL), hybrid energy systems.

I. INTRODUCTION

All-electric hybrid energy systems have played a key role in microgrids [1] and zero-emission transportations, e.g in ferry boats [2], electric vehicles [3]. Hybridization in electric energy systems requires a simultaneous power flow of several electric energy sources, and bidirectional operations are strictly required in such systems equipped with energy storages [3]. Using conventional single input converters for multisource conversions would result in the bulky and complex configuration, and high cost [4]. Towards hybrid energy systems, multiple input dc-dc converters (MICs), either isolated or non-isolated, have been proposed in literature [5]. The isolated MICs are based on magnetically connected circuits (through transformers or coupled inductors) while the non-isolated MICs are based on electrically connected circuits [6].

Both isolated and non-isolated MICs are generally derived from the conventional single input converters with a goal of sharing as much components as possible between the input ports of the MICs [7, 8]. They can also be either multi-output or single-output topologies. Recently, isolated and non-isolated multiple-input multiple-output (MIMO) dc-dc converters capable of unidirectional and bidirectional power flow were proposed in [9–12]. However, these MIMO converters suffer from the problem of cross regulation and require complex control strategies to suppress the cross regulation. In [13, 14], MIMO converters were proposed to solve the cross regulation problem, but both topologies, aside having high component count, equal output voltages for all outputs and are unidirectional, thus only applicable to hybrid energy systems, which do not require bidirectional operation. MICs with single output could address these drawbacks.

Single-output isolated MICs are galvanically isolated, being required for certain hybrid systems and high gains [15–17]. The isolated MICs in [16, 17] are synthesized from dual active bridge (DAB) converters through flux additivity. Each input requires its own primary winding, associated active bridge and clamping circuit. This results in the high component count and control complexity due to the phase-shifted pulse width modulation (PS-PWM) required to control the output voltage and the various active clamp controllers [18]. Bulky structure and complex control restrict the isolated MICs from hybrid energy systems, which do not require isolation feature. The non-isolated MICs have features of reduced size, cost, and ease of miniaturization [19]. These features allow non-isolated MICs to gain popularity in all-electric energy systems with extensive developments in recent years [20–30]. The non-isolated MICs in [20, 21] are not capable of independent power flow from the input ports with simultaneous power flow, being possible in boost mode only, like the unidirectional MIC proposed in [23]. In [24], a MIC is proposed in a cascaded arrangement of the conventional buck-boost converters, sharing only an output stage converter and the dc link capacitor like the MICs in [25, 26]. The MICs in [25, 27, 28] are bidirectional buck-boost topologies, but every additional input port to the converters requires an additional inverter leg and an inductor, increasing the board footprint and cost. The MIC proposed in [29] is formed by integrating a synchronous buck converter with a non-isolated LC-DAB converter. However, it can only accommodate two inputs, and its control is complex with each input requiring its own controller, using both duty ratio PWM and PS-PWM. To tackle this problem, a single-inductor MIC proposed in [30] is capable of independent and simultaneous power flow in buck-

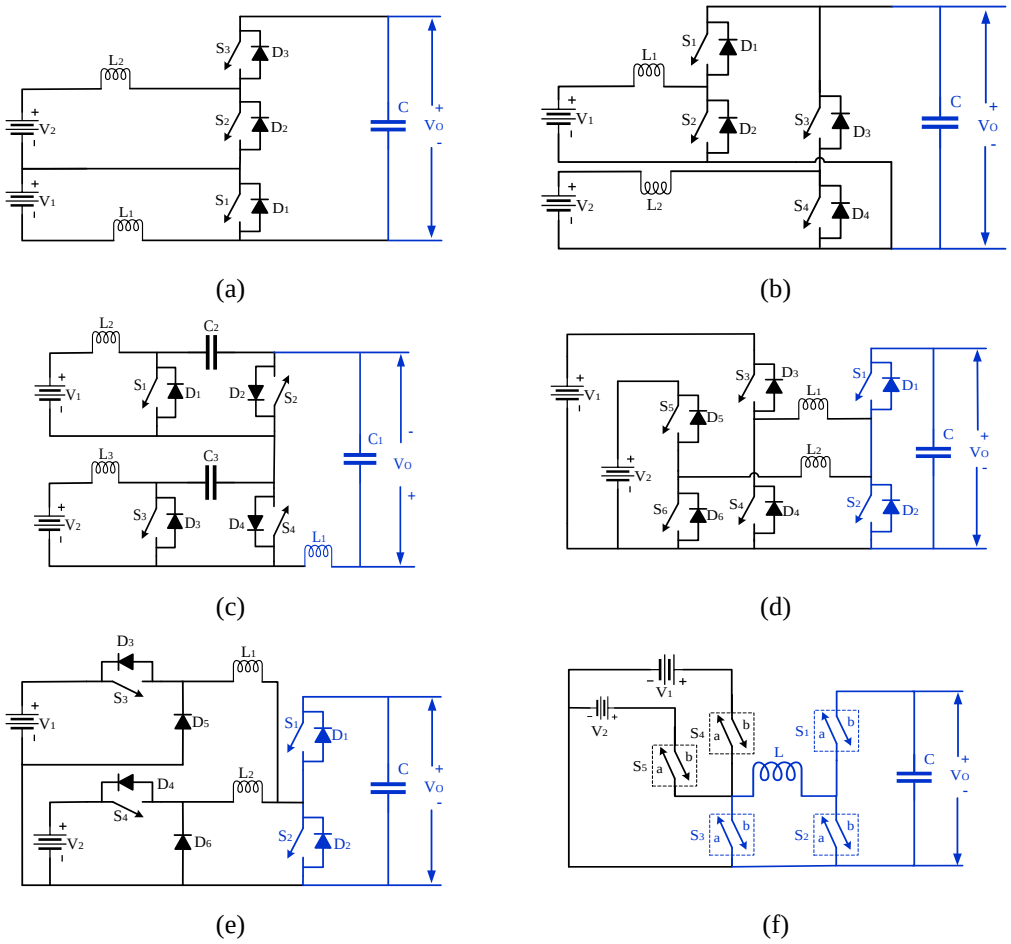


Fig. 1. Integrating multiple energy storage devices into a dc bus using (a) MIC in [20], (b) MIC in [25], (c) MIC in [26], (d) MIC in [27] (e) MIC in [28], and (f) the proposed MIC topology.

boost mode, but it is unidirectional, and its' output voltage is inverted. A non-inverting single inductor unidirectional MIC is proposed in [22], which can only allow for simultaneous power flow in boost mode.

To address the mentioned limitations in the existing MICs, this study proposes a novel MIC for hybrid energy systems, with low component count its key features includes:

1) Non-inverting bidirectional, buck-boost operation.

2) Simultaneous and independent power flow from more than one source of different voltages to the DC bus, in both buck and boost modes, and is modular such that additional input ports can be introduced without modifications to the MIC.

3) Requiring the use of only one inductor for all input sources.

4) Its controller is simple despite its robust operation of ensuring desired dynamic and steady state responses and required power management balance among the sources.

The proposed MIC is constructed by time-multiplexing of a single inductor and utilises four-quadrant switches, aiming to reduce component count and topology complexity while enhancing the converter robustness. To further highlight the novelty of the proposed MIC, the related existing bidirectional MIC topologies proposed [20, 25–28] shown in Fig. 1 (a-e), respectively, are compared with the proposed MIC in Fig. 1. (f). The components highlighted (in blue) are the shared component of every input to the MIC. This is to indicate the level of redundancy in each MIC if only one of the input ports is operational. The MICs in Figs. 1 (a-c) only share the dc link capacitor, only one of the inductors and the dc link capacitor is shared, resulting in a lot of redundant components. Though the MICs in Figs. 1 (d & e) share the dc link capacitor and the output half-bridge, they have more redundant switches and passive components as compared to the proposed MIC in Fig. 1 (f), which shares the dc link capacitor, output half-bridge, one inductor and switch, thus reducing the redundant components to only one bidirectional switch per input port.

Within this framework, a novel voltage transformation factor is proposed, and a single input single output (SISO) controller for parallel configuration with multiple voltages involved is introduced and verified by a high-fidelity real-time hardware-in-the-loop (HIL). The initial idea of the MIC proposed in this work has been presented in [31]. In this paper, the detailed analysis and features are numerically verified through simulations on the HIL device, and experimentally validated using an in-house SiC-switch based experimental test rig.

II. PROPOSED MIC TOPOLOGY

The proposed MIC presented in Fig. 1 (f) consists of one inductor, one capacitor and four-quadrant switches. Four-quadrant switches, also known as fully-controllable bidirectional switches (FBSs), or matrix switches in some cases, are power electronic switches that can control ON-state current and OFF-state voltage bidirectionally. Fig. 2 presents different implementations of FBSs, including two gates, directing the flow of current through the switch. To achieve the ideal switching afforded by FBSs, two unidirectional switches (MOSFET or IGBTs with their respective anti-parallel diodes) are connected in anti-series configuration. In Figs. 2 (a) and (b), the SiC-MOSFETs are connected in common source and drain configuration, respectively. Another interesting approach to achieve monolithic FBSs is illustrated in Fig. 2 (c), in which two reverse blocking IGBTs (RB-IGBTs) are connected in anti-parallel, thereby eliminating the two anti-parallel diodes as

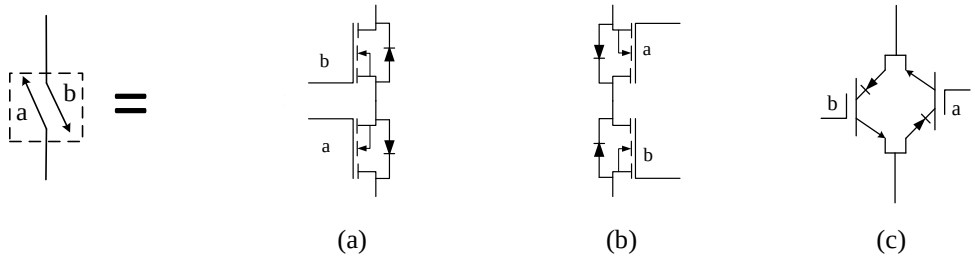


Fig. 2. Four-quadrant switch using (a) common source (b) common drain and (c) reverse blocking IGBTs in antiparallel configuration.

required in Figs. 2 (a) and (b). This could result in lowering the losses, increasing efficiency and reducing switch cost [32], but IGBTs can only be applied for low switching frequency (<20 kHz), increasing the filter requirement in the MIC [33]. Yet, this configuration has received an attention as discussed in [34–36], achieving reverse blocking high electron mobility transistors (HEMTs), allowing for high frequency switching at high power applications. This progress leads to new possibilities for monolithic FBSs from GaN HEMTs as in [37]. FBSs in the proposed MIC allows for a bidirectional power flow between the DC bus and energy storage systems. This converter is capable of bucking and boosting the input voltage in all operation modes. Further, it requires only one additional FBS when another input port is introduced to the MIC.

A. Steady state analysis

The proposed MIC can operate in five modes when using two input sources. The first four modes (A-D) represent the interaction between the DC bus and two energy storage devices exclusively, e.g. from V_1 or V_2 to the DC bus, and vice-versa respectively. Mode E will be elaborated later, representing the situation, in which both energy storages V_1 and V_2 supply the DC bus simultaneously. Fig. 3 presents steady-state waveforms in the associated continuous conduction mode (CCM) for modes A to D. The switching period T_S is divided into two, T_1 and T_2, for the inductor charging and discharging period, respectively, in all four modes of operation.

In mode A, only V_1 is supplying the DC bus, thus the inductor L is charged during time T_1 by switching ON S_{4b} and S_{2b}. During T_1, the voltage V_L becomes V_1 while the inductor current i_L increases with a gradient of V_1/L. After time T_1 has elapsed, T_2 follows immediately. During this period, L discharges through C to the DC bus by switching ON S_{1a} and S_{3a}. During this time, V_L becomes $-V_o$ (the output voltage) and i_L decreases with a gradient of V_O/L. Similarly, when the converter operates in the opposite direction, by sending energy from the DC bus to V_1 in mode C, L

is charged by switching ON S_{1b} and S_{3b} during T_1, while it discharges during T_2 by switching ON S_{4a} and S_{2a}. V_L is V_o and (V_1-V_o) during T_1 and T_2, respectively, while i_L increases with a gradient of V_O/L during T_1 and decreases with a gradient of $(V_1-V_o)/L$ during T_2. The interaction between V_2 and the DC bus in mode B and D is as earlier described for modes A and C, respectively. S_1 to S_3 do not need to block the reverse current as required in S_4 to S_N. The demerit of using only a MOSFET with its freewheeling diode in a synchronous configuration for S_1 to S_3, as listed in [38], makes FBSs very attractive.

The voltage balance analysis on the steady state waveform in Fig. 3 proves that the proposed converter can operate in the buck and boost modes, depending on the duty ratio D, where D is T_1/T_S or the ratio of the inductor charging time to the total switching period. Therefore, the conventional equation (1) describing the relationship between the input V_{in} and output voltage V_{out} of the basic buck-boost converter applies to this converter for modes A to D.

$$V_{out} = \left[T_1/T_2\right]V_{in} = \left[D/(1-D)\right]V_{in} \tag{1}$$

B. Simultaneous power flow

The simultaneous mode of operation was earlier referred to as mode E, in which both V_1 and V_2 supply to the DC bus as illustrated in Fig. 4. This mode is necessary when the required power of the DC bus cannot be satisfied by only a single energy storage. Two or more energy storages then must supply the energy simultaneously. Fig. 5 shows the steady state CCM waveforms, where the inductor charging period

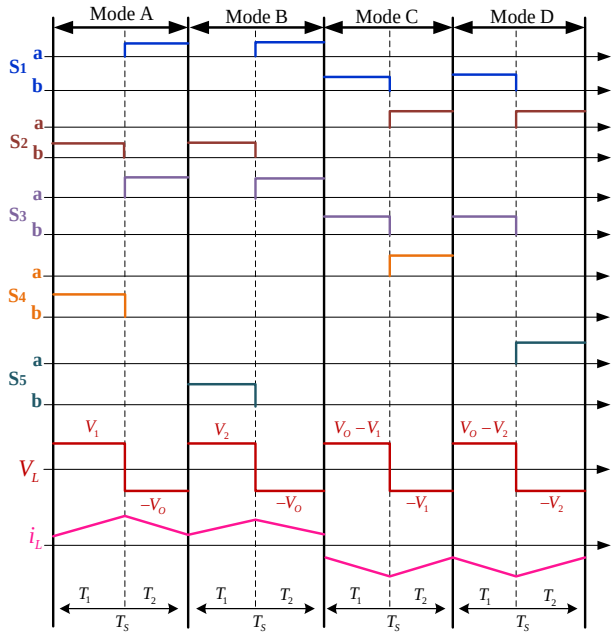
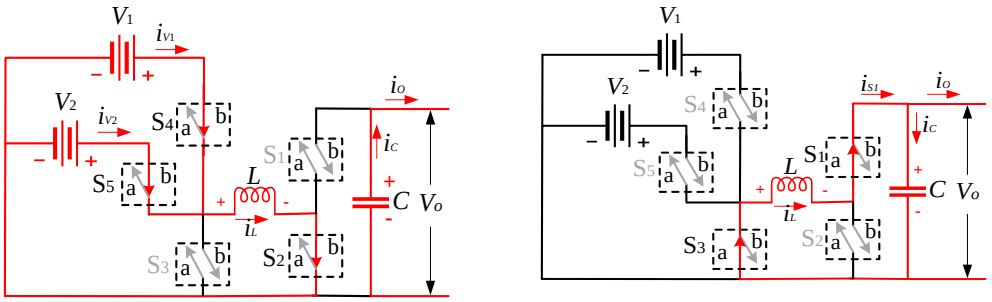


Fig. 3. Steady-state waveforms of operation in CCM for modes A to D.

T_1 is further sub-divided into two for the studied two-input MIC. This sub-division is directly proportional to the number of input sources of the MIC providing a simultaneous power transfer. During T_1, switches S_{4b}, S_{5b} and S_{2b} are all ON. However, in the first subdivision of T_1, the inductor voltage V_L is equal to V_1, which is the source voltage with the highest potential difference. Accordingly, L charges with a gradient of V_1/L. When the first subdivision period of T_1 is over, S_{4b} is turned OFF while S_{5b} and S_{2b} remain ON. In the second subdivision of T_1, V_L becomes V_2 while the inductor continues to charge with a gradient of V_2/L. This process will continue with more than two inputs in the decreasing order of the magnitude in their input voltages. When the inductor charging period is over, S_{5b} and S_{2b} are turned OFF, being immediately followed by the discharging period T_2. During T_2, L discharges through the capacitor to the DC bus by switching ON S_{1a} and S_{3a}, thus V_L becomes $-V_o$, while L discharges with a slope of the sum of the input voltages during their respective ON time divided by the inductance.



(a) (b)

Fig. 4. Path of current flow during mode E for inductor (a) charging and (b) discharging during steady state operation.

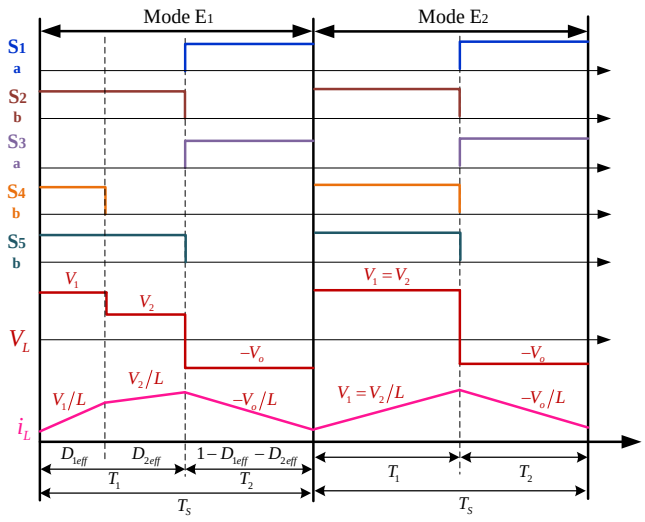


Fig. 5. Steady-state CCM waveform in mode E.

Therefore, L will discharge with a gradient of $(D_{1eff}+D_{2eff}V_2)/L$ during T_2 as shown in Fig. 5.

For an effective commutation in mode E, some basic principles need to be respected to achieve the simultaneous power transfer to the load. When the voltages are unequal in mode E_1 in Fig. 5, with magnitude of the sources arbitrarily arranged in order of increasing magnitudes such that $V_1 > V_2 > \cdots > V_N$ for N input ports, then the duty cycle of the PWM signal controlling the input sources (S_{4b} and S_{5b} in the two input MIC) must be in such a way that $D_1 < D_2 < \cdots < D_N$ and vice versa, where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ... , $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. If the source magnitudes are equal such that $V_1 = V_2 = \cdots = V_N$ for N input ports in mode E_2, duty cycles of the PWM signal controlling the input sources (S_{4b} and S_{5b} in the case of the two input converter) must be as $D_1 = D_2 = \cdots = D_N$ in order to achieve the equal power delivery from the sources. If it is required that the power delivery from the sources must be unequal, then the values of $D_1, D_2, \ldots, D_N$ can be determined in order of increasing magnitude of the required power delivery from the respective sources. The relationship between the input sources and output voltage in steady state is given by (2) for N input sources.

$$V_o = \left[\sum_{i=1}^{N} D_{(i)eff} V_i\right] \Big/ \left[1 - \sum_{i=1}^{N} D_{(i)eff}\right] \tag{2}$$

C. Voltage transformation factor

The proposed MIC can operate in a parallel configuration with multiple voltages involved, thus a novel voltage gain is proposed in this section. During simultaneous power transfer from the sources to the dc bus, the effect of different input voltages on the output voltage does not solely depend on the duty cycles but also on the effective duty cycle of the other input sources. Thus, the gain relationship of MICs, capable of simultaneous power transfer from the inputs, is best defined as a voltage transformation factor (V_{TR}). This is a relationship between the output voltage and its input voltages considering the duty of the switches controlling each respective input port to the MIC. For the proposed MIC, V_{TR} is defined by (3). The obtainable values of V_{TR} are 10.0 and 1.11 if the converter operates at 90% and 10% effective duties. Although V_{TR} for the proposed MIC is similar to the gain of a conventional boost converter, it is vital to note that the input voltages, being compared to the output voltage, is not the full input voltages, but the sum of the input voltages scaled by ON time of their respective switches

($\sum_{i=1}^{N} V_i D_{ieff}$). Thus, the conventional reasoning for the gain relationships of the basic single input converters cannot be applied for MICs.

$$V_{TR} = V_o \Big/ \left[\sum_{i=1}^{N} D_{(i)eff} V_i \right] = 1 \Big/ \left[1 - \sum_{i=1}^{N} D_{(i)eff} \right] \tag{3}$$

D. Power management and control

The simplicity of control is one of the key merits of the proposed MIC as other MICs would require a multiple-input multiple output (MIMO) control structure. The proposed MIC only requires a single-input single-output (SISO) control structure. The closed-loop operation using a double-loop PI controller is illustrated in Fig. 6. The control layer consists of the secondary and primary controller, which is the double loop PI controller, the power management controller (PMC) and the pulse width modulator (PWM). The secondary controller sets the output voltage reference ($V_{o\text{-}ref}$), depending on the MIC's mode of operation. It also determines the proportion of power flow from the sources when operating in a simultaneous power flow mode or mode E. To do this, it determines a scaling factor k_1 to k_{N-1}, which is obtained by comparing the total power capacity (kw_T) of all the sources to the individual power capacities (kw_1 to kw_N) for sources (V_1 to V_N) as described in (4), respectively, or based on other pre-programmed constraints, such as the state of charge (SoC).

$$\left.\begin{aligned} k_1 &= \frac{kw_1}{kw_T} \\ \left(kw_T = kw_1 + \cdots + kw_N\right), &\quad \vdots \\ k_{N-1} &= \frac{kw_{N-1}}{kw_T} \end{aligned}\right\} \tag{4}$$

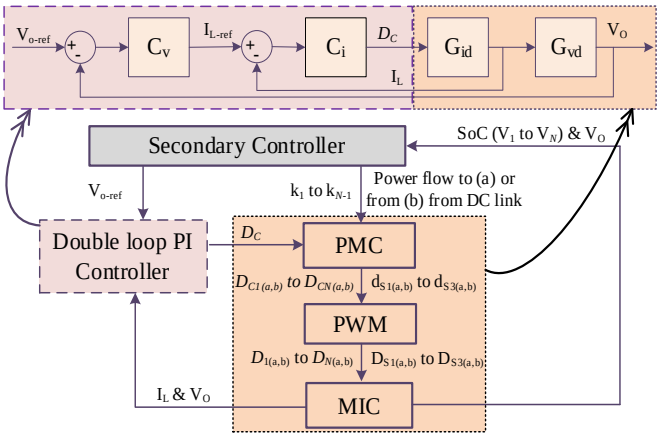


Fig. 6. Converter operational control structure.

The output voltage (V_O) and inductor current (i_L) are used to determine the control variable D_C. D_C is the effective ON time to charge the inductor to achieve the target output voltage as described in (5). To achieve the desired controller performance, the linearised inner current and output voltage-loop transfer functions, G_{id}, (6) and G_{vd}, (7), are developed. The PI gains of controllers, C_i and C_v, are heuristically selected to achieve the desired performance.

$$D_C = \sum_{i=1}^{N} D_{(i)eff} \tag{5}$$

$$G_{id} = \frac{\left[s\left(\sum_{i=1}^{N} D_{(i)eff} V_i \right) \Big/ L \right] + \left[\left(\sum_{i=1}^{N} D_{(i)eff} V_i \right) \Big/ RLC \right]}{s\left(s + \frac{1}{RC} \right) + \frac{1}{LC}} \tag{6}$$

$$G_{vd} = \left[\left(\sum_{i=1}^{N} D_{(i)eff} V_i \right) \Big/ LC \right] \Big/ \left[s\left(s + \frac{1}{RC} \right) + \frac{1}{LC} \right] \tag{7}$$

The operation of the PMC and the PWM is summarised on Table I. The function of the PMC is to adequately manage power and energy supply among sources based on instructions from the secondary controller. At the output of the PMC, $D_{C1(a,b)}$ to $D_{CN(a,b)}$ corresponding to $D_{1(a,b)}$ to $D_{N(a,b)}$ at the output of the PWM refer to the duties applied to the switches controlling the respective input ports i.e. S_{i+3} to S_{N+3}. While $d_{S1(a,b)}$ to $d_{S3(a,b)}$ corresponding to $D_{S1(a,b)}$ to $D_{S3(a,b)}$ at the output of the PWM refer to the duties applied to S_1 to S_3. In mode E, the sum of currents from the sources is presented in (8), and the PMC determines $D_{C1b} - D_{CNb}$ according to (9).

$$I_1 + I_2 + \cdots + I_N = I_L \left(\sum_{i=1}^{N} D_{(i)eff} \right) \tag{8}$$

TABLE I

PARAMETER SCALING BY THE PMC AND PWM

Mode of Operation		PMC	PWM
Mode A or B (V_i to V_O)	T_1	$D_C = D_{Ci(b)} = d_{S2b}$	D_{ib} goes to $S_{(i+3)b}$ & D_{S2b} to S_{2b}
	T_2	$1 - D_C = d_{S1a} = d_{S3a}$	D_{Sia} goes to S_{1a} & D_{S3a} to S_{3a}
Mode C or D (V_O to V_i)	T_1	$D_C = d_{S1b} = d_{S3b}$	D_{S1b} goes to S_{1b} & D_{S3b} to S_{3b}
	T_2	$1 - D_C = D_{Ci(a)} = d_{S1a} = d_{S3a}$	D_{ia} goes to $S_{(i+3)a}$ & D_{S2a} to S_{2a}
Mode E ($\sum_{i=1}^{N} V_i$ to V_O)	T_1	$D_C = d_{S2b}$ & scaled using (9)	D_{ib} to D_{Nb} goes to $S_{(i+3)b}$ to S_{Nb} & D_{S2b} to S_{2b}
	T_2	$1 - D_C = d_{S1a} = d_{S3a}$	D_{Sia} goes to S_{1a} & D_{S3a} to S_{3a}

$$\left.\begin{aligned} D_{C1b} &= D_{1eff} = k_1\left(\sum_{i=1}^{N} D_{(i)eff}\right) \\ &\vdots \\ D_{C(N-1)b} &= D_{N-1eff} = k_{N-1}\left(\sum_{i=1}^{N} D_{(i)eff}\right) \\ D_{CNb} &= D_{Neff} = \sum_{i=1}^{N} D_{(i)eff} - \sum_{i=1}^{N-1} D_{(i)eff} \end{aligned}\right\} \tag{9}$$

III. COMPARISON WITH RELATED TOPOLOGIES

Table II presents a comparison between some existing non-isolated MICs and the proposed one in this paper. It is arranged in descending order of the total component count. Other key parameters are the possibility of bidirectional power flow, simultaneous and independent power flow from the input sources and the topology of operation that is, buck, boost or both buck-boost. For this comparison, when the MIC topology is defined as, buck, boost, this means that the converter is bidirectional and so in one direction it bucks and boosts in the other direction of power flow. The basis for selecting the MICs on Table II for the comparison with the proposed MIC is their similarity in structure as shown in Fig. 1.

TABLE II
COMPARISON OF THE PROPOSED MIC WITH OTHER NON-ISOLATED MICS

Parameters		[26]	[25]	[27]	[28]	[20]	[22]	Proposed
Component Count (CC)	S	2N	2N	2N+2	N+2	N+1	N+1	N+3 (2N+6)*
	D	2N	2N	2N+2	2N+2	N+1	1	0
	L	N+1	N	N	N	N	1	1
	C	N+1	N+1	1	1	1	N+1	1
	T	6N+2	6N+1	5N+5	4N+5	3N+3	2N+4	N+5 (2N+8)*
IPF		Yes	Yes	Yes	No	Yes	Yes	Yes
PFP		No	No	Yes	No	No	No	No
Simultaneous power flow		Yes, buck-boost	No	Yes, buck-boost	Yes, boost	Yes, boost	Yes, boost	Yes, buck-boost
Modular?		Yes	Yes	Yes	No	Yes	Yes	Yes
Bidirectional?		Yes	Yes	Yes	Yes	Yes	No	Yes
Topology		Ćuk	buck-boost	buck-boost	buck, boost	buck, boost	boost	buck-boost
V_{TR}		SP	NA	SP	NR	SP	SP	(3)
F_{SW} (kHz)		20 – 80	15	20	NR	20	20	20 – 150

N=Number of inputs, IPF=Independent power flow, PFP=PF between ports, S=Switch, D=Diode, L=Inductor, C=Capacitor, T=Total, SP=Same with proposed, NA=Not applicable, NR=Not reported, *=Value when two unidirectional switches are used to achieve one bidirectional switch.

The MICs in [25, 28] using a high component count can operate in buck/boost modes, but they do not allow for a simultaneous power transfer from the input ports, or power transfer between ports. The MICs in [20, 26] require lower component counts as compared to [25, 28], but the power from the input ports can be simultaneously transferred only in the boost mode. The MIC in [22] seems to have competitively low component count as the proposed MIC, but the simultaneous power flow is only possible in boost mode as against the buck-boost simultaneous power flow possible in the proposed MIC. Further, it can be argued that since the current implementation of FBSs require two pairs of MOSFETs, the total component count of the proposed MIC should be 2N+8. However, the proposed MIC will still require less component count than the 5N+5 required in [27], which is the closest competitor in terms of bidirectional buck-boost capabilities with simultaneous power flow possible in buck boost mode. The MIC in [22] would have a lower component count than the proposed MIC but it is not bidirectional and only allows for simultaneous power flow in a boost mode. All the compared MICs have the same VTR except for the MICs in [25], which is not capable of simultaneous power transfer, and [20] for which the relationship between input and output voltages is not defined.

IV. RESULTS AND DISCUSSION

The proposed MIC topology is numerically verified in simulations on the in-house real time HIL using OPAL-RT's OP5700 running a 64bit virtex-7 FPGA. Further, the proposed topology is experimentally validated on actual SiC switches, which can handle up to 5-kW. The proposed MIC is controlled from Imperix's B-box 3.0, a kintex grade FPGA controller. Table III presents the parameters used for the verification and validation. The switches are the PEB-SIC 8024 configurable switch legs from Imperix. This switch bank is made from CREE's C2M0080120D SiC power MOSFETs. The in-house setup for both HIL verification and experimental implementation is presented in Fig. 7. The test setup consists of the switch and passive component (L and C) bank, controller, real-time simulator, oscilloscope, DC power supplies and loads. In the HIL simulations, the converter hardware is implemented in the RT-HIL simulator while being controlled externally. In the experimental validation, the open-loop operation of the proposed MIC is tested using real SiC switches. The proposed MIC is numerically verified and experimentally validated in the different operation modes. Since operations in modes A-D are conventional in buck-boost converters and sufficiently addressed

TABLE III
PARAMETERS USED IN MIC VALIDATION

Parameter	Value
Switching frequency (F_{SW})	20 – 150 kHz
Source 1, V_1	300 V
Source 2, V_2	200 V
Output power (P_O)	5 kW
Output voltage (V_O)	200 – 400 V
L, Hammond – 195E50	2.5 mH/50A/8mΩ
C, KEMET – ALS70A472NF500	4.7 mF/500V/59mΩ
S_{1a} – S_{5b}, CREE – C2M0080120D	1200V/36A/80mΩ

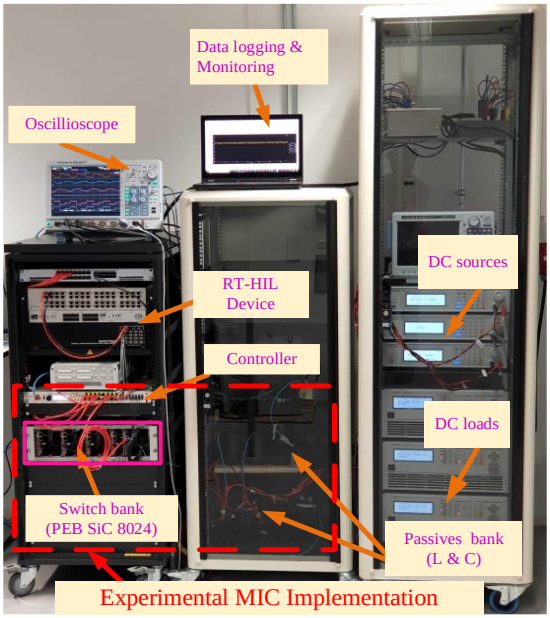


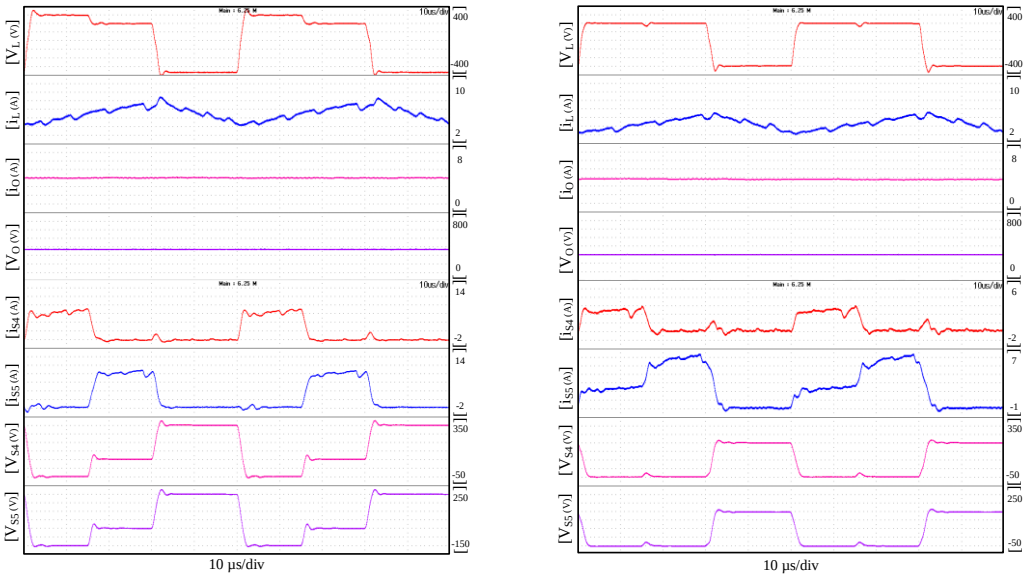
Fig. 7. Validation of the MIC on the HIL platform and the experimental test setup.

in literature, and due to the page limit, the results presented are mostly for mode E, demonstrating the simultaneous flow of energy from two sources.

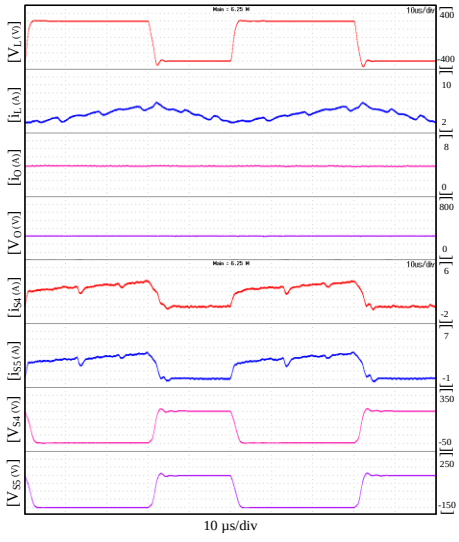
A. Open-loop implementation on HIL

The numerical results of open-loop tests on the HIL platform are presented in Fig. 8. Three different scenarios are considered in mode E. The first one is when both energy storages have different voltage levels or need to be controlled using two different duty cycles. The second scenario is characterized by the two energy storages having equal voltage levels but different duty cycles or unequal power flow from both sources. In the third scenario, both voltage levels and duty cycles are equal, or the sources provide an equal power flow to the DC link. The HIL results for these scenarios are presented in Figs. 8 (a) – (c), respectively, in which the voltages across some switches are also presented, particularly switches S_4 and S_5, controlling the energy flow from the sources. In Fig. 8 (a), the voltages of V_1

and V_2 are different, with the duty cycle applied to S_4 less than that to S_5. Therefore, the currents supplied from the sources are different, and the output voltage (V_O) is about 369 V in the HIL implementation, verifying the 375 V obtained analytically. The inductor ripple current (ΔI_L) is about 4 A with an average (I_L) of 5.5 A, the output current (I_O) is about 3.85 A. In Fig. 8 (b), although both V_1 and V_2 are equal, the duty of S_5 is greater than that of S_4, so the average current supplied by V_1 is less than that supplied by V_2. In this scenario, V_O is about 297 V also validating the 300 V obtained analytically, I_O is about 3.5 A, ΔI_L is 3.82 A and I_L is about 4 A.



(a) (b)



(c)

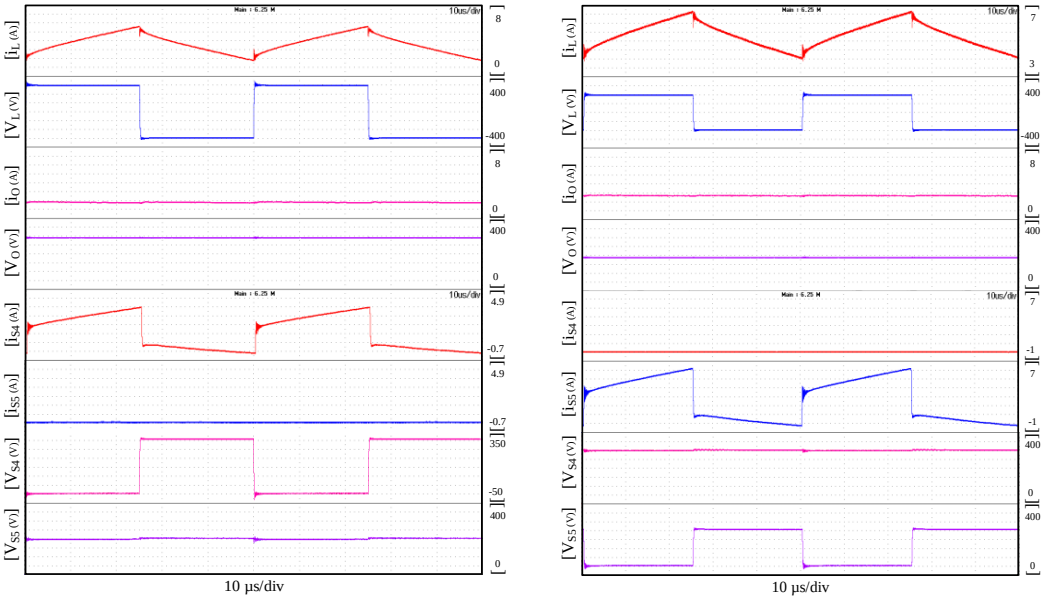
Fig. 8. HIL results in mode E where V_L & i_L: inductor voltage & current, i_O & V_O: output current & voltage, and i_{S4}, i_{S5}, V_{S4} & V_{S5}: S_4 & S_5 current & voltage, for (a) V_1=300 V, V_2=200 V, D_1=30%, D_2=60% and load=1.5 kW (b) V_1=V_2=200 V, D_1=30%, D_2=60% and load=1 kW and (c) V_1=V_2=200 V, D_1=D_2=60% and load=1 kW.

Conversely, in Fig. 8 (c), V_1 = V_2 = 200 V and D_1 = D_2 = 60%, thus equal current is supplied by both sources. Thus, similar values of V_O, I_O, ΔI_L and I_L as in Fig. 8 (b) are obtained since V_1 and V_2 are the same.

B. Open-loop experimental validation

Fig. 9 presents the results of open loop validations of the proposed MIC in modes A and B, respectively. In both cases, the load is 500 W with V_1=300V, V_2=200 V while the respective duty cycle of the switch is 0.5, i.e. D_1=0.5 D_2=0, in mode A and D_1=0 while D_2=0.5 in mode B. In Fig. 9 (a), ΔI_L is about 4 A with an average I_L of 3.8 A, and I_O is about 1.8 A while the output voltage, V_O, is about 290 V, which is a 10 V drop from the calculated of 300 V. In Fig. 9 (b), the inductor ripple, ΔI_L, is about 3 A with a higher average I_L than in Fig. 9 (a) at about of 5.5 A, since I_O is also higher in Fig. (b) at about 2.7 A due to the lower output voltage, V_O, of about 191 V, which is a 9 V drop from the calculated of 200 V. The voltages (V_{S4} & V_{S5}) and currents (i_{S4} & i_{S5}) of the switches controlling the input sources (S_4 & S_5) are also presented in Fig. 9.

The experimental tests on the SiC switch bank were performed to validate the HIL results in IV. A. Fig. 10 presents the results of experimental validation in open-loop operations. In Fig. 10 (a), V_1 = 300 V, V_2 = 200 V, D_1 =30% and D_2 = 60% while V_O is about 360 V, which is about 9 V and 15 V drop from the respective



(a) (b)

Fig. 9. Experimental results with V_1=300 V, V_2=200 V, under 500W load where V_L & i_L: inductor voltage & current, i_O & V_O: output current & voltage, and i_{S4}, i_{S5}, V_{S4} & V_{S5}: S_4 & S_5 current & voltage, for (a) Mode A, D_1=50% and D_2=0 and (b) Mode B, D_1=0 and D_2=50%.

HIL and calculated results. ΔI_L is about 4 A, like the HIL result, but I_L is about 7.4 A, or an increase of about 2 A from the HIL result and I_O is about 2.7 A. In, Figs. 10 (b & c), the source voltages are V_1 = V_2 = 200 V, but the unequal duty cycles are considered in Fig. 10 (b) while equal ones are shown in Fig. 10 (c). In both cases, V_O is about 286 V, which is about 10 V and 14 V drop from the respective HIL and calculated results. ΔI_L is about 3.4 A, I_L is about 5.9 A with I_O of about 2

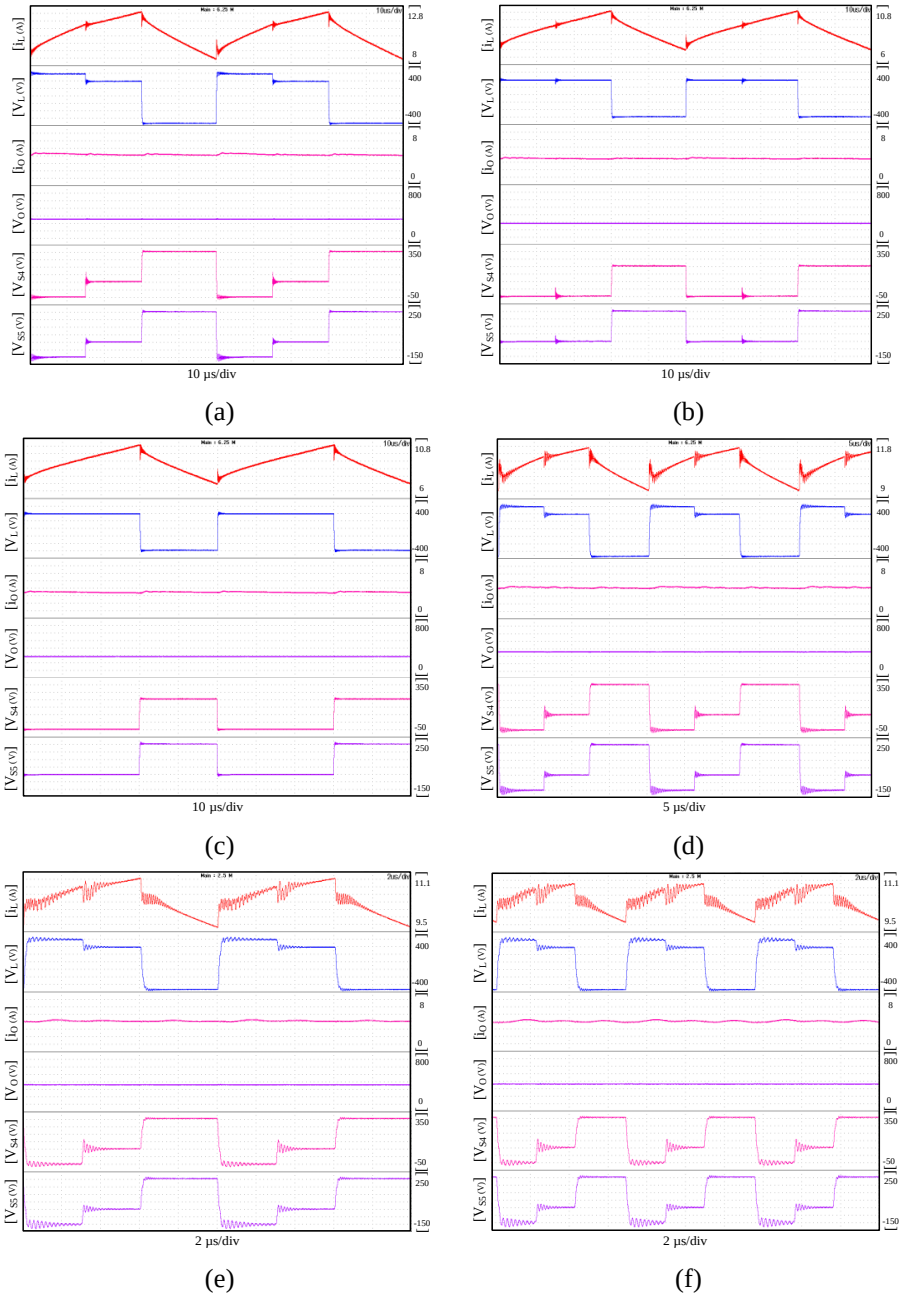


Fig. 10. Experimental results in mode E, where V_L & i_L: inductor voltage & current, i_O & V_O: output current & voltage, and V_{S4} & V_{S5}: voltage across S_4 & S_5, for (a) V_1=300 V, V_2=200 V, D_1=30%, D_2=60% and load=1.5 kW, (b) V_1=V_2=200 V, D_1=30%, D_2=60%, and load=1 kW, (c) V_1=V_2=200 V, D_1=D_2=60%, and load=1 kW. F_{SW}= 20kHz in (a) – (c) while in (d) – (f) V_1=300 V, V_2=200 V, D_1=30%, D_2=60% and load=1 kW, but F_{SW}= 50kHz, 100kHz & 150kHz.

A. The expected differences are within acceptable limits and are due to the non-idealities (e.g. parasitic impedances) in the experimental setup that was unaccounted for in the simulation.

To demonstrate the effect of high F_{SW} on the proposed MIC, it was operated using the same parameters in Fig. 10 (a), but F_{SW} is changed to 50 kHz, 100 kHz and 150 kHz and the results are presented in Figs. 10 (d-f), respectively. It is observed that as F_{SW} increases, ΔI_L reduces from about 4 A at 20 kHz to about 1.7 A at 150 kHz. Similarly, I_L reduces from about 7.4 A to about 7.2 A. Further, it is observed that as F_{SW} increases, V_O increases from about 360 V at 20 kHz to about 367 V at 150 kHz. Thus at 150 kHz, V_O is only about 2 V and 8 V less than the V_O obtained in the HIL and calculation.

Fig. 11 shows V_{TR} obtained from analytical calculations, HIL simulations and experimental tests for different combinations of duty cycles D_1 and D_2, where F_{SW} is 20 kHz, V_1= 50 V and V_2 = 25 V. V_1 and V_2 are chosen such that at 90% duty cycle, the limits of the test equipment are not violated. D_1 is kept constant at 30% duty while D_2 is varied. It is observed that when $D_2 < D_1$, V_{TR} remains constant. This is because $V_1 > V_2$, thus D_{2eff} = 0. The effect of V_2 appears only when $D_2 > D_1$. Similarly, when D_2 is kept constant at 60%, V_{TR} remains constant when $D_1 < D_2$ despite the magnitude of V_1 is greater than V_2. The reason is that D_{1eff} keeps increasing as D_1 is increased while D_{2eff} reduces proportionately as D_{1eff} increases, thus keeping $\sum_{i=1}^{N} D_{(i)eff} V_i$ constant. This changes when $D_1 > D_2$ and at this point, D_{2eff} = 0. Fig. 11 shows a good agreement among the results from analytical calculation, HIL simulations and experimental tests despite the expected losses. Further, there is a multi-fold increase in V_{TR} with change in duty cycle from 80% to 90%.

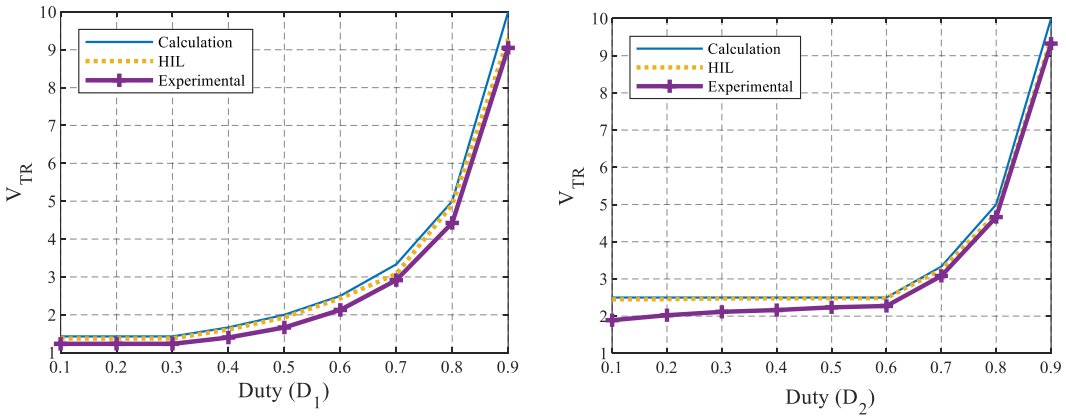


Fig. 11. Obtained V_{TR} comparison in mode E, with F_{SW}=20 kHz, V_1=50 V, V_2=25 V, D_1=0.3 and D_2=0.6.

C. Closed-loop operations using HIL

This section shows HIL simulation results of the proposed MIC under closed loop operations to prove its robust operation despite of using a SISO controller. The double-loop PI controller for the proposed MIC is designed based on the Ziegler-Nichols tuning method. Fig. 12 shows the closed loop performance of the MIC under perturbations in the input voltages and load current. The step response of the output voltage is also presented, where the time constant is about 20 ms, the rise time is 30 ms and the settling time is about 50 ms with a steady state error of about

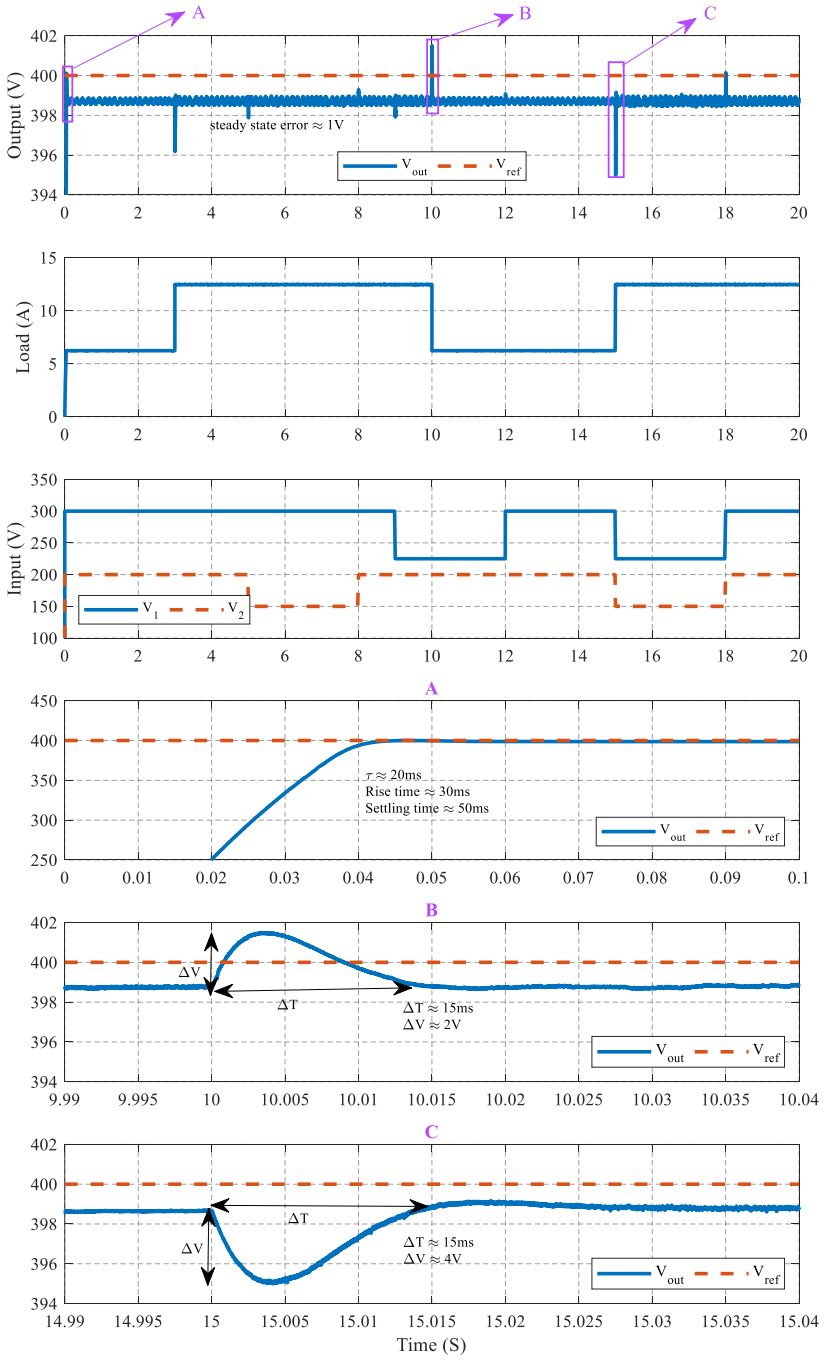


Fig. 12. Closed loop performance under voltage and current perturbations.

1 V. The MIC's controller can reject the disturbances in the input voltages from 300 V to 225 V and 200 V to 150 V, respectively, for V_1 and V_2. The load current is also stepped from 6 A to 12 A, and vice-versa. The controller can maintain the output voltage in less than 15 ms while the dip remains less than 4 V under the disturbances. These results indicate how a simple controller is sufficient to control the output voltage.

D. Efficiency

The efficiency of the MIC in the experimental setup, as presented in Fig. 13, showing the effect of varying F_{SW} on efficiency at varying load conditions. Fig. 13 (a) is conducted when V_1=300 V, V_2=200 V with D_1=0.3 and D_2=0.6 thereby yielding an output voltage of about 360 V. In Fig. 13 (b), when V_1=V_2=200 V with D_1=D_2=0.6, the output voltage is about 290 V. It is observed that as the load is increased, efficiency also increases. The converter prototype was designed for operation at 5 kW, but the available in-house load is only 2.5 kW. A significant improvement in the efficiency is observed on increase in F_{SW}, highlighting the benefits derived from using WBG devices as it has up to 96% efficiency with F_{SW} of 150 kHz at 2.5 kW load in Fig. 13 (a) and up to 95% efficiency in Fig. 13 (b).

The power losses (P_L) in MIC can be estimated using (10), consisting of the inductor winding (P_{indW}) and core (P_{indC}) losses [39], capacitor losses (P_{cap}), MOSFET switching and conduction losses [40], where T_S is the switching period, R_{ESRL} is the inductor's equivalent series resistance (ESR), $\hat{i}_L$ is the inductor average current, Δi_L is the inductor ripple current, $K, \beta \& \alpha$ are Steinmetz parameters, R_{ESRC} is the capacitor ESR, V_{DS} is the MOSFET drain to source voltage, i_{DS} is the MOSFET drain to source current, t_{on} & t_{off} is the MOSFET ON and OFF time, R_{DSon} is the MOSFET on state resistance and *D* is its respective duty cycle.

Fig. 10 shows that increasing F_{SW} reduces Δi_L, lowering the losses in inductor and capacitor based on (10) thus increasing efficiency. However, at a point, the effect of Δi_L is less obvious although Δi_L reduces with the increase in F_{SW}, the switching losses and conduction losses at some point overturn the gains of reduced Δi_L. Thus, it is necessary to find an optimal F_{SW} so that it does not negatively affect the MIC's efficiency. Further, the loss distribution presented in Fig. 13 (b) is obtained by (10).

$$P_L \approx \left\{ \underbrace{\frac{1}{T_S}\int_0^{T_S} R_{ESRL}\left(i_L^{\,2} + \frac{\Delta i_L^{\,2}}{12}\right)}_{P_{indW}} + \underbrace{K\Delta i_L^{\beta} F_{SW}^{\alpha}}_{P_{indC}} + \underbrace{R_{ESRC}\left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}_{P_{cap}} + \underbrace{\frac{1}{2}V_{DS} i_{DS} F_{SW}\left(t_{on}+t_{off}\right)}_{P_{SWMOS}} + \underbrace{R_{DSon} i_{DS}^2 D}_{P_{onMOS}} \right\} \quad (10)$$

It shows an average break-down of the losses in the different components of the proposed MIC under 2.5 kW load at 150 kHz switching frequency. The losses in the capacitor (P_{cap}) account for less than 1% of the total losses under this condition. The losses in the inductor accounts for almost 30% of the total losses of which about 10% is in the winding (P_{indW}) and the rest is due to the core (P_{indC}). The bulk of the total losses comes from the switches, accounting for almost 70% of the losses in the MIC. The conduction losses (P_{onMOS}) account for almost 40% of the total loss, which is noticeably higher than the switching losses. This is because the configuration of FBSs used in the experimental verification is as shown in Fig. 2

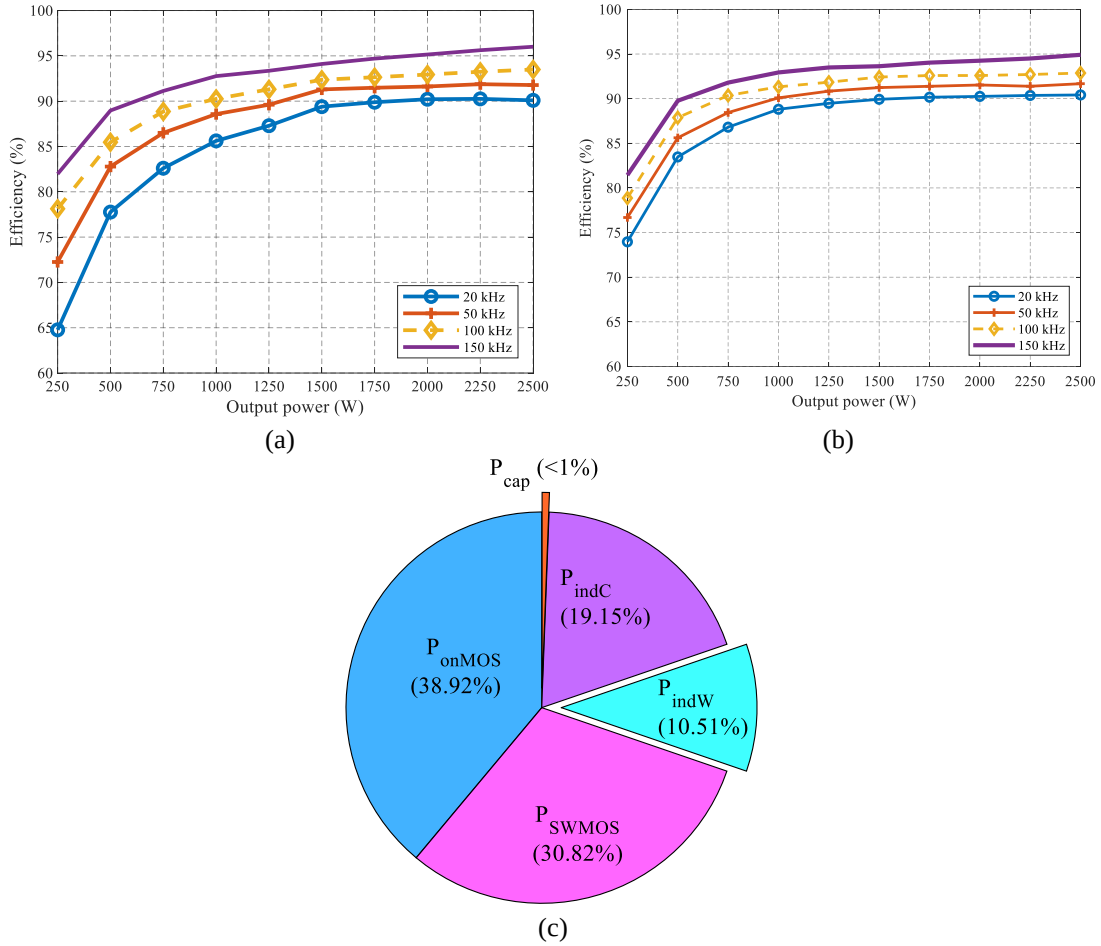


Fig. 13. Experimental efficiency analysis of the MIC under varying F_{SW} for (a) $D_1 = 0.3$, $D_2 = 0.6$, $V_1 = 300$ V & $V_2 = 200$ V, (b) $D_1 = D_2 = 0.6$ & $V_1 = V_2 = 200$ V and (c) theoretically obtained loss distribution at 2.5 kW load and F_{SW}=150 kHz.

(a). Thus, when a switch is turned ON, it is conducting through the diode of the other pair as well, therefore, its losses are also considered. As the WBG technology matures and the adoption of GaN (which has better characteristics than SiC) based switches increase, the losses in the switches will drop due to the reduction in the switching times (t_{on} and t_{off}) and the on-state resistance (R_{DSon}).

V. CONCLUSION

A multisource dc-dc converter using four quadrant switches was proposed in this study with key merits of bidirectional and simultaneous power flow with multiple sources of varying voltage levels, non-inverting buck-boost operations, using one inductor for multiple-input sources, and simplicity of control using a single-input single-output control structure. The detailed analysis and performance of the proposed topology were numerically verified by the in-house high-fidelity hardware-in-the-loop platform and experimentally validated at different switching frequencies using SiC switches. It was demonstrated that the proposed MIC has attractive features such as modularity, high efficiency, and lower component count as compared to the counterparts.

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Paper III:

Novel Isolated Multiple-Input Buck-Boost DC-DC Converter for Renewable Energy Sources

This paper has been published as:

I. N. Jiya, H. Van Khang, A. Salem, N. Kishor and R. Ciric, "Novel Isolated Multiple-Input Buck-Boost DC-DC Converter for Renewable Energy Sources," *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society,* Toronto, Canada, 2021, pp. 1-6, doi: 10.1109/IECON48115.2021.9589538.

Novel Isolated Multiple-Input Buck-Boost DC-DC Converter for Renewable Energy Sources

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***Abstract*—An isolated multiple input dc-dc converter (MIC) with unidirectional buck-boost characteristics and simultaneous power transfer is proposed for multi-sources in renewable energy systems in this paper. When compared to existing isolated MICs, the proposed MIC significantly reduces the component count and control complexity since it requires a fixed coupled inductor with only one primary and secondary winding each for any number of inputs and does not require any phase-shifted pulse-width modulation. The operation of the proposed converter for simultaneous power transfer from multiple sources with varying voltages is numerically verified in simulation and validated on OPAL-RT's OP5700 hardware-in-the-loop (HIL) validation platform.**

Keywords—buck-boost, dc-dc converter, isolated converter, hardware-in-the-loop, multiple input converter, multi-source converter, renewable energy sources

I. INTRODUCTION

With the increasing penetration of multiple renewable energy sources, power electronic converters have gained popularity for effective energy utilization [1]. Among others, dc-dc converters have been widely used to convert the different voltage levels of several dc sources to a standard operating voltage in dc microgrids [2]. To reduce the complexity, size and cost of using single input dc-dc converter systems, multiple input dc-dc converters (MICs), both isolated and non-isolated ones, have gained an increased attention for application in renewable energy systems such as in photovoltaic systems [3].

Isolated MICs have key features of high gain and safety due to the magnetic isolation of input and output provided by the magnetic components [4–12]. In [4–8], several isolated MICs were proposed, but their common limitation is the use of

multiple windings for the inputs of the transformers or coupled inductors based on flux additivity. This leads to reduced power density, increased size, and control complexity since the phase-shifted pulse-width modulation (PS-PWM) control is required to achieve simultaneous power transfer from the input sources. Further, since multiple windings are required at the primary side of the magnetics for the input sources, and multiple clamping circuits will also be required, further increasing component count and potentially control complexity if active clamping is applied. To mitigate these issues, the authors in [9–12] propose isolated MICs with only two windings, one primary and secondary each. However, these MICs also suffer from high component count with some requiring multiple inductors and capacitors at each input [10].

The isolated MIC proposed in this paper addresses the mentioned limitations of the existing topologies. The component count is kept low while the simultaneous power transfer from multisources is implemented by time multiplexing the magnetizing inductance of a two winding (one primary and secondary winding each) magnetically coupled inductor. By utilizing switches based on wide band gap (WBG), the MIC can achieve high frequency switching, thus lowering the magnetizing inductance and filter component requirement, and increasing the power density.

Within the framework of this research, the proposed isolated MIC has the following unique features: It requires the use of only one primary and secondary winding for any number of input sources. Also, it is capable of simultaneous power transfer from more than one source of varying voltage levels to the dc bus. The proposed MIC is capable of unidirectional buck and boost operation with non-inverted output voltage and a high gain. The detailed analysis of these features was performed numerically verified through detailed simulation studies and implemented on an in-house high fidelity real-time hardware-in-the-loop (HIL) platform.

II. PROPOSED ISOLATED MIC TOPOLOGY

Fig. 1 presents the isolated MIC proposed in this research. It involves the use of a coupled inductor, a capacitor, a diode, an RCD clamping circuit, and reverse blocking transistors controlling the respective input sources. The MIC is capable of unidirectionally bucking or boosting the input voltage depending on its application. It requires only one additional reverse blocking transistor (SW) when additional inputs are being introduced. Currently, there are few reverse blocking

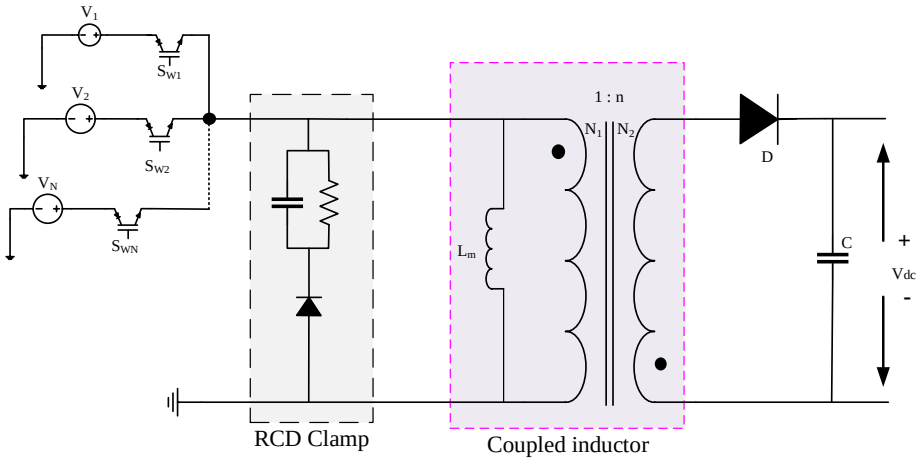

Fig. 1. Proposed flyback-based isolated multiple input converter.

FETs on the market. Therefore, to realize the reverse blocking transistor, a diode can be connected in series to a regular FET instead. One of the main selling points of this isolated MIC is that contrary to conventional topologies where each input of the isolated MIC has its own primary winding, this MIC needs only one primary winding for any number of inputs, resulting in yielding smaller size. Further, only one clamping circuit is required since only one primary winding is needed by the MIC and the control is also simpler for active clamping.

A. Independent power transfer in CCM and DCM

In single input modes, when energy is delivered from only one of the inputs to the dc bus, that is from V_1 or V_2. The respective switch S_{W1} or S_{W2} is turned ON to charge the magnetizing inductance (L_m) for a period of DT_S, where D is the duty cycle and T_S is the total switching period. During switching time $(1-D)T_S$, the switch is turned OFF and then diode, D, conducts to discharge L_m to the dc bus. Thus, the converter will operate like a standard flyback converter where (1) and (2) describe the relationship between input and output voltages for continuous conduction (CCM) and discontinuous conduction modes (DCM), respectively, where R is the resistance of the RCD clamp.

$$V_{dc} = \frac{V_{in} D}{1-D} n \tag{1}$$

$$V_{dc} = V_{in} D \sqrt{\frac{R}{2L_m} T_S} \tag{2}$$

B. Simultaneous power transfer in steady state CCM

For simultaneous power transfers from two or more sources, as illustrated in Fig. 2 with two inputs. The switches controlling all the sources are turned ON at the

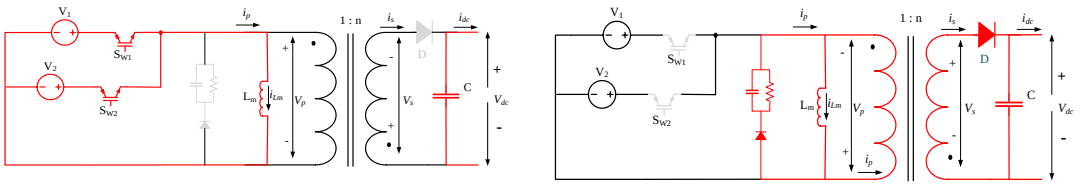

Fig. 2. Path of current during L_m (a) charging and (b) discharging for simultaneous operation of a two input MIC.

same time but turned OFF in the order of decreasing magnitude of the respective voltages. Therefore, the charging of L_m is time multiplexed as illustrated in Fig. 3 for the operation of two simultaneous inputs.

In steady state CCM as illustrated in Fig. 3, the switching period is divided into two main parts, the charging and discharging times of L_m. The first part is further subdivided depending on the number of inputs of the MIC in simultaneous operation:two divisions (D_{1eff} and D_{2eff}) in this case while the second part remains fixed as $(1 - \sum_{i=1}^{N} D_{ieff})$, indicating the discharging time of L_m. When the switches are turned ON, current flows from the source with the highest potential first or V_1 in this case, so L_m is charged with a slope of V_1/L_m during D_{1eff}. When the time D_{1eff} is elapsed, V_2 takes over to continue charging L_m with a slope of V_2/L_m during D_{2eff}. This continues up to D_{Neff} with a slope of V_N/L_m for any number of inputs. At the end of the charging time, $\sum_{i=1}^{N} D_{ieff}$, L_m is discharged to the dc bus with a slope of $-[(V_{dc}/n)/L_m]$, where n is the turns ratio N_2 / N_1 of the coupled inductor. By applying volt-second balance of the resulting steady state CCM waveform in Fig 3 the input-output voltage is described by (3).

$$V_{dc} = \frac{\sum_{i=1}^{N} V_i D_{ieff}}{1 - \sum_{i=1}^{N} D_{ieff}} n \tag{3}$$

For an effective commutation of the switches in multi-input mode, some principles need to be respected to achieve simultaneous power transfer to the load. When the voltages are unequal, the magnitude of the sources is arbitrarily arranged in order of decreasing magnitudes such that $V_1 > V_2 > \cdots > V_N$, the duty cycles of the PWM signals of controlling the input sources, e. g S_{W1} and S_{W2}, must be such that $D_1 < D_2 < \cdots < D_N$, and vice versa, where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ..., $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. However, if the source voltages are equal such $V_1 = V_2 = \cdots = V_N$, duty cycles of the PWM signals must be in such a way that

$D_1 = D_2 = \cdots = D_N$ to achieve an equal power delivery from the sources. If the required power delivery from the sources is unequal, $D_1, D_2, \ldots, D_N$ can be determined in order of increasing magnitude of the required power delivery from the respective sources.

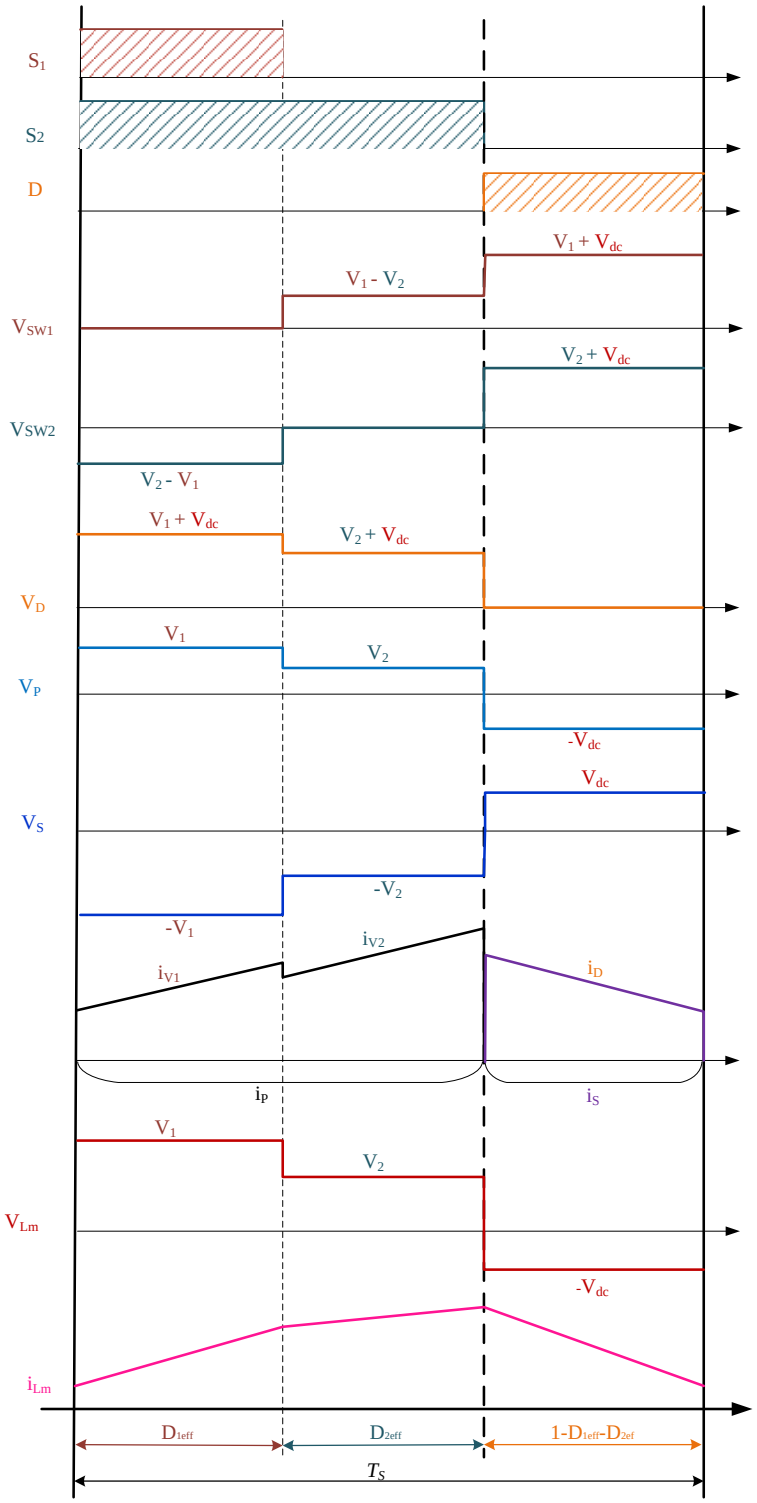

Fig. 3. Steady state CCM waveform for the MIC with two inputs.

C. Simultaneous power transfer in steady state DCM

In the conventional application of flyback converters, a popular approach is its operation in DCM due to ease of stabilization and the possibility of zero current and voltage switching (ZCS and ZVS), although ZVS is only possible with additional circuitry. The steady state waveform for DCM operation of the proposed MIC is illustrated in Fig. 4. The main difference between the DCM and the CCM operation previously described is that in DCM, L_m is designed to be much smaller than that required for CCM. Consequently, the slope of the current in L_m, the primary winding and the secondary winding is much steeper in DCM than in CCM. Therefore, at the end of each switching period, the core is completely discharged. From the steady state DCM waveform presented in Fig. 4, the input-output voltage relationship is described by (4), which is obtained by volt-second balance and balancing the input and output power such that DCM operation is guaranteed. From Fig. 4, it is observed that ZCS can be achieved at turn ON of switches S_{W1} to S_{WN} while the diode will also benefit from ZCS at its turn OFF. However, the conduction losses are much higher since the DCM has a higher peak current than CCM. Consequently, the inductor core will also be much larger at high power application. Therefore, the DCM operation of the proposed MIC is only attractive for low power applications.

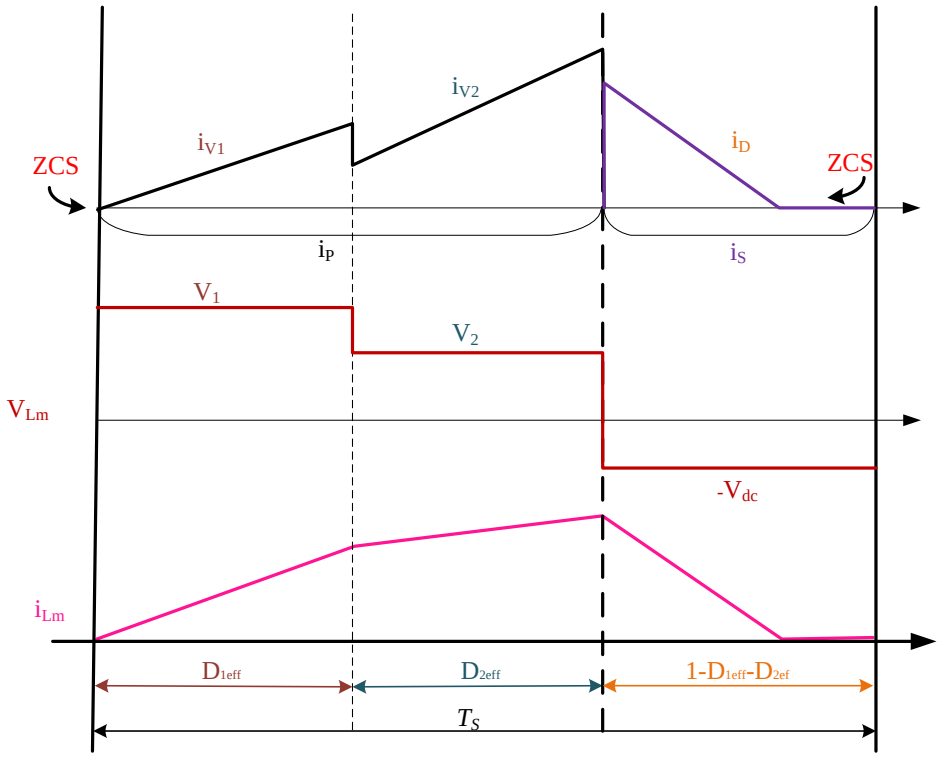

Fig. 4. Steady state DCM waveform for the MIC with two inputs.

$$V_{dc} = \sum_{i=1}^{N} V_i D_{ieff} \sqrt{\frac{R}{2L_m} T_S} \tag{4}$$

D. Voltage stress and gain

Ignoring the voltage ripple across the RCD clamp circuit, the voltage stress on any of the switch (S_{Wx}) is derived as expressed in (5), where V_x is the source voltage. The first part consists of the voltage blocking action due to other switches conducting for simultaneous power flow. Thus, in single input mode of operation, only the second part applies. The second part is due to the secondary side voltage, being referred to the primary since the coupled inductor behaves like a transformer. Similarly, the voltage stress on the diode is as expressed in (6), consisting of the voltages referred from the primary side and the dc bus voltage when the diode is in OFF state.

$$V_{SWx\_str} = \begin{Bmatrix} \sum_{i=1}^{N} \left[\left(V_x - V_i \right) D_{ieff} \right] + \\ \left(V_x + V_{dc} \right) \left(1 - \sum_{i=1}^{N} D_{ieff} \right) \end{Bmatrix} \tag{5}$$

$$V_{D\_str.} = \sum_{i=1}^{N} \left(V_i + V_{dc} \right) D_{ieff} \tag{6}$$

The voltage gain of the proposed MIC is a little different from the conventional single input converter. This is because the input voltages are introduced with respect to their effective duty cycles (D_{ieff}). Therefore, the gain is best expressed as the voltage transformation ration (V_{TR}). V_{TR} for the proposed MIC is derived from the output voltage equation and is expressed as (7). For this MIC, VTR can be up to 10*n* at a duty cycle ($\sum_{i=1}^{N} D_{ieff}$) of 90%. This points to the potential for high gain depending on the turns ratio (*n*) of the coupled inductor.

$$V_{TR} = \frac{V_{dc}}{\sum_{i=1}^{N} V_i D_{ieff}} = \frac{1}{1 - \sum_{i=1}^{N} D_{ieff}} n \tag{7}$$

III. RESULTS

The proposed isolated MIC is numerically verified in simulation and validated through hardware-in-the-loop (HIL) implementation using OPAL-RT's OP5700 device running a 64-bit virtex-7 FPGA. Fig. 5 shows the laboratory setup used for the validation and the values of the different component's parameters are presented on Table I.

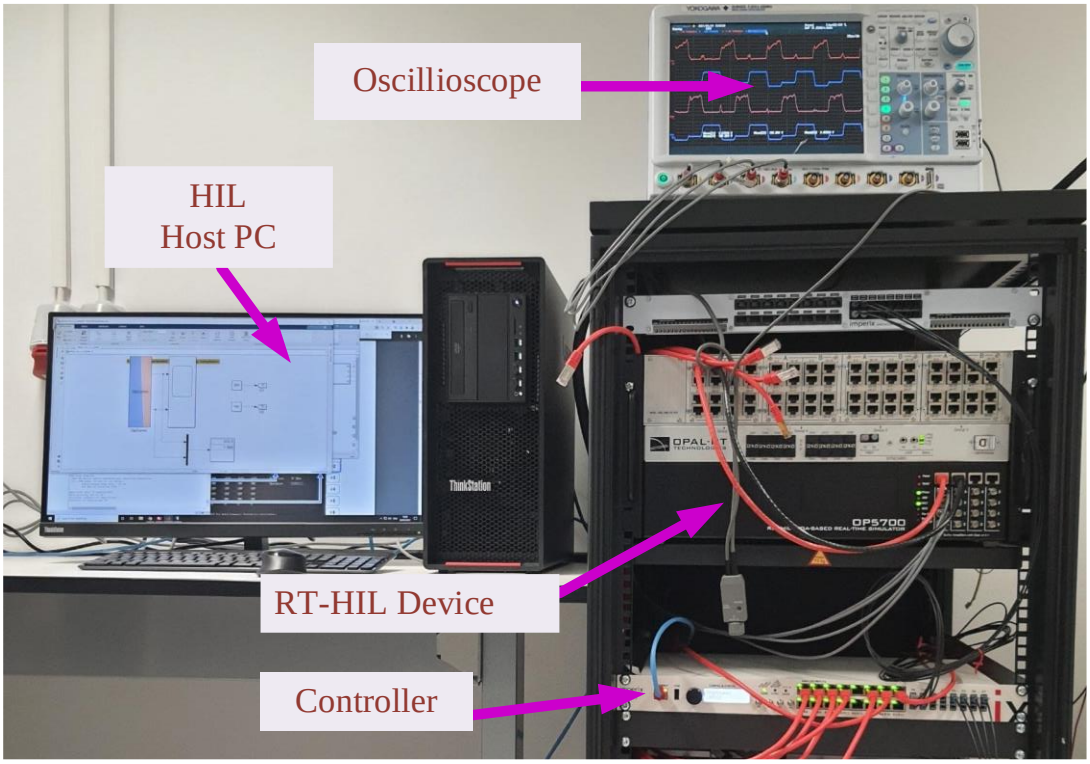

Fig. 5. In-house HIL platform used for validating the MIC.

TABLE I
PARAMETERS USED IN HIL VALIDATION

Parameter	Value	Unit
Magnetising inductance (L_m)	680	mH
Output capacitor (C)	4.7	µF
Voltage sources (V_1/V_2)	200/100	V
Clamp capacitor	47	µF
Clamp resistor	1000	Ω

The verification and validation were implemented in open loop with three different scenarios. The first scenario is selected to have $V_1>V_2$ and so $D_1<D_2$ and the other two scenarios have equal voltages but $D_1<D_2$ in the second scenario and $D_1=D_2$ in the third case. The results are presented in Figs. 6-11 for simulations and HIL implementations, alternately, for the three scenarios. In these results, the currents (i_{V1} and i_{V2}) from each of the sources are presented as well as the voltages across the switches (S_{W1}, V_{SW1}; S_{W2}, V_{SW2}; D, V_D), voltage and current in the primary (V_P and i_P), secondary (V_S and i_S) winding and the dc bus (V_{dc} and i_{dc}). The current in the magnetizing inductance (i_{mag}) is presented only in the simulation results due to the difficulty of measuring it in actual implementation.

In the first scenario, V_1=200 V, V_2=100 V, D_1=0.3, D_2=0.6. The results are presented in Figs. 6 and 7 for simulation and HIL, respectively. Since the input

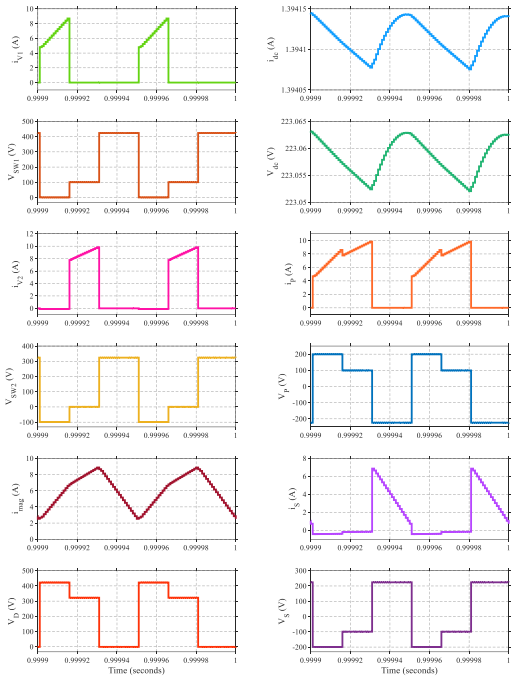

Fig. 6. Simulation results for V_1=200 V, V_2=100 V, D_1=0.3 and D_2=0.6.

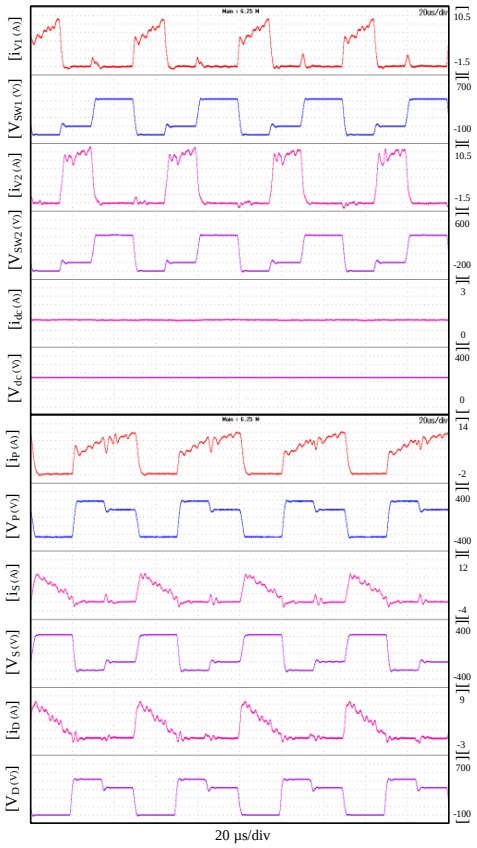

Fig. 7. HIL results for V_1=200 V, V_2=100 V, D_1=0.3 and D_2=0.6.

voltages are different, the current from the sources is time multiplexed so during the first 30% of the switching period (T_S), only V_1 is charging L_m since D_1=0.3, and in the second 30% of T_S only V_2 is charging L_m since D_2=0.6 hence D_{2eff}=0.3. The values of V_{dc} and i_{dc} are about 223 V and 1.4 A with the ripple of V_{dc} being less than 1mV in simulations. In the HIL implementations, V_{dc} and i_{dc} are about 220 V and 1.2 A, thus validating the analytical result of 220 V for V_{dc}.

Similar characteristics are noticed in the second scenario presented in Figs. 8 and 9 for simulation and HIL implementation, respectively, but in this case, V_1=V_2=100 V. Since the voltages are now equal, both V_1 and V_2 are charging L_m at the beginning of T_S, delivering equal amounts of energy. Since D_1<D_2, at the end of D_1, V_2 continues to charge L_m till the end of D_2, thus V_1 is delivering less energy to the dc bus than V_2. The values of V_{dc} and i_{dc} are about 148 V and 0.9 A, respectively, with the ripple of V_{dc} being less than 1mV in simulation while in the HIL implementation V_{dc} and i_{dc} are about 145 V and 0.9 A, respectively, again these results validate analytical result of 150 V for V_{dc}.

The results of the third scenario are presented in Figs. 10 and 11 for simulation and HIL implementation, respectively. This scenario is like the second except that

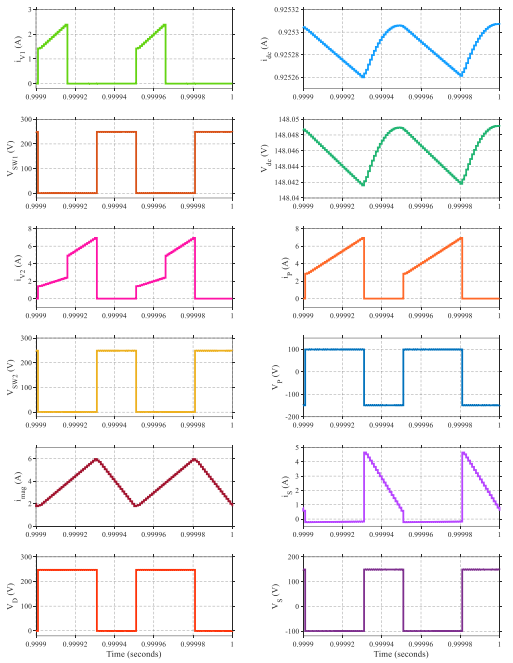

Fig. 8. Simulation results for V_1=V_2=100 V, D_1=0.3 and D_2=0.6.

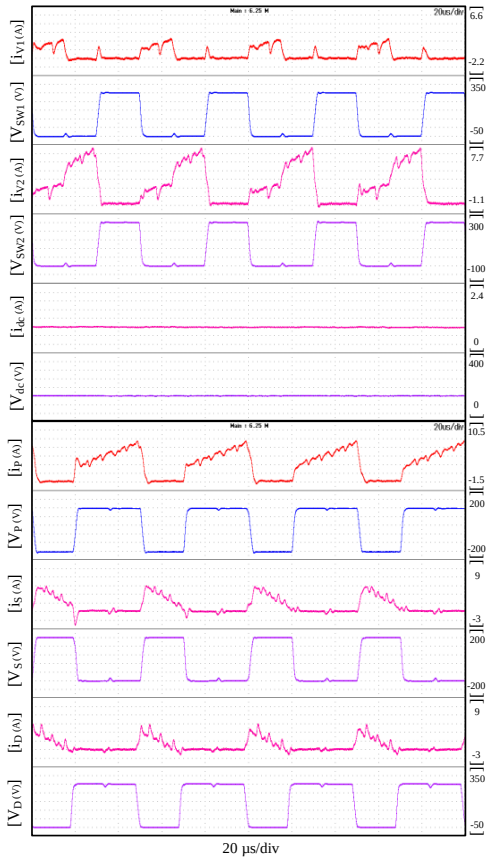

Fig. 9. HIL results for V_1=V_2=100 V, D_1=0.3 and D_2=0.6.

D_1=D_2=0.6. The values of V_{dc} and i_{dc} are like those obtained in the second scenario. The major difference in the third scenario is that since V_1=V_2=100 V and the duty cycles are equal, both sources are delivering equal amounts of energy to the dc bus. With the results presented, the earlier equations (5) and (6) for obtaining the voltage stress on the switches (V_{SW1}, V_{SW2} and V_D) are verified. Also, the selection of L_m is validated since the ripple on the magnetizing current (i_{mag}) in all the three scenarios is under 4 A. Further, in Fig. 12, the V_{TR}-duty cycle relationship of the proposed MIC is compared across analytical calculations, detailed simulation and HIL validation. The MIC's performance in simulation and HIL implementation closely matches the analytical calculation. Since the turns ratio of the coupled inductor used is 1, the highest V_{TR} obtained in all three cases was 10. At V_{TR}<2, the MIC is bucking the input voltages while it is boosting when V_{TR}>2. This result validates the buck-boost and the high gain characteristic of the proposed MIC.

IV. COMPARISON WITH RELATED MIC TOPOLOGIES

To highlight the merits of the proposed isolated MIC, it is compared with other isolated MICs in literature based on the characteristic of allowing simultaneous

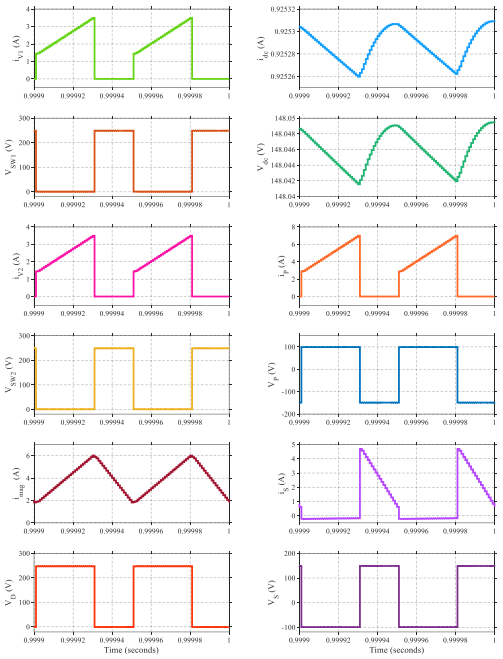

Fig. 10. Simulation results for V_1=V_2=100 V and D_1=D_2=0.6.

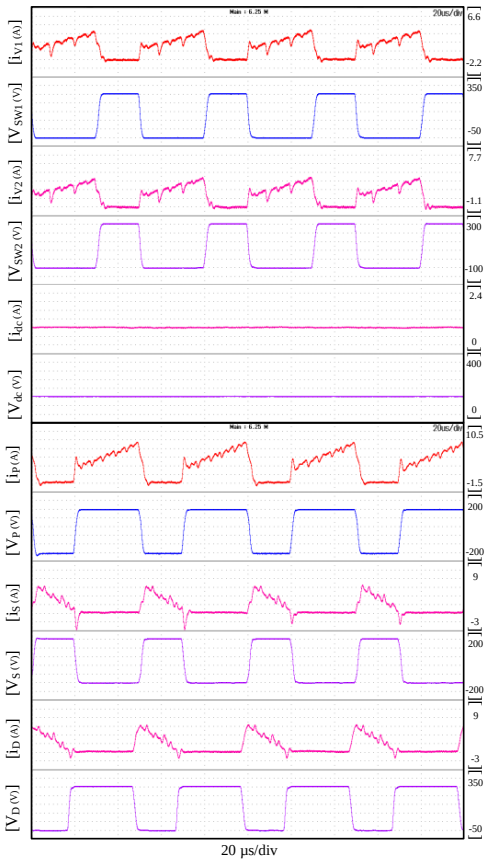

Fig. 11. HIL results for V_1=V_2=100 V and D_1=D_2=0.6.

power flow from the sources. This comparison is presented on Table II, in order of decreasing components needed for two input sources, showing the number of possible inputs, component count, control strategy and operation topology. Further, the modularity, that is the possibility of increasing the number of inputs to the MIC without modifying the core of the magnetic component, is also compared. The MIC in [6] is modular, it has the highest component count, resulting in reduced power density since each input source requires its own transformer. Thus, only the dc bus is shared by the sources and has a complex control strategy requiring PS-PWM. The MICs in [7, 8] proposed require a lower component count than that of [6] for the same number of inputs, but they have a fixed number of input sources as well as complex control strategy, further, the MIC in [7] can only operate in boost mode. The component count of the MICs in [9, 10] is lower than that of [6–8]. Having no restriction on the number of input ports, they both require a fixed magnetic component for any number of input ports, but the control strategy in [9] is PS-PWM. The isolated MIC proposed in this paper combines the advantages of [9, 10], by using a fixed magnetic component, without limitations

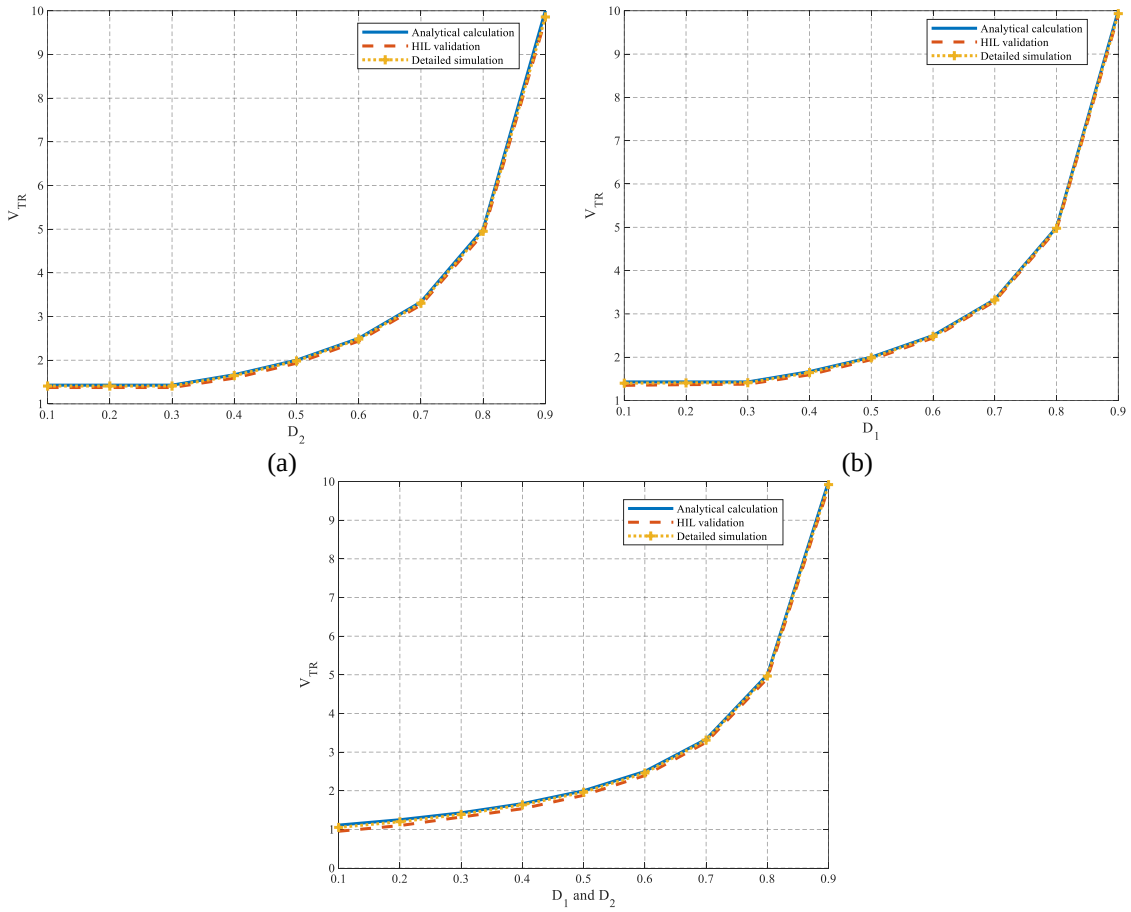

Fig. 12. Obtained V_{TR} where (a) V_1 = 200 V, V_2 = 100 V and D_1 = 0.3 (b) V_1 = V_2 = 100 V and D_2= 0.3 and (c) V_1 = V_2 = 100 V.

TABLE I
COMPARISON WITH RELATED PREVIOUSLY PROPOSED ISOLATED MICS

MIC	Number of inputs	Number of components							Modularity	Control strategy	Operation topology
		S_W	D	L	C	N_P	N_S	Total			
[6]	N	6N	0	2N-1	3N-1	N	N	13N-2	Yes	PS-PWM	MAB
[7]	2	8	8	2	1	2	2	23	No	PS-PWM	Boost
[8]	2	8	4	1	1	2	1	17	No	PS-PWM	MAB
[9]	N	2N+8	0	1	2	1	1	2N+13	Yes	PS-PWM	DAB
[10]	N	N	1	N	N+1	1	1	3N+4	Yes	PWM	Buck-Boost
Proposed	N	N	1	0	1	1	1	N+4	Yes	PWM	Buck-Boost

S_W = active switches, D= diodes, L = inductors, C = capacitors, N_P = number of primary windings, N_S = number of secondary windings, MAB = multi-active bridge, DAB = dual active bridge

on the number of input ports. Further, it requires a smaller number of components and still has a simple control strategy.

V. CONCLUSION

A novel unidirectional multiple input dc-dc converter with magnetic isolation using coupled inductors has been proposed in this research. The proposed isolated MIC has been analysed and validated for two inputs with equal and unequal input voltages at different duty cycles. It was also demonstrated that it features a significant reduction in component count as compared to the counterpart MICs in literature. The results presented in this paper show the verification in simulation and on the in-house hardware-in-the-loop (HIL) platform. The proposed MIC can be implemented for energy harvesting in PV farms and other renewable energy systems with DC voltage sources.

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Paper IV:

Novel Family of High-Gain Nonisolated Multiport Converters With Bipolar Symmetric Outputs for DC Microgrids

This paper has been published as:

I. N. Jiya, H. Van Khang, N. Kishor and R. M. Ciric, "Novel Family of High-Gain Nonisolated Multiport Converters With Bipolar Symmetric Outputs for DC Microgrids," in *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12151-12166, Oct. 2022, doi: 10.1109/TPEL.2022.3176688.

Novel Family of High-Gain Nonisolated Multiport Converters With Bipolar Symmetric Outputs for DC Microgrids

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***Abstract*- Bipolar dc grid systems are fast gaining attraction for renewable energy source (RES) integration, because of their merits of higher reliability, efficiency and robustness as compared to the unipolar dc grids. However, the progress in multiport converters, resulting into lower cost and more compact design for bipolar microgrid systems, is fairly slow. Therefore, this paper proposes a novel family of five non-isolated multiport dc-dc converter topologies with bipolar symmetric outputs. The performance and key operational features of the proposed converters under varying input voltages, duty cycles and loads are numerically verified and experimentally on an in-house test setup to prove the concept of the proposed converters. In the experimental validation, the operation of the converter under simultaneous and arbitrary individual power transfer from two input ports is tested. Further, the easy integration of the proposed converters with a multilevel inverter to achieve high-quality ac voltages is demonstrated. As compared to the few existing counterparts, the proposed converters have a competitive edge in terms of higher number of input ports and voltage gains. Alongside the possibility of arbitrary independent power flow from the input ports, inherently symmetrical outputs require a simple balance control for asymmetrical members of the family.**

Index Terms—Bipolar dc-dc power converter, bipolar dc grid, dc microgrid, high-gain converter, multiport converter, symmetric outputs.

I. INTRODUCTION

Distributed generation systems are the back-bone of future power systems, which are majorly based on dc microgrids, since they have no issues with reactive power and synchronisation beside advantages like lower losses and less conductor material, as compared to the ac microgrids [1–3]. Three-wire dc bus grid systems, called bipolar dc grids (BDCG) as shown in Fig. 1, are fast gaining popularity since they have been recently implemented in telecommunication systems, electric vehicle (EV) and marine vessel charging, data centres and high voltage dc (HVDC) transmission and distribution systems [4–6]. This fast adoption is due to the higher

efficiency because to transmit the same power, the current is smaller in BDCGs than in unipolar dc grids (UDCGs). The reliability of BDCGs is also higher than that of UDCGs because when one of the poles fails, the other pole can continue to transmit power with reduced capacity. Further, BDCGs offer an easier and better-quality conversion from dc to ac voltage using multilevel inverters (MLIs), due to the three voltage levels ($\pm\frac{V_o}{2}$ and V_o) while UDCGs offer only one voltage level. With these attractive features of BDCGs, RESs and dc loads can be more easily integrated by dc-dc converters [7]. However, many sources and loads are uniquely voltage-different, requiring many single-input single-output (SISO) dc-dc converters to step-up or step-down the voltage to or from the BDCG system. Consequently, high component count in addition to bulky and complex configurations, and high cost, amidst global semiconductor chip shortages are the major reluctances of using SISO dc-dc converters in BDCG systems [8, 9]. Multiport dc-dc converters (MPCs) recently proposed in [10–14] can address the mentioned problems in conventional SISO converters.

Proposing novel MPCs with and without galvanic isolations have gained a great attention in recent years. In [15–20], MPCs with multiple-inputs and single-outputs (MISO) have been proposed for renewable energy system integration with features such as reduced component count and simplified control strategy, but they are all

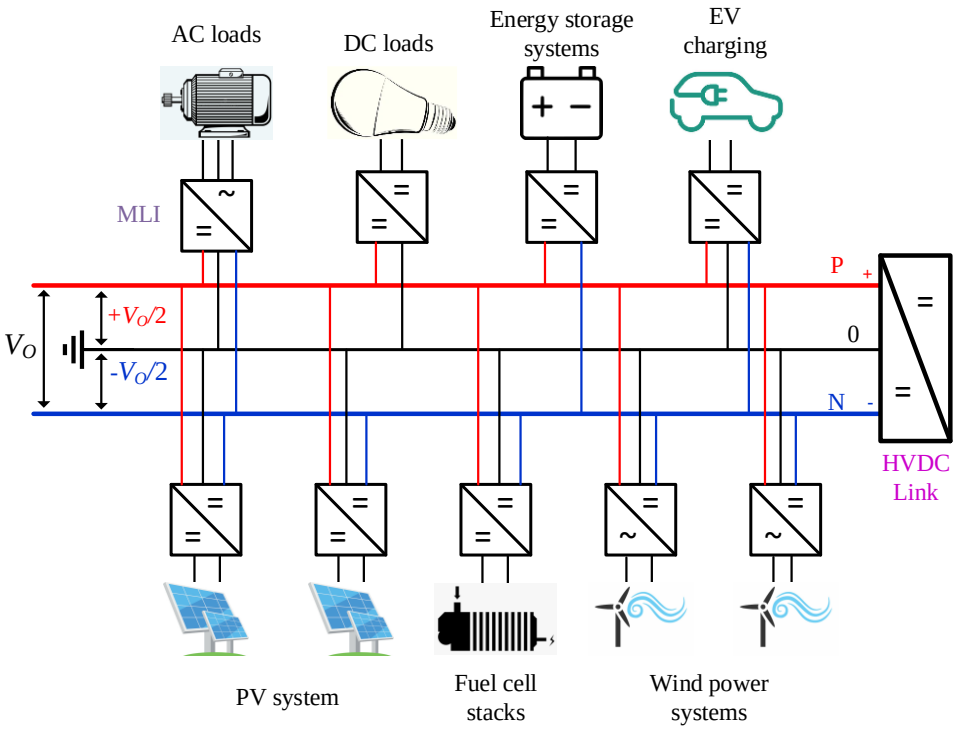


Fig. 1. Structure of a bipolar dc grid (BDCG) system.

unsuitable for BDCG systems because they have only one output port. To overcome this, MPCs with multiple inputs and outputs (MIMO) have been proposed in [21–24]. However, these MIMO MPCs must deal with cross-regulation of the voltage at the output ports, requiring complex controllers to suppress this problem. Bipolar dc-dc converters (BDCs), typically having only symmetrically positive and negative outputs, were therefore proposed in [25–30]. These BDCs based on SEPIC, half-bridge, full-bridge and dual active bridge (DAB) converters are all SIMO converters, thus being limited to only one input source enumerated earlier for SISO converters. To resolve this, multiport bipolar dc converters (MBDCs) have been proposed recently in [31–34], in which the isolated MBDCs proposed in [31, 32] feature soft switching in some cases. Due to the use of transformers or coupled inductors for isolation, they yield generally bulky designs with higher component count, lower efficiency, higher magnetic interference, weight constraints, and lower power density [35], as compared to the non-isolated MBDCs in [33, 34]. To our knowledge, the non-isolated MBDCs in [33, 34] are the most promising solutions for non-isolated MBDCs so far in literature. However, like the isolated counterparts in [31, 32], they are restricted to have two inputs, and cannot be extended for an arbitrary number of inputs, which is a key feature of MPCs. Further, they both cannot allow for an arbitrary independent power flow from either of the input sources to the bipolar dc bus, aside the low voltage gain feature and the requirement for complex control to achieve balanced symmetric output voltages in [33], and using high component count in [34]. Further, fewer MPCs with bipolar symmetric outputs exist for dc microgrids or integrating RES in literature as compared to the unipolar counterparts.

In this paper, a novel family of five non-isolated MBDCs (MBDC types A to MBDC type E) is proposed to fill the aforementioned gaps. These MBDCs have the following salient and novel features:

1) Number of input ports can be arbitrarily increased without much modification to the existing MBDC, by introducing only the respective input ports' active switch.
2) Independent power flow can be carried out arbitrarily from either of the input sources to the bipolar dc link.
3) The bipolar output voltages of MBDC types A to C are inherently symmetrical while types D and E require a simple open loop control alone to keep the bipolar outputs symmetrical.

4) Having higher voltage gains than the counterpart non-isolated MBDCs in literature, which is an attractive feature for application in RES penetrated BDCG transmission and distribution systems.
5) Inductor time-multiplexing is used to achieve simultaneous power transfer from more than one input port of different voltage levels, keeping the part count fixed for any number of inputs.
6) A single input single output (SISO) controller, such as the standard double loop PI controller, is sufficient to control the output voltages despite the multiple ports of the converters.
7) Using switched inductor cells allows the proposed family of MBDCs to yield even higher voltage gain than the previously proposed one in [36].

Within this framework, the proposed novel family of MBDCs was first analysed for two input sources of equal and unequal input voltage levels under simultaneous power transfer from both sources. The analysis is then numerically verified in detailed simulations, and experimentally validated with key results presented. Finally, the integration of the proposed MBDCs with future dc-ac conversion systems was also demonstrated alongside key simulation results by integrating one of the proposed MBDCs with the multilevel inverter (MLI) proposed in [37].

II. PROPOSED CONVERTERS

The proposed family of multiport bipolar dc-dc converters (MBDCs) is presented in Fig. 2. It consists of five unidirectional non-isolated MBDCs, which are derived from the basic buck-boost converter. They all have bipolar symmetric outputs, and the first three members, MBDC types A-C, have their bipolar outputs derived from the Greinacher voltage doubler (GVD) while the last two, MBDC types D and E, have their bipolar outputs derived from a synchronous buck converter (SBC). The MBDCs with bipolar outputs based on the GVD have a higher component count than those with bipolar outputs based on the SBC, but their control complexity is lower since the bipolar outputs do not need any controller to balance the output voltage as required in SBC output based MBDCs. Further, the MBDCs with two inductors (L_1 and L_2) switched by three diodes (D_1–D_3) at the dc conversion stage have higher gains than those with only one (MBDC types A and D). The switched inductor cells implemented to achieve high gain were first proposed in [36], but its application in the proposed MBDC types B, C and E yields at least two times (2x) higher gain than that in [36]. Furthermore, they are all capable of simultaneous and independent power flow from the input ports to the bipolar dc links, being capable

of producing three voltage levels, $\pm\frac{V_o}{2}$ and V_o. The proposed family of MBDCs allows for integrating RESs such as PV systems, wind turbine and fuel cells to a bipolar dc bus. For analysis, the input sources are referred to as basic dc sources V_1–V_N. The following subsections present the steady state analysis of the MBDCs in detail.

A. Steady State Analysis of MBDC type A

The MBDC type A in Fig. 2 (a) consists of five diodes, one inductor, four capacitors and *N*+1 reverse blocking switches, where *N* is the number of input ports to the MBDC. The capacitors, C_1 – C_4 and the diodes D_{g1} – D_{g4} are responsible for the bipolar output stage based on the GVD. Meanwhile, switches S_1 – S_{N+1}, diode D_1 and inductor L, are responsible for the dc conversion stage. For MBDC type A with two inputs, Fig. 3 (a) describes the path of current during the MBDC's operation during simultaneous power transfer from the two input ports to the dc link. Further, the steady state waveforms of this MBDC's operation with two inputs simultaneously for two scenarios, when the voltage of both input ports are equal ($V_1 = V_2$) and when they are unequal ($V_1 > V_2$) is presented in Fig. 3 (b). For both scenarios, the switching period is divided into two main parts $\sum_{i=1}^{N} D_{ieff}$ and $1 - \sum_{i=1}^{N} D_{ieff}$. The first parts D_{1eff} and D_{2eff} are essentially D_{ieff}, since the

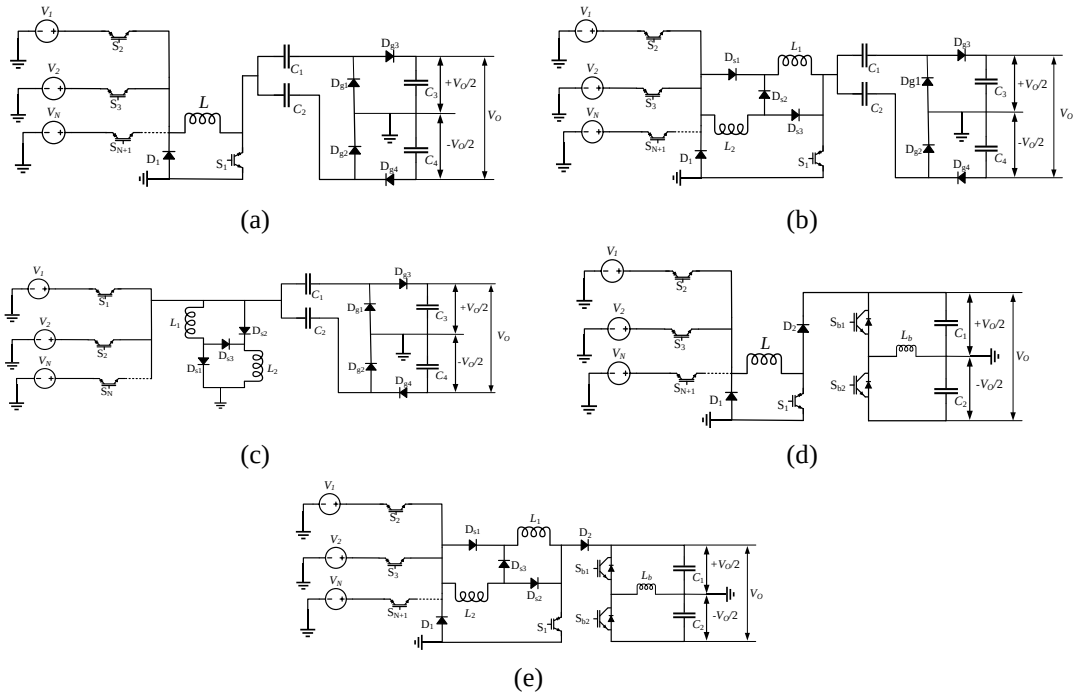
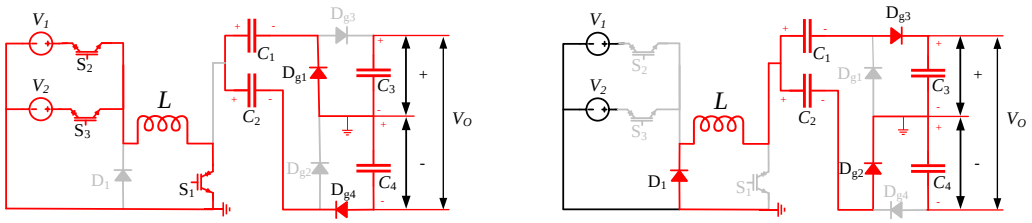


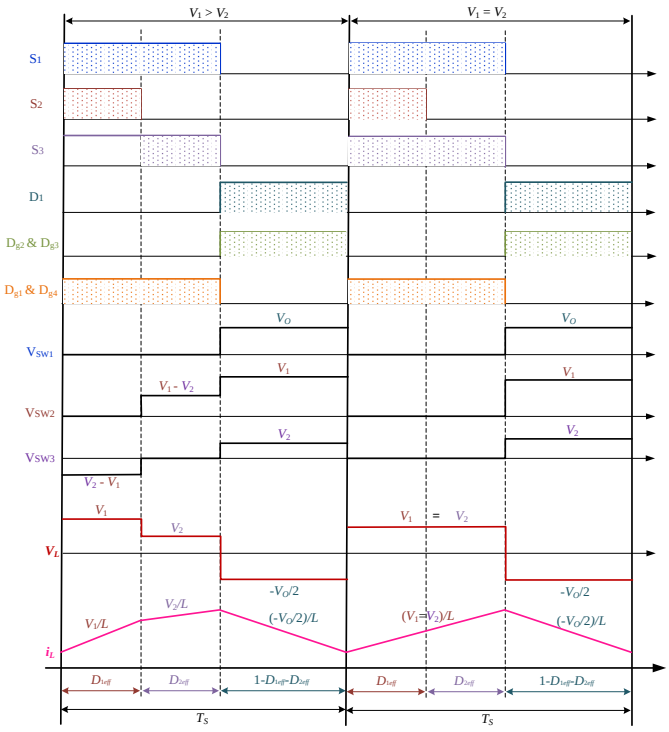
Fig. 2. Proposed Family of five MBDCs with (a) MBDC type A with GVD, (b) MBDC type B with GVD, (c) MBDC type C with GVD, (d) MBDC type D with SBC and MBDC type E with SBC.

MBDC is analysed for two voltage sources, referring to the effective time during which the sources are charging the inductor while the second main division, $1 - D_{1eff} - D_{2eff}$, is the discharging of the inductor.

All the switches S_1 – S_3 are turned ON at the same time during the switching period, T_S, with S_2 turned off and the end of D_{1eff} to end the inductor charging by V_1 and then V_2 is allowed to continue charging the inductor to until both S_1 and S_3 are turned OFF at the end of D_{2eff}. The inductor is charging with a slope of $\left(\sum_{i=1}^{N} D_{ieff} V_i\right)/L$ during which diodes D_{g1} and D_{g4} are discharging capacitors C_1 and C_2 to the dc link. At the end of the inductor charging time, it discharges to the dc link with a slope of $(-V_O/2)/L$ through D_1, D_{g2} and D_{g3}. The same charging and discharging actions of the inductor are observed when the input voltages are equal ($V_1 = V_2$). Similarly, in single input mode, i.e when only one of the sources



(a)



(b)

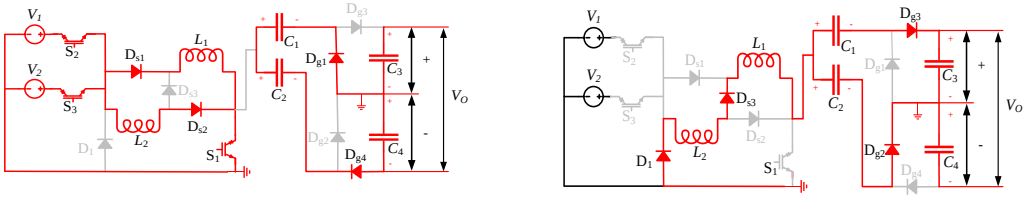
Fig. 3. MBDC type A with (a) path of current flow for inductor charging and discharging time, respectively, and (b) steady state CCM waveforms.

is supplying the dc link, the inductor is charged with a slope of V_i/L during D_i for the respective input port. By applying volt-second balance on the steady state waveforms in Fig. 3 (b), the output voltage, V_o, of MBDC type A is described by (1).

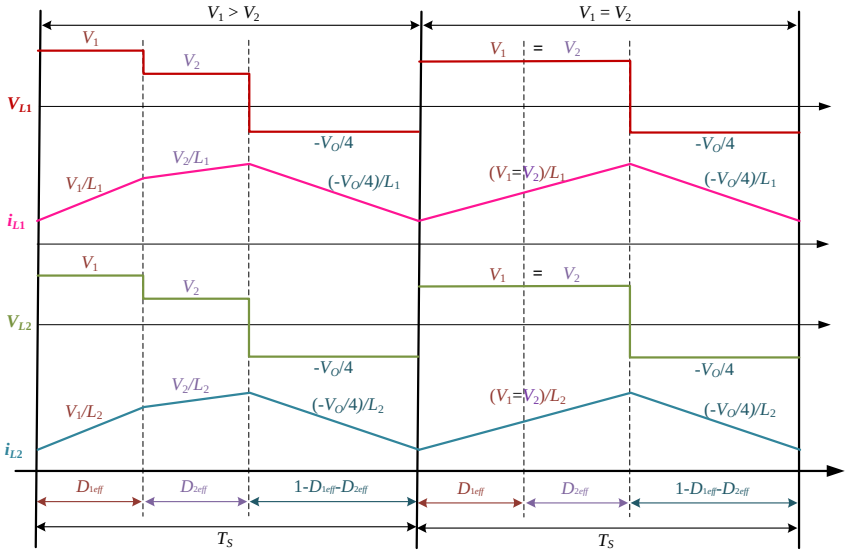
$$V_o = 2\left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right)\Big/\left(1-\sum_{i=1}^{N} D_{ieff}\right)\right] \tag{1}$$

B. Steady State Analysis of MBDC type B

Fig. 2 (b) presents the topology of MBDC type B, consisting of N+1 reverse blocking switches, eight diodes, two inductors and four capacitors. Like MBDC type A, C_1 – C_4 and the diodes D_{g1} – D_{g4} are also responsible for the bipolar output stage based on the GVD while the other components are responsible for the dc conversion stage with D_{s1} – D_{s3}, L_1 and L_2, forming the diode switched inductor component of the MBDC. Through the diode switched inductor component, MBDC type B can achieve a higher output voltage than MBDC type A. For the analysis of MBDC type B with two input voltages, the path of current flow is presented in Fig. 4 (a), and the steady state waveforms are shown in Fig. 4 (b).



(a)



(b)

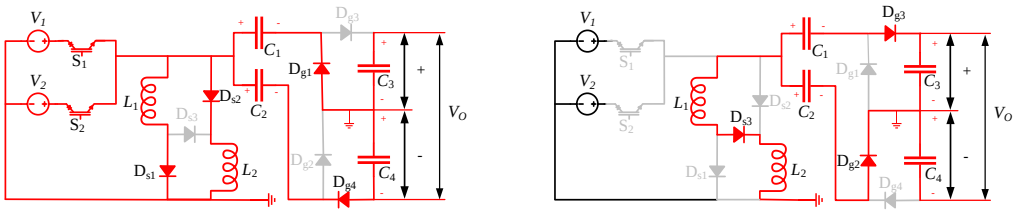
Fig. 4. MBDC type B with (a) path of current flow for inductor charging and discharging time, respectively, and (b) steady state CCM waveforms.

From these Figs, it can be observed that the operation of MBDC type B is similar to that of type A except that the inductor L in MBDC type A is split into two, L_1 and L_2, in MBDC type B through the switched diodes. During the charging of L_1 and L_2, D_{s1} and D_{s2} are forward biased, and each inductor is charged with a slope of $\left(\sum_{i=1}^{N} D_{ieff} V_i\right)/L$, so in the discharging mode, D_1 and D_{s3} are forward biased while the inductor slope is $(-V_O/4)/L$ for each inductor. By applying volt-second balance on the steady state waveforms presented in Fig. 4 (b), the output voltage, V_o, for MBDC type B is described by (2).

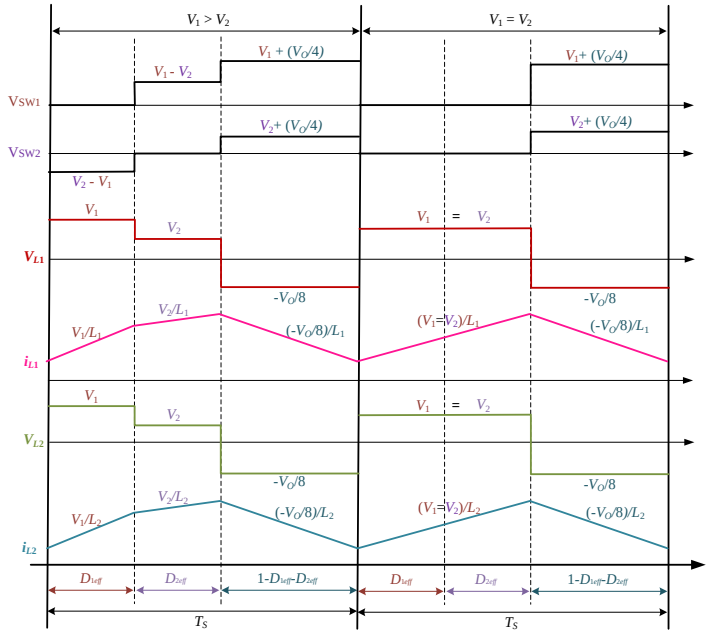
$$V_o = 4\left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right)\Big/\left(1-\sum_{i=1}^{N} D_{ieff}\right)\right] \tag{2}$$

C. Steady State Analysis of MBDC type C

The topology of MBDC type C is presented in Fig. 2 (c), consisting of N reverse blocking switches, seven diodes, two inductors and four capacitors, resulting in one less reverse blocking switch and diode than MBDC type B. For the analysis of



(a)



(b)

Fig. 5. MBDC type C with (a) path of current flow for inductor charging and discharging time respectively and (b) steady state CCM waveforms.

MBDC type C with two input voltages, the path of current flow is presented in Fig. 5 (a), and the steady-state waveforms are shown in Fig. 5 (b). Like MBDC type B, capacitors $C_1 - C_4$ and the diodes D_{g1}–D_{g4} are also responsible for the bipolar output stage based on the GVD while D_{s1}–D_{s3}, S_1–S_N, L_1 and L_2 are responsible for the dc conversion stage. In MBDC type C, diode switched inductor components are directly connected to ground, thus the currents through L_1 and L_2 are higher than those of MBDC type B. Therefore, although each inductor is charged with a slope of $\left(\sum_{i=1}^{N} D_{ieff} V_i\right)/L$ when D_{s1} and D_{s2} are forward-biased during $\sum_{i=1}^{N} D_{ieff}$, each inductor discharges with a slope of $(-V_O/8)/L$. However, the bipolar bus is also connected to the input ports through S_1 – S_N, thus the stresses on S_1 – S_N, are higher than those of S_1 – S_{N+1} in MBDC types A and B. By applying volt-second balance on the steady state waveforms presented in Fig. 5 (b), the output voltage, V_o, for MBDC type C is described by (3).

$$V_o = 8\left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3}$$

D. Steady State Analysis of MBDC types D and E

The circuit topologies for MBDC types D and E are presented on Fig. 2 (d) and (e), respectively, except that the GVD based bipolar dc bus is replaced with a SBC based bipolar dc bus. MBDC type D has two capacitors and four diodes less than MBDC type A, but one half-bridge switch is introduced alongside diode, D_2, and inductor, L_b, in MBDC type D. For the analysis of MBDC type D with two input voltage sources, the path of current flow is presented in Fig. 6 (a) and the steady state waveforms are shown in Fig. 6 (b). The operation of MBDC type D is similar to that of MBDC type A except that during the discharging of the inductor, both D_1 and D_2 are forward-biased. Further, the bipolar dc bus switches S_{b1} and S_{b2} are independently and synchronously controlled with a constant duty cycle of 50% to ensure that the bipolar output voltages, $\pm\frac{V_o}{2}$, are balanced irrespective of the possible imbalance in the loads applied across the different poles. Although an additional control is required, the open loop control is sufficient to maintain balanced output voltages.

Similarly, MBDC type E has two capacitors and four diodes less than MBDC type B, but like MBDC type D, one switch half-bridge, diode, D_2, and inductor, L_3, are introduced. Comparing the path of current flow presented in Fig. 7 (a) and the

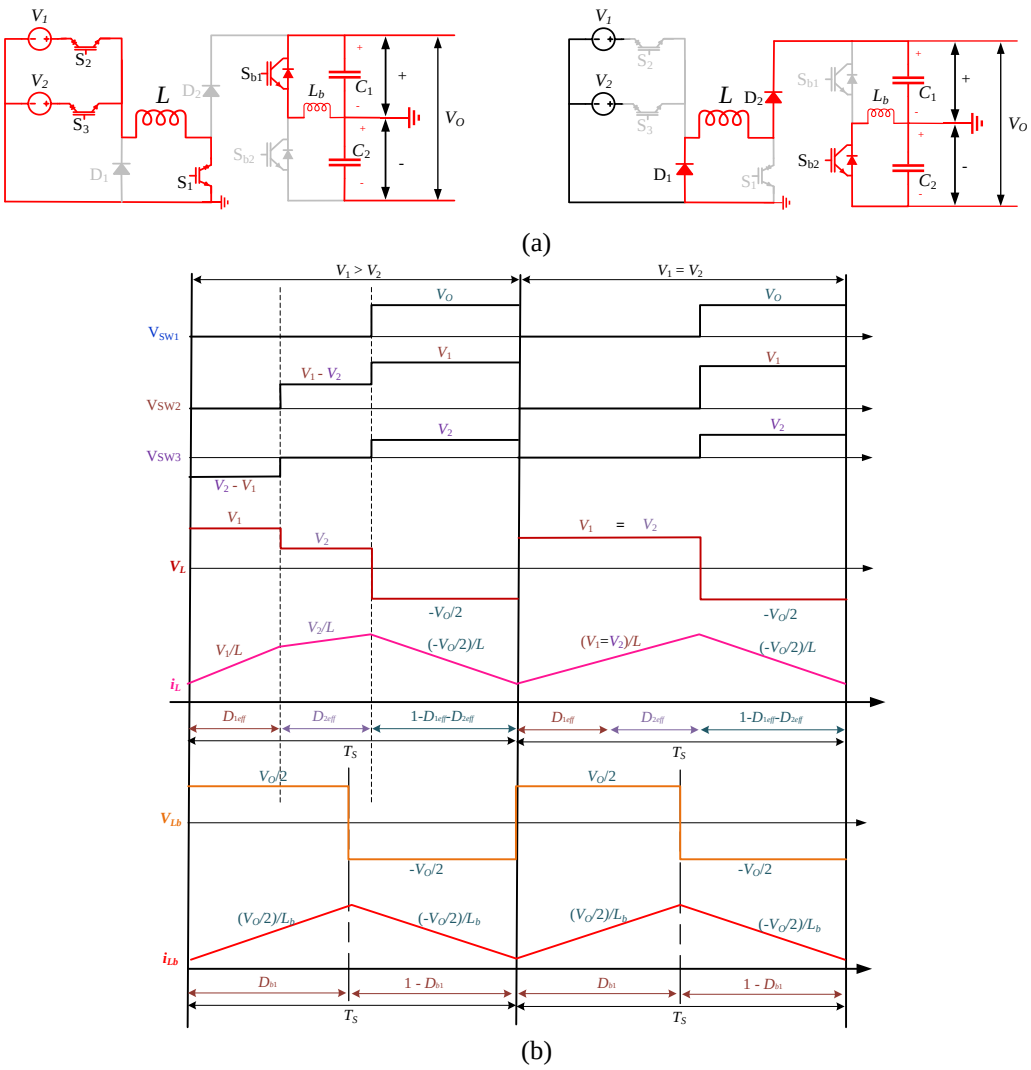


Fig. 6. MBDC type D with (a) path of current flow for inductor charging and discharging time respectively and (b) steady state CCM waveforms.

steady state waveforms in Fig. 7 (b) for the analysis of MBDC type E with two input voltage sources, to that of MBDC type B, it can be observed that they are both similar except that when the inductors, L_1 and L_2, are discharging, diodes D_1, D_2 and D_{s3} are forward-biased. Further, its bipolar dc bus behaves exactly as that of MBDC type D. By applying volt-second balance on the steady state waveforms of MBDC types D and E, the output voltages are the same as those of MBDC types A and B, being defined by (1) and (2), respectively.

E. Independent Power Flow

One key feature of the proposed family of MBDCs is that independent power flow from the input sources to the bipolar dc link can be carried out arbitrarily. To achieve this, the switch controlling the input port, which is not required to supply the dc link, is turned OFF throughout the switching period. For example, if V_1 is

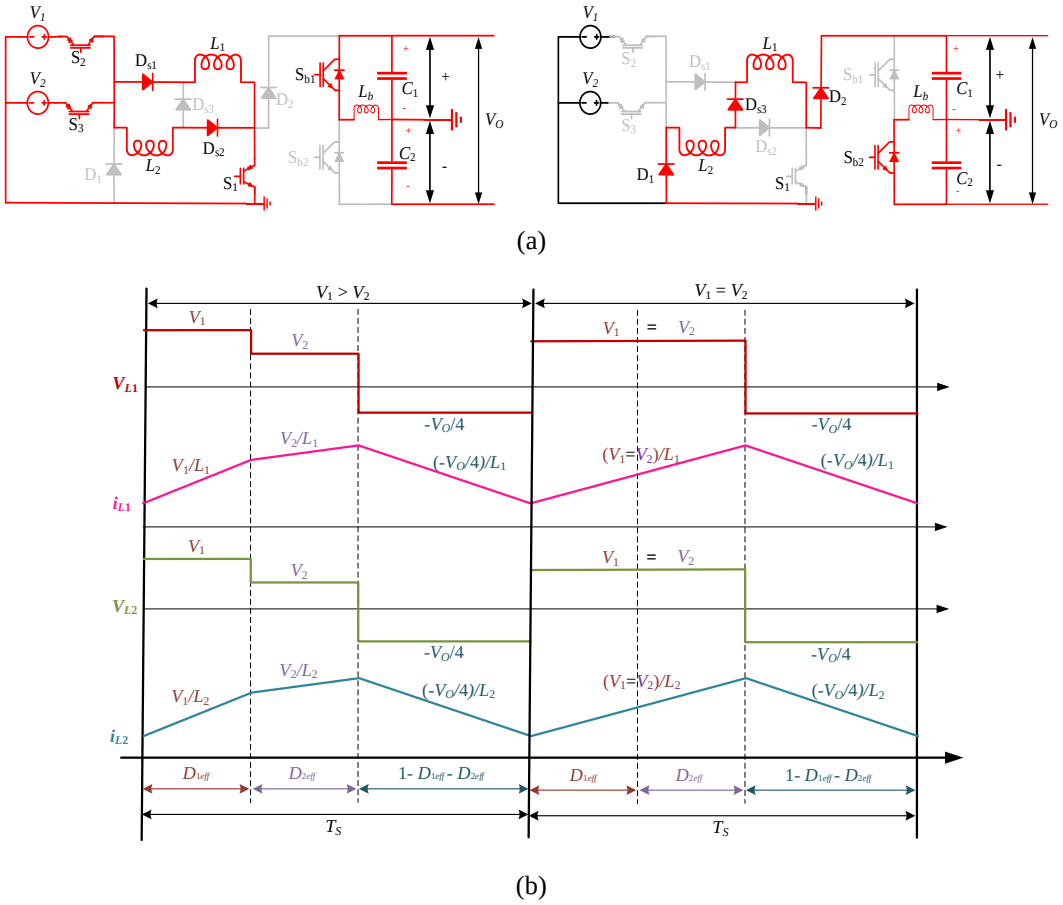


Fig. 7. MBDC type E with (a) path of current flow for inductor charging and discharging time, respectively and (b) steady state CCM waveforms.

required to supply the dc link for MBDC type A, during the inductor charging time (D_{ieff}), S_1 and S_2 are turned ON with the same duty cycle (D_{1eff}). After this, the inductor discharges through forward-biasing D_1 exactly as described earlier during simultaneous power flow mode, while S_3 is left OFF for the entire switching period. Similarly, if V_2 is required to supply the dc link, S_1 and S_3 are turned ON with the same duty cycle (D_{2eff}) during the inductor charging time (D_{ieff}) while S_2 is left OFF for the entire switching period. Further, arbitrary independent power flow is achieved in similar fashion for all the other members of the family, including in MBDC type C for which the switch controlling the input sources V_1 and V_2 are named S_1 and S_2, respectively.

F. Effective Switch Commutation and Voltage Stress

For an effective operation of the MBDCs in simultaneous power transfer from the input ports to the dc link, some principles need to be respected. When the voltages are unequal, the sources are arbitrarily arranged in the controller in order of decreasing magnitude such that $V_1 > V_2 > \cdots > V_N$ for N input ports, the duty

cycle of the switches controlling the respective input ports (i.e., S_2 to S_{N+1} for MBDC types A, B, D & E and S_1 to S_N for type C), must be in such a way that $d_1 < d_2 < \cdots < d_N$ and vice versa, where $d_1 = D_{1eff}$, $d_2 = D_{1eff} + D_{2eff}$, ⋯, $d_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. If the source voltages are equal, such that $V_1 = V_2 = \cdots = V_N$, the duty cycles controlling the respective input sources can be equal or in order of increasing the magnitude of power required from each respective source. However, in all cases except type C, the duty cycles applied to S_1 for all the MBDCs must be the maximum duty applied to the switches controlling the input ports i.e., $d_{max} = {}_{i=1}^{N}[max.\, d_i] = d_N$. Further, it is important to note that for simultaneous power transfer to take place, switches S_1 to S_N (for type C) and S_1 to S_{N+1} (for the other types) must be implemented using reverse blocking switches. These reverse blocking switches which have recently received attention in literature [38], prevent reverse conduction prevalent in the traditional switches.

Ignoring the parasitics, the voltage stresses on the switches and diodes are described in (4-11). $S_{i+1} - S_{N+1}$ and $S_i - S_N$ are the voltage stresses on the switches controlling the input ports for MBDC types A, B, D, E and MBDC type C, respectively, where V_x is the respective port voltage. The first part of (5) and (6) is due to the voltage blocking action when other switches are conducting during simultaneous power flow while the second part is when the switch is turned OFF. Therefore, in single input mode, i.e when only one source is supplying power to the bipolar dc link, the second part of the equations is applied. It is obvious that although MBDC type C has less switches as compared to types A and B, and the highest output voltage among the proposed MBDCs, its switches also undergo the highest voltage stress. Further, the voltage stresses for the capacitors and inductors are presented in (12-16) respectively.

$$\underset{typesA,B,D\&E}{V_{S_1}} = \frac{V_o}{2}\alpha; \quad \alpha = 1 - \sum_{i=1}^{N} D_{ieff} \tag{4}$$

$$\underbrace{V_{S_{i+1}} \cdots V_{S_N}}_{typesA,B,D\&E} = \sum_{i=1}^{N}\left(V_x - V_i\right)D_{ieff} + \left(V_x\alpha\right) \tag{5}$$

$$\underbrace{V_{S_1} \cdots V_{S_N}}_{typeC} = \left[\sum_{i=1}^{N}\left(V_x - V_i\right)D_{ieff}\right] + \left[\left(V_x + \frac{V_o}{4}\right)\alpha\right] \tag{6}$$

$$\underset{typesA,B,D\&E}{V_{D_1}} = \underset{typesD\&E}{V_{D_2}} = \underset{typesB,C\&E}{V_{D_{s3}}} = \sum_{i=1}^{N} V_i D_{ieff} = \gamma \tag{7}$$

$$V_{D_{s1}\&D_{s2}} = \underbrace{(V_O/4)\alpha}_{typesB\&E} = \underbrace{(V_O/8)\alpha}_{typeC} \tag{8}$$

$$V_{D_{g1}} = V_{D_{g4}} = \underbrace{\sum_{i=1}^{N}\left[V_i + (V_O/4)\right]D_{ieff}}_{typeC} = \underbrace{(V_O/2)\alpha}_{typesA\&B} \tag{9}$$

$$\begin{aligned} V_{D_{g2}} = V_{D_{g3}} &= \underbrace{\left[\sum (V_x - V_i)D_{ieff} + \left(\max V_i + \tfrac{V_o}{4}\right)\beta\right]_{i=1}^{N}}_{typeC} \\ &= \underbrace{(V_O/2)\beta}_{typesA\&B};\quad \beta = \sum_{i=1}^{N} D_{ieff} \end{aligned} \tag{10}$$

$$\underbrace{V_{S_{b1}} = V_{S_{b2}}}_{typesD\&E} = \underbrace{V_{C_1} = V_{C_2}}_{typesD\&E} = \underbrace{V_{C_3} = V_{C_4}}_{typesA-C} = V_o/2 \tag{11}$$

$$\underset{typesA-C}{V_{C_1}} = \frac{(V_o/2)\alpha}{\beta} \tag{12}$$

$$\underset{typesA-C}{V_{C_2}} = \frac{(V_o/2)}{\beta} \tag{13}$$

$$V_L = \underbrace{\gamma + \left[(-V_o/2)\alpha\right]}_{typesA\&D} \tag{14}$$

$$V_{L_b} = \underbrace{\left[D_{b1}(V_o/2)\right] + \left[(1-D_{b1})(-V_o/2)\right]}_{typesD\&E} \tag{15}$$

$$V_{L_1} = V_{L_2} = \underbrace{\gamma + \left[(-V_o/4)\alpha\right]}_{typesB\&E} = \underbrace{\gamma + \left[(-V_o/8)\alpha\right]}_{typeC} \tag{16}$$

G. Voltage Gain

Aside the merits of low component counts, the high voltage gain is another important feature of the proposed MBDCs. Because the input voltages of multiport dc-dc converters are introduced with respect to their effective duty cycles, D_{ieff}, their gain is best described as the voltage transformation factor (V_{TR}) [39]. This is easily derived for the proposed family of MBDCs from their output voltage (V_o) equation. The V_{TR} for the proposed family of MBDCs are expressed in (17).

$$V_{TR} = V_o/\gamma = \underset{typesA\&D}{2/\alpha} = \underset{typesB\&E}{4/\alpha} = \underset{typesB\&E}{8/\alpha} \tag{17}$$

To demonstrate the high gain of the proposed family of MBDCs, V_{TR} is computed for two scenarios: when $V_1 > V_2$ ($V_1 = 100$ V and $V_2 = 75$ V), and $V_1 = V_2 = 75$ V. In the first scenario presented in Fig. 8 (top plot), the duty applied to the respective switching controlling V_1 is kept constant at 0.3 ($d_1 = 0.3$) while d_2 is varied from 0.1 to 0.9. In the second scenario presented in Fig. 8 (bottom plot),

while the duty cycles are equal i.e., $d_1 = d_2$, they are both varied from 0.1 to 0.9. In both cases, the maximum V_{TR} obtainable when $\sum_{i=1}^{N} D_{ieff} = 0.9$, are 80, 40, and 20 for MBDC type C, types B and E, and types A and D, respectively. Further, when $\sum_{i=1}^{N} D_{ieff}$ is at the minimum of 0.1, the resulting gains V_{TR} are about 8.89, 4.44 and 2.22 for MBDC type C, types B and E, and types A and D, respectively. At $V_{TR} > 2$, the MDBC is operating in the boost mode, and vice versa for the buck mode, thus, this proves the high gain boost capabilities of the proposed family of MBDCs.

H. Control Structure

Fig. 9 presents the control structure of the proposed family of MBDCs. The control layer consists of the secondary controller, the double loop PI controller, the power management controller (PMC) and the pulse width modulator (PWM). The secondary controller sets the output voltage reference ($V_{o\text{-}ref}$), depending on the

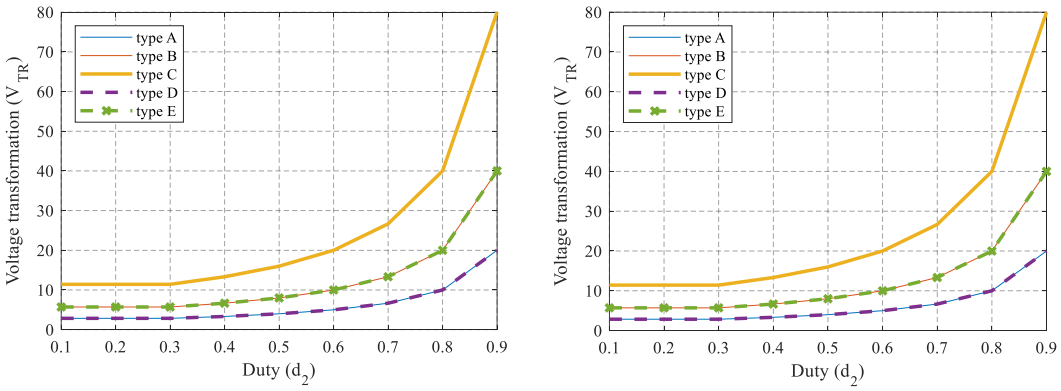


Fig. 8. Gain of the family of MBDCs expressed as V_{TR}.

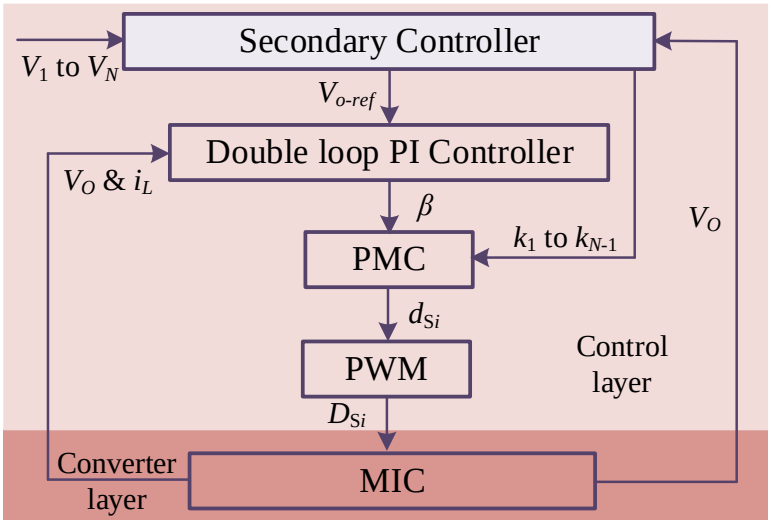


Fig. 9. Control structure of the proposed family of MBDCs.

required operating mode of the MBDC. It is responsible for the proportion of power flow from the sources when operating in a simultaneous power flow mode. To do this, the secondary controller determines scaling factors k_1 to k_{N-1}, which are obtained by comparing the total power capacity (kw_T) of all the sources to the individual power capacities (kw_1 to kw_N) for sources (V_1 to V_N) as in (18), or based on other parameters like the maximum power point tracking (MPPT).

$$\left.\begin{array}{c} \left(kw_T = kw_1 + \cdots + kw_N\right), \end{array}\right. \quad \left.\begin{array}{c} k_1 = \dfrac{kw_1}{kw_T} \\ \vdots \\ k_{N-1} = \dfrac{kw_{N-1}}{kw_T} \end{array}\right\} \tag{18}$$

V_O and i_L are used to determine the control variable β, which is the time required to charge the inductor(s). The non-linear equations of the inductor currents and output capacitor voltages of the MBDCs are presented in (19) are obtained and linearised. Taylor series expansion is used to obtain the inner current and output voltage-loop transfer functions, G_{id}, (20) and G_{vd}, (21). Further, the PI gains of the double loop PI controllers are heuristically selected based on G_{id}, (20) and G_{vd}, (21). The PMC based on the scaling instructions from the secondary controller determines $D_{1eff} - D_{Neff}$ and the respective duty cycles according to (22).

$$\left.\begin{array}{l} \dfrac{di_L}{dt} = \left(\dfrac{\gamma + V_o}{L}\right)\beta - \dfrac{V_o}{L} \\ \dfrac{dV_C}{dt} = \dfrac{i_L(1-\beta)}{C} - \dfrac{V_o}{RC} \end{array}\right\} \tag{19}$$

$$G_{id} = \frac{\left[s\gamma/L\right] + \left[\gamma/RLC\right]}{s\left(s + \dfrac{1}{RC}\right) + \dfrac{1}{LC}} \tag{20}$$

$$G_{vd} = \left[\gamma/LC\right] \Big/ \left[s\left(s + \frac{1}{RC}\right) + \frac{1}{LC}\right] \tag{21}$$

$$\left.\begin{array}{l} D_{1eff} = k_1\beta \\ \vdots \\ D_{N-1eff} = k_{N-1}\beta \\ D_{Neff} = \beta - \sum_{i=1}^{N-1} D_{ieff} \end{array}\right\} , \quad \left.\begin{array}{c} d_1 = D_{1eff} \\ d_2 = D_{1eff} + D_{2eff} \\ \vdots \\ d_{N-1} = \sum_{i=2}^{N-1} D_{ieff} \\ d_N = \sum_{i=1}^{N} D_{ieff} \end{array}\right\} \tag{22}$$

TABLE I
PARAMETERS USED IN VALIDATING THE MBDCS

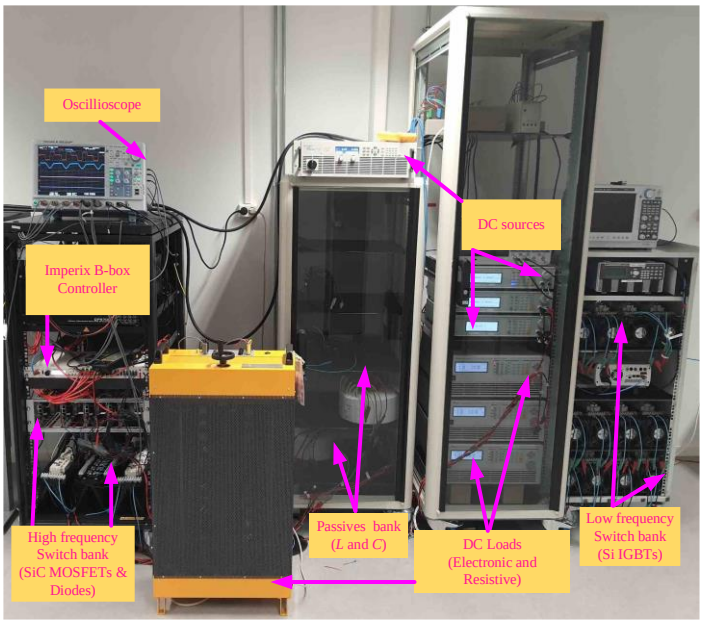
Parameter	Value
Switching frequency (F_{SW})	50 kHz
V_1	100 V
V_2	75 V
L, Hammond – 195E50	2.5 mH/50 A/8 mΩ
$L_b = L_1 = L_2$, Hammond – 195C50	1 mH/50 A/5 mΩ
$C_1 = C_2$, KEMET – ALS70A472NF500	4.7 mF/500 V/59 mΩ
Diodes, SemiQ – GHXS050B065S-D3	650 V/50 A
MOSFETs, CREE – C2M0080120D	1200 V/36 A/80 mΩ

III. RESULTS AND DISCUSSIONS

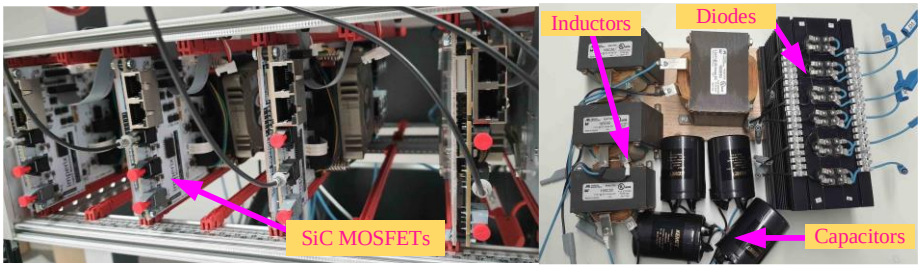
The proposed MBDC topologies have been numerically verified in simulations using Matlab's Simulink. Further, MBDC types D and E were verified on our in-house experimental test setup using the circuit parameters presented in Table I. Fig. 10 shows the experimental test setup, consisting of the high and low switching frequency reconfigurable switch banks, passive component (*L* and *C*) bank, Imperix B-box 3.0 controller, oscilloscope, dc power supplies and loads. To achieve the reverse blocking capability required in S_1 to S_3 in MBDC types D and E, each SiC MOSFET was connected in series to a SiC diode since the reverse blocking WBG devices are not commonly available on the market at this time. Although all five MBDCs proposed were tested in simulations, only results for MBDC types D and E are presented here since only these two topologies were validated on the experimental test platform. The following subsections present the open loop simulation and experimental results for operation under different conditions to authenticate the operation of the proposed MBDC topologies with two input ports. Further, although the proposed MBDCs are capable of independent power flow from the sources, only results for simultaneous power flow is presented since the independent power flow operation is like the conventional single input converters, which are sufficiently addressed in literature.

A. Simulation and Experimental Results for MBDC type D

To validate the operation of MBDC type D, two different scenarios of different and equal input voltages are tested in this section. The simulation and experimental results of the first scenario are presented in Fig. 11 (a and b), respectively. In this scenario, the input voltages are unequal with V_1 = 100 V, V_2 = 75 V, so the duty cycles applied to S_2, S_3 are d_1 = 20%, d_2 = 40% such that $D_{1eff} = D_{2eff}$ = 0.2. A



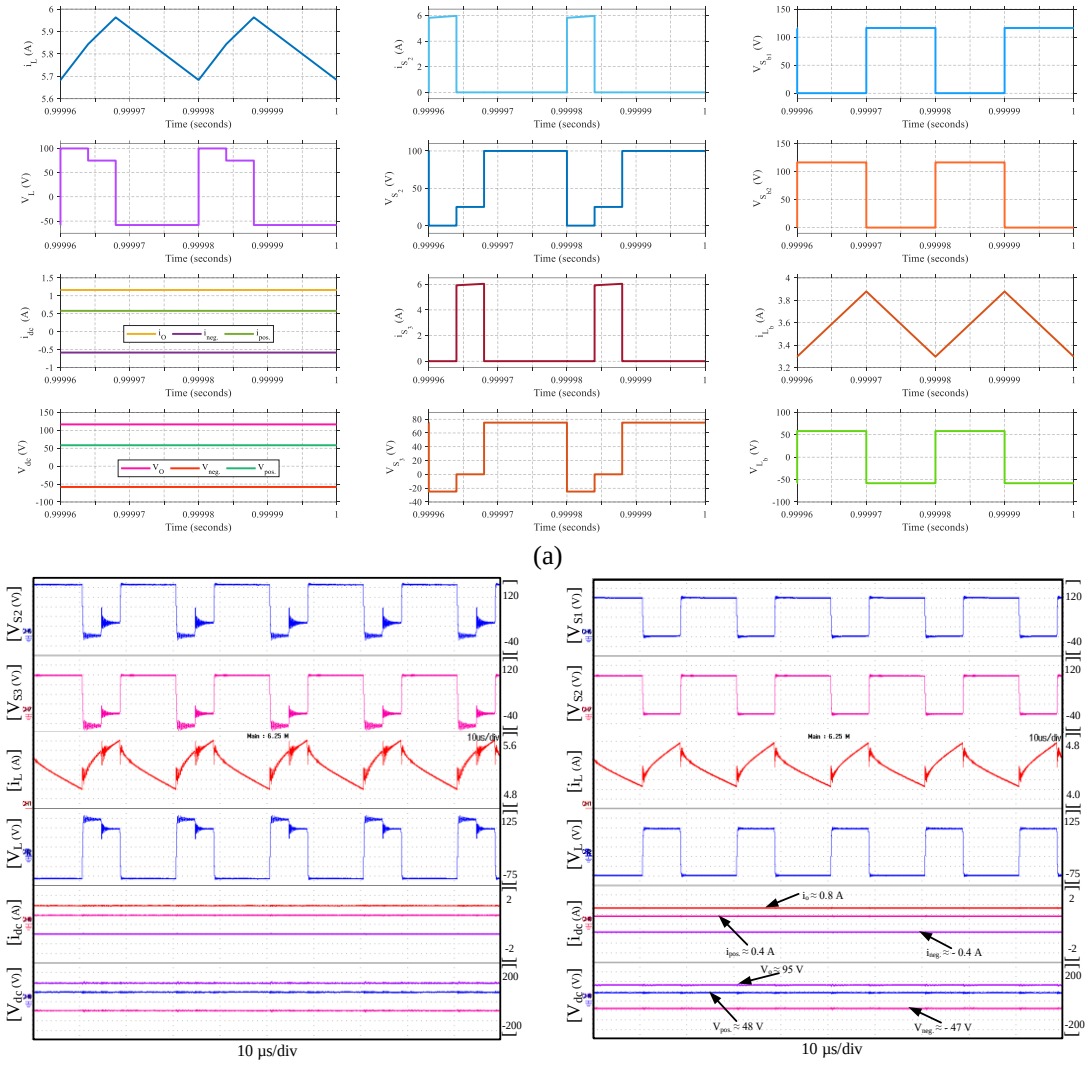
(a)



(b)

Fig. 10. Experimental test setup with (a) overview of the MBDC verification setup and (b) the components used in the implementation.

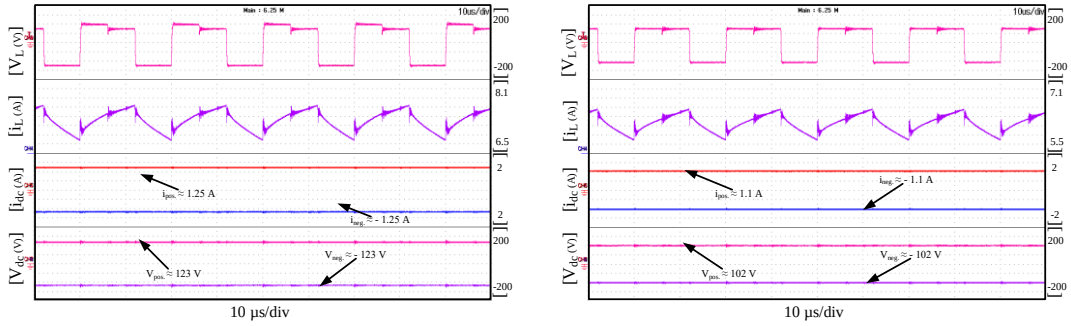
resistive load was used in the verification and was set to 100 Ω for all three levels of the bipolar dc bus. $\pm V_O/2$ and V_O is about ±55 V and 109 V while the current is ±0.5 A and 1 A respectively. This is about 3 V and 7 V drop, while the output currents are ±80 mA and 160 mA lower than the simulation results under similar conditions in Fig. 11 (a). Similarly, i_L and Δi_L is about 5.8 A and 0.3 A for the simulation while the experimental is not so far apart at about 5 A and 0.5 A, respectively. Other parameters presented includes the V_L, the current and voltages of the switches and the inductor of the bipolar dc bus. In the second scenario, $V_1 = V_2 = 75$ V, and the duty cycles applied to S_2, S_3 are $d_1 = d_2 = 40\%$ such that $D_{1eff} = D_{2eff} = 0.4$. The load is also 100 Ω for all three levels of the bipolar dc bus. $\pm V_O/2$ and V_O are about ±48 V and 95 V while the current is ±0.4 A and 0.8 A, respectively in the results of experimental implementation in Fig. 11 (c). Further, the inductor current and its ripple, i_L and Δi_L are about 4.45 A and 0.5 A in the experimental implementation, respectively.



(a) (b) (c)

Fig. 11. Verification results for operating MBDC type D when V_1=100V, V_2=75V, d_1=20% and d_2=40% for (a) simulation (b) experimental implementation and (c) experimental results when V_1=V_2=75V and d_1= d_2=40%.

In both scenarios, the experimental results closely match within 5% with those of simulation and analytical calculations. Further, because the input voltages are different in the first scenario, V_2 only starts to supply the output by charging the inductor after S_2 has been turned off. This is indicated in the switch current and voltage (i_{S2}, i_{S3}, V_{S2} and V_{S3}) controlling the input sources V_1 and V_2, respectively as shown in Fig. 11 (a). While S_2 is conducting, the voltage of S_3 is negative, at about –25 V, which is V_2–V_1, because of its reverse current blocking action. Further, while S_3 is conducting, the voltage of S_2 is about 25 V, which is V_1–V_2, also due to its reverse blocking action. In the second scenario, since both voltages and duty cycles are equal, V_1 and V_2 are supplying equal currents to the load. Furthermore, the bipolar dc bus is kept balanced by applying a duty cycle of 50%



(a) (b)

Fig. 12. Experimental verification of MBDC type D at high duty of d_1=30% and d_2=60% for (a) V_1=100V, V_2=75V, and (b) V_1=V_2=75V.

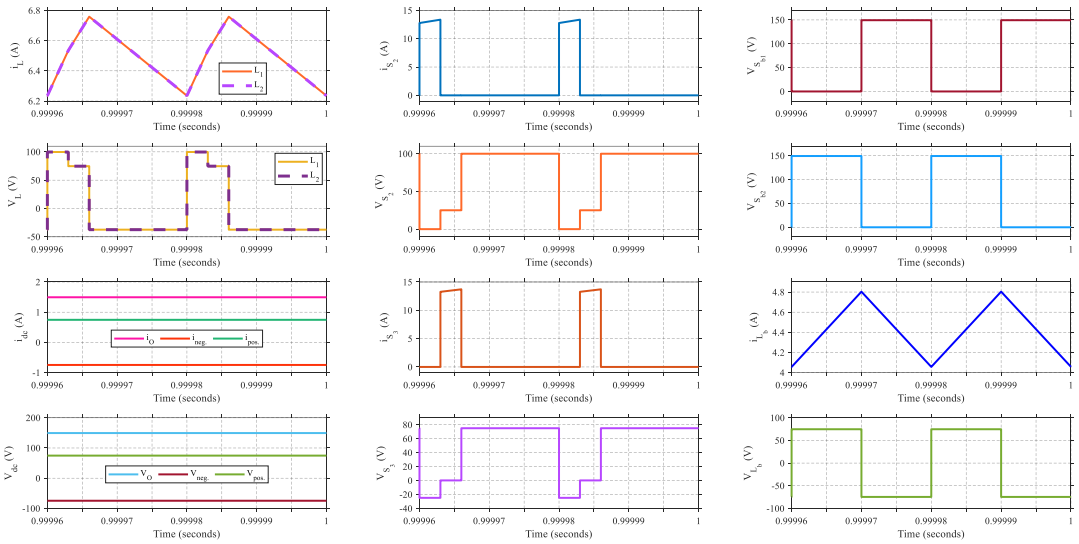
to S_{b1} and S_{b2} in both scenarios. Further, MBDC type D is tested for operation under higher duty cycles (d_1=30% and d_2=60%) to prove its high gain characteristics with results presented respectively in Fig. 12 for unequal (V_1>V_2) and equal (V_1=V_2) input voltages. Under these conditions, the performance of the MBDC is desirable and acceptable when compared to analytical results. All these results validate the expected performance characteristics presented earlier in Fig. 6 for MBDC type D.

B. Simulation and Experimental Results for MBDC type E

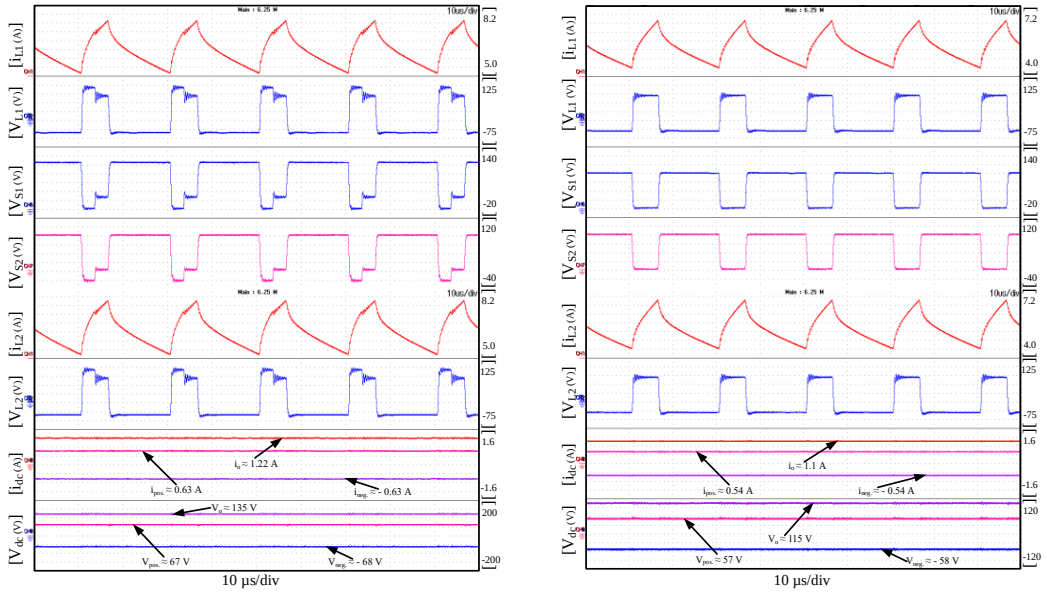
MBDC type E was also validated under two different scenarios like in MBDC type D: different and equal input voltages. In the first scenario of MBDC type E in Figs. 13 (a) and (b), respectively, for simulation and experiment, V_1 = 100 V, V_2 = 75 V is just like in MBDC type D, but in this case, the duty cycles applied to S_2 and S_3 are d_1 = 15% and d_2 = 30% such that D_{1eff} = D_{2eff} = 0.15. The resistive load across each pole of the dc bus was set to 100 Ω. The output voltages obtained in the experimental implementation are about ±68 V and 135 V, which are about 10% drop from the simulation results of ±75 V and 150 V, respectively, for $\pm V_O/2$ and V_O. The output currents in simulations are ±0.75 A and 1.5 A, and about ±0.63 A and 1.22 A in the experimental implementation. Further, the currents and voltages of L_1 and L_2 are equal (i.e., $i_{L1} = i_{L2}$ and $V_{L1} = V_{L2}$) in the simulation and experimental results: $i_{L1} = i_{L2} \approx 6.45$ A, $\Delta i_{L1} = \Delta i_{L2} \approx 0.5$ A in simulations, and $i_{L1} = i_{L2} \approx 6.2$ A, $\Delta i_{L1} = \Delta i_{L2} \approx 2.4$ A in the experiments. In the second scenario of MBDC type E with experimental results presented in Fig. 11 (c), V_1 = V_2 = 75 V and d_1 = d_2 = 30% such that D_{1eff} = D_{2eff} = 0.3, the load at the poles of the bipolar dc bus was set to 100 Ω. The output voltages of the three levels are about ±58 V and 115 V with output currents of about, ±0.54 A and 1.1 A, respectively. Like the

first scenario, the currents and voltages in the inductors are equal, i.e., $i_{L1} = i_{L2}$ and $V_{L1} = V_{L2}$.

The experimental output voltages are about 10% less than those in the simulations, which are slightly higher than obtained for MBDC type D because of the increased losses due to higher component count and higher current flowing through the inductors to achieve the higher voltage gain. Although MBDC type E has a higher gain than MBDC type D, avoiding the potential for increased losses at higher duty cycles must be taken into consideration. Other parameters such as S_{b1}, S_{b2} and L_b behave in MBDC type E as earlier discussed in the MBDC type D. In short, the



(a)



(b) (c)

Fig. 13. Verification results for operating MBDC type E when V_1=100V, V_2=75V, d_1=15% and d_2=30% for (a) simulation, (b) experimental implementation and (c) experimental results when V_1=V_2=75V, d_1=d_2=30%.

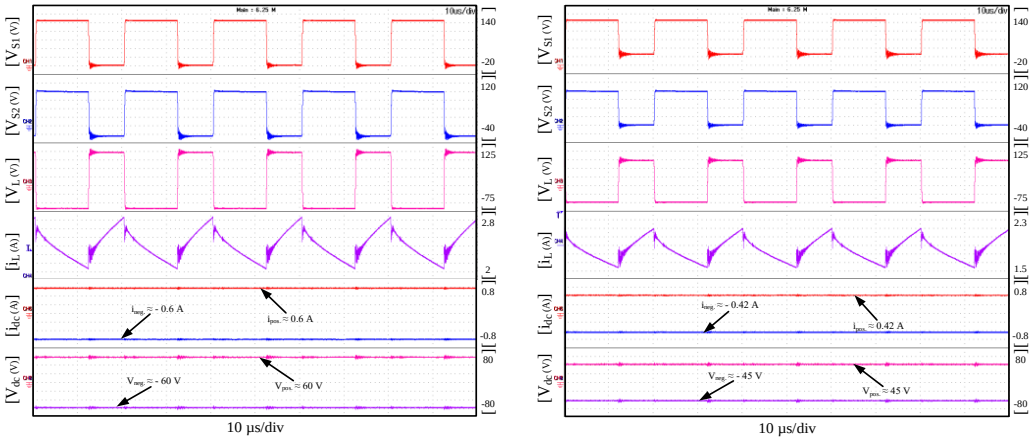
experimental results are congruent with the expected characteristics shown in Fig. 7.

C. Experimental Verification of Independent Power Flow and Mode Transition.

The experimental verification of arbitrary independent power flow from both sources was performed for MBDC type D and the results are presented in Fig. 14. In Fig. 14 (a), only the first input source, V_1, is supplying energy to the bipolar dc link thus d_1=40% and d_2=0, such that D_{1eff} =0.4 and D_{2eff} = 0. V_1=100 V, V_2=75 V and the load at the poles of the bipolar dc bus was set to 100 Ω. Under these conditions, the bipolar output voltages and currents are about ±60 V and ±0.6 A, respectively, while i_L and Δi_L are about 2.4 A and 0.6 A, respectively.

Similarly, in Fig. 14 (b) only the V_2, is supplying energy to the bipolar dc link, thus d_1=0 and d_2=40% such that D_{1eff} =0 and D_{2eff} =0.4, and the loads were also set to 100 Ω. The input sources and output loads are the same as earlier when only V_1 is supplying (V_1=100 V, V_2=75 V and 100 Ω). In these conditions, the bipolar output voltages and currents are about ±45 V and ±0.42 A, while i_L and Δi_L are about 1.8 A and 0.55 A, respectively. This proves the performance of the MBDCs under arbitrary independent power flow.

Further, MBDC type D was verified for transition between the independent and simultaneous power flow from both sources during operation with results presented in Fig. 15. In Fig. 15 (a), V_1=100 V and V_2=75 V, and for the first 3 seconds, only V_1 is supplying the dc link with d_1=20% and d_2=0, during which the



(a) (b)

Fig. 14. Experimental verification of independent power flow from the input sources for (a) V_1 only supplying when V_1=100V, V_2=75V, d_1=40% and d_2=0, and (b) V_2 only supplying when V_1=100V, V_2=75V, d_1=0 and d_2=40%.

output voltages and currents are about ±20 V and ±0.2 A, respectively. During the next 5 seconds, both V_1 and V_2 are supplying the dc link with d_1=20% and d_2=40%. Therefore, the output voltages and currents increased to about ±55 V and ±0.5 A, respectively. Finally, in the last few seconds, only V_2 is supplying the dc link with d_1=0 and d_2=40%, thus the voltages and currents at the output decrease to about ±45 V and ±0.4 A, respectively. Similar tests are performed when the input voltages are equal i.e., V_1=V_2=75 V, being presented in Fig. 15 (b). Under this condition, the voltages and currents at the output are about ±45 V and ±0.4 A, respectively. These results demonstrate a roughly seamless transition between independent and simultaneous modes of power transfer from the input ports to the bipolar dc link.

D. Verification of Operation with Unbalanced Load

To validate the self-balancing characteristics of the proposed MBDCs, MBDC type D was operated with different loading conditions of the positive and negative poles. The simulation and experimental results are presented in Fig. 16. For both cases V_1 = 100 V, V_2 = 75 V, d_1 = 20%, d_2 = 40% and the duty of 50% was applied to S_{b1} and S_{b2}, alternately. It was observed that although the load is increased on one pole, the output voltages remain balanced, being the key feature of the proposed MBDCs. The bipolar dc bus voltage balancing does not require a closed loop control to keep the output voltage balanced on both poles under these

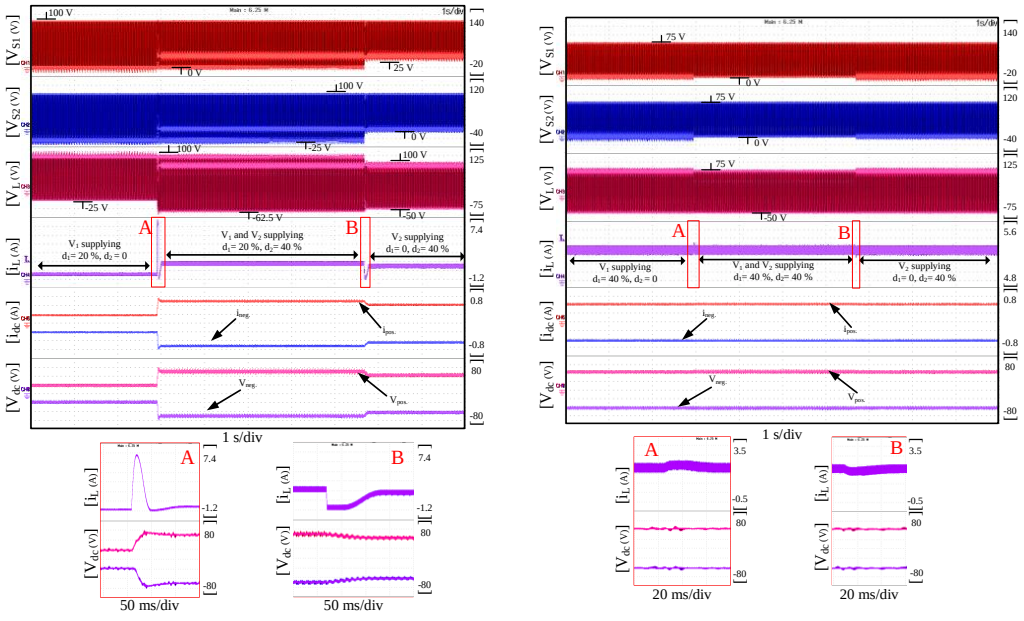
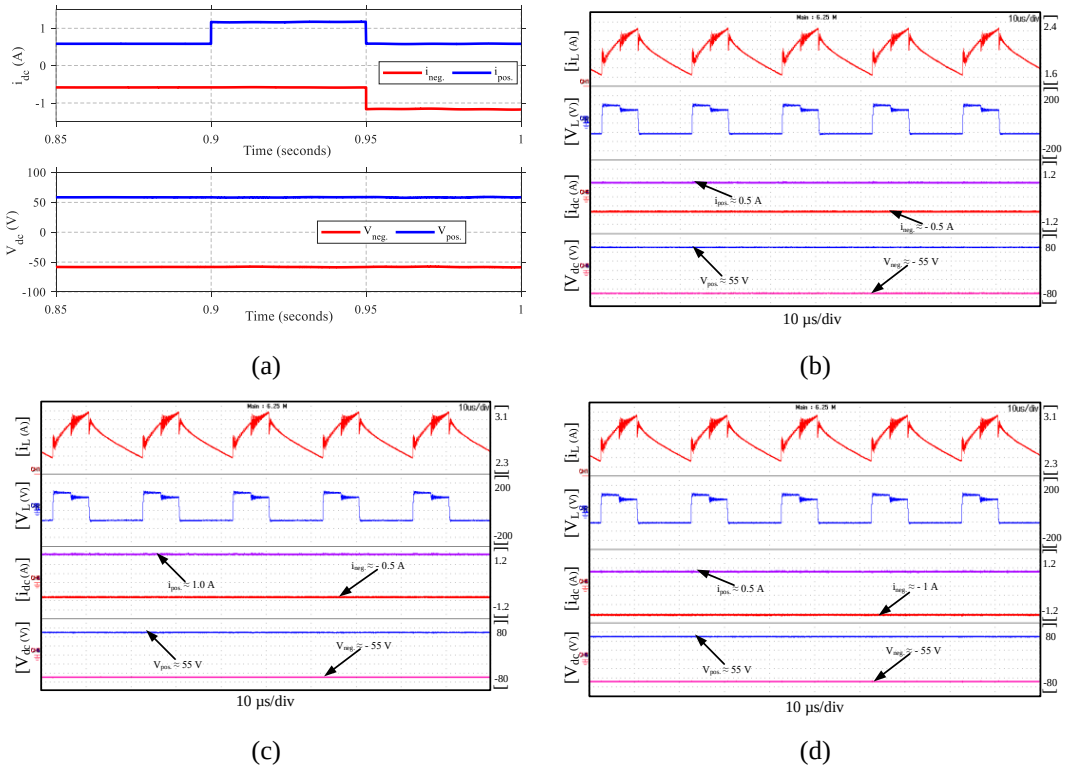


Fig. 15. Experimental verification of operating mode transition for (a) V_1=100V, V_2=75V, and (b) V_1=V_2=75V.

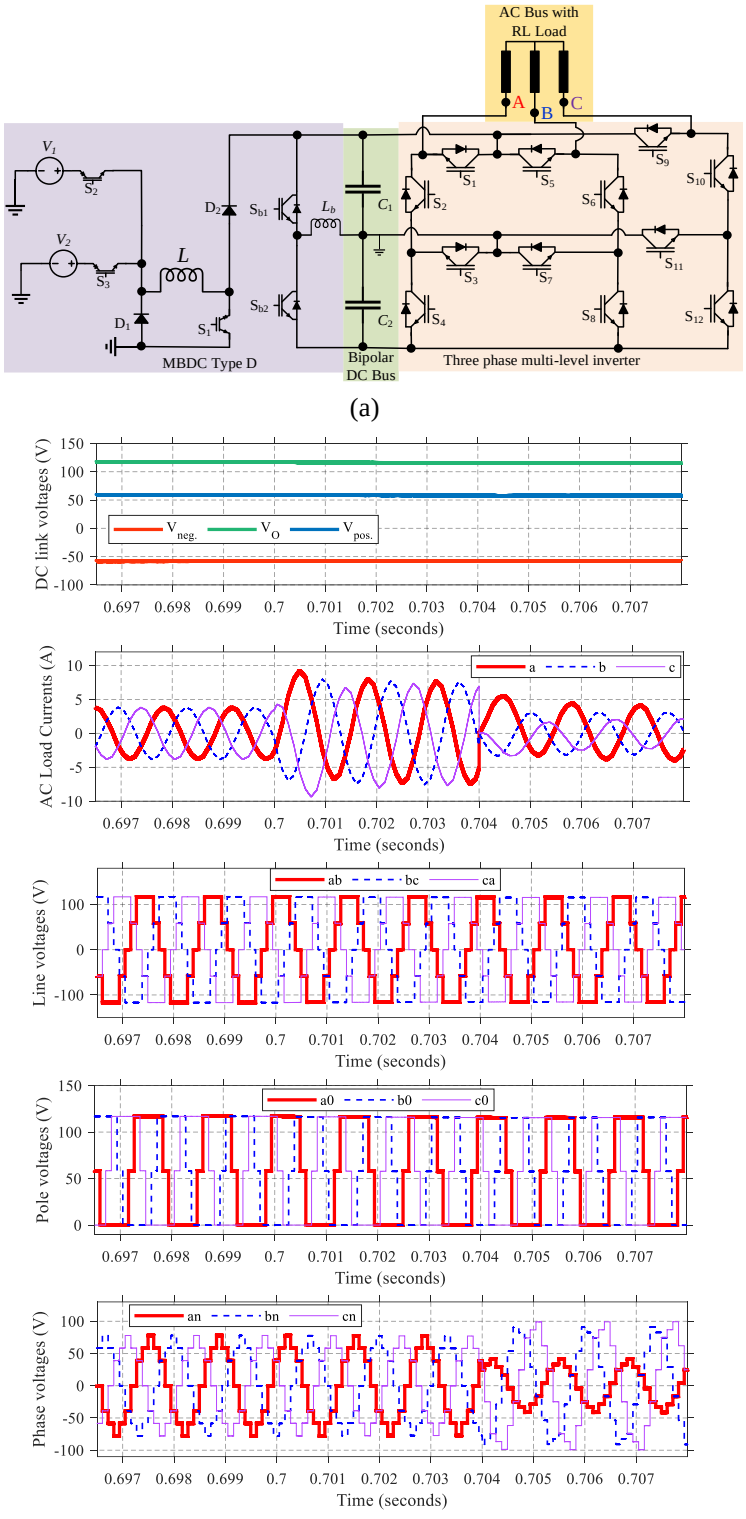
disturbances. To further test this feature, MBDC type D was integrated with the multilevel inverter proposed in [37] as shown in Fig. 17 (a). The inputs to the MLI were replaced by the bipolar outputs of the MBDC to create a multi-input multi-level inverter. The MLI switches were operated with low frequency modulation as discussed in [37] with three phase *RL* loads connected in wye configuration at the outputs of the inverter. The simulation results of this implementation are presented in Fig. 17 (b), showing the currents through the three phases to the loads and the voltages of the bipolar dc link, ac line, ac phase and the poles of the MLI. Although the currents through the phases are varied, the dc link voltage remains constant at about 115 V and ±57 V. The line and pole voltages also remain constant throughout the duration of the disturbance. As expected for wye connected loads, when the currents in all three phases are unbalanced, the phase voltages are disturbed. Further, the total harmonic distortion (THD) of the phase and line voltages were all about 16.83%, while the currents had a THD of about 1.67% all through the different conditions before adding filters. Thus, the applicability of the proposed MBDCs for MLIs and other applications that could potentially cause unbalanced loads at the poles of the dc bus is validated. The voltage balance is achieved



(a) (b) (c) (d)

Fig. 16. Verification results for operating MBDC type D under unbalanced loads when V_1=100V, V_2=75V, d_1=20% and d_2=40% for (a) simulation result, (b) experimental result when $R_{pos.}$=$R_{neg.}$=100Ω, (c) experimental result when $R_{pos.}$=50Ω, $R_{neg.}$=100Ω and (d) experimental result when $R_{pos.}$= 100Ω, $R_{neg.}$=50Ω.

without requiring closed loop control, or only 50% duty applied alternately to S_{b1} and S_{b2} was sufficient to keep the output voltages balanced. Furthermore, the closed loop performance of the proposed MBDCs were examined with results for



(a)

(b)

Fig. 17. Integrating MBDC type D with the multilevel inverter proposed in [37], with (a) integration schematic and (b) simulation results showing the bipolar DC link voltages and the ac stage voltages and current under different load conditions.

MBDC type A presented in Fig. 18. Under various changes, in the load currents, input and output voltages, a set of heuristically selected PI gains for the double loop PI controller is sufficient to achieve desirable characteristics. The rise time is less than 15 ms, settling time is less than 30 ms and overshoot is less than 2 V at converter start-up. Under all the different perturbations, the controller can track the

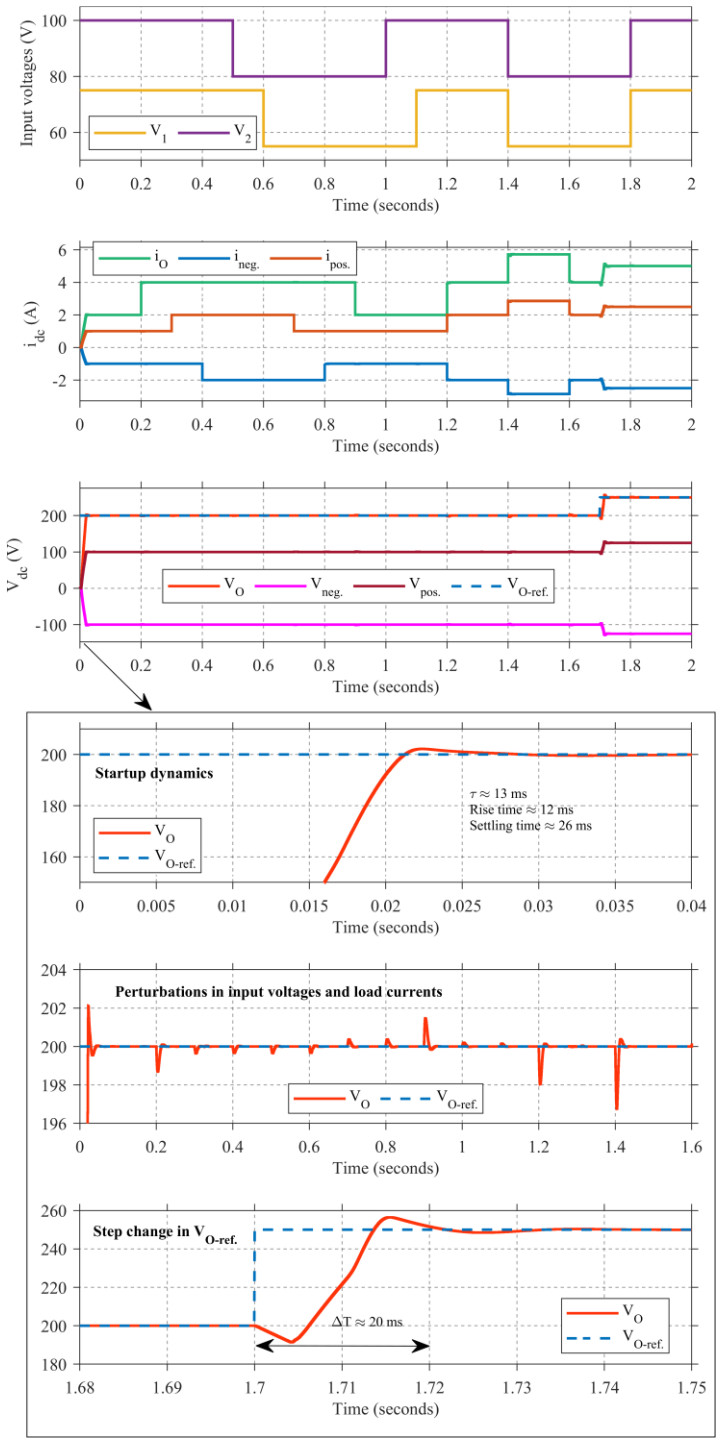


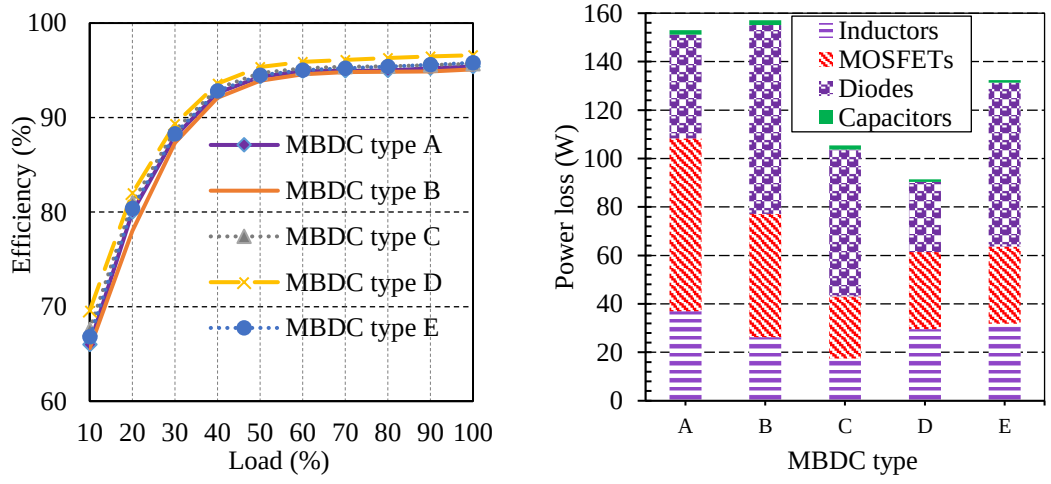
Fig. 18. Closed loop performance of MBDC type A under perturbations in the input voltages, load currents and output reference voltage.

reference voltage with very minimal perturbations on the output voltage. This result further proves the ability of the GVD based MBDCs to keep the voltages at the respective poles balanced under unbalanced loads, without the need for a dedicated controller.

E. Power Loss Analysis

The power losses (P_L) in the proposed family of MBDCs can be estimated using (23), consisting of the inductor winding (P_{indW}) and core (P_{indC}) losses, capacitor losses (P_{cap}), MOSFET switching and conduction losses, where T_S is the switching period, R_{ESRL} is the inductor's equivalent series resistance (ESR), $\hat{i}_L$ is the inductor average current, Δi_L is the inductor ripple current, $K, \beta \,\&\, \alpha$ are Steinmetz parameters, R_{ESRC} is the capacitor ESR, V_{DS} is the MOSFET drain to source voltage, i_{DS} is the MOSFET drain to source current, t_{on} & t_{off} is the MOSFET ON and OFF time, R_{DSon} is the MOSFET on state resistance, D is the respective duty cycle, i_d is the current through the diode and V_f is its forward voltage.

Based on (23), the efficiency at different loading conditions and loss distribution in the components of the proposed family of MBDCs was computed and presented in Fig. 19, respectively. This loss distribution was computed at 2 kW load with the positive and negative poles (±V_O/2) having 600 W each, and the full dc link (V_O) was 800 W. Both input sources were equal at 100 V, and V_O of the converter was regulated to 200 V. MBDC types A and B exhibit the most losses under these conditions due to the losses in the diodes. MBDC type C shows remarkably lower



(a) (b)

Fig. 19. Efficiency analysis (a) at different loading conditions and (b) loss distribution at 2 kW load with V_O = 200 V and V_1 = V_2 = 100 V.

losses since it requires fewer active switches and diodes than MBDC types A and B, respectively. However, due to the ultra-high gain of MBDC type C, high currents flow through the switches and the voltage stress on its active switches are high. MBDC type E also experiences more than 100 W of losses due to the diodes in the switched inductors. Comparatively, MBDC types D and E have lower losses than MBDC types A and B, respectively, showing that the use of the SBC based bipolar outputs have lower losses than the use of the GVDs.

$$P_L \approx \left\{ \begin{array}{l} \underbrace{\frac{1}{T_S}\int_0^{T_S} R_{ESRL}\left(i_L{}^2 + \frac{\Delta i_L{}^2}{12}\right)}_{P_{indW}} + \underbrace{K\Delta i_L^{\beta} F_{SW}^{\alpha}}_{P_{indC}} + \underbrace{R_{ESRC}\left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}_{P_{cap}} \\ + \underbrace{\frac{1}{2}V_{DS} i_{DS} F_{SW}\left(t_{on}+t_{off}\right)}_{P_{SWMOS}} + \underbrace{R_{DSon} i_{DS}^2 D}_{P_{onMOS}} + \underbrace{i_d V_f D}_{P_{onD}} \end{array} \right\} \quad (23)$$

IV. COMPARISON WITH RELATED NON-ISOLATED MBDCS

Table II presents the comparison of the proposed family of MBDCs with the recently proposed non-isolated MBDCs in [33, 34]. The basis for selecting these MBDCs for comparison is that, to our knowledge, they are the only existing non-

TABLE II
COMPARISON OF THE PROPOSED FAMILY OF MBDCS WITH EXISTING NON-ISOLATED MBDCS.

Parameters		[33]	[34]	Proposed MBDC types				
				A	D	B	E	C
Part Count	S	2	3	N+1	N+3	N+1	N+3	N
	D	4	4	5	2	8	5	7
	L	1	3	1	2	2	3	2
	C	3	6	4	2	4	2	4
	T	10	16	N+11	N+9	N+15	N+13	N+13
No. of inputs		2	2			N		
IPF		*Partially	*Partially	Yes	Yes	Yes	Yes	Yes
PFP		No	+Partially	No	No	No	No	No
SPF		Yes, boost	Yes, boost	Yes, buck-boost		Yes, boost	Yes, boost	Yes, boost
Modulable		No	No	Yes	Yes	Yes	Yes	Yes
Output voltage-balancing		Complex closed loop	Inherently symmetrical	Inherently symmetrical	Open loop control	Inherently symmetrical	Open loop control	Inherently symmetrical
V_{TR}		1/(0.5+0.5α)	1/α	2/α	2/α	4/α	2/α	8/α
Rated power (W)		200	100			2000		
Sw. frequency (kHz)		30	100			50		
Efficiency (%)		≈93	≈93.5			≈95		

N=Number of inputs, IPF=Independent power flow, PFP=PF between ports, SPF=Simultaneous PF, S=Active switch, D=Diode, L=Inductor, C=Capacitor, T=Total, *=IPF is only possible from the second input port, +=PFP is only possible from the first to the second input port and not vice versa, Sw.= Switching.

isolated MBDCs in literature. Table II is arranged in the order of increasing voltage gain (expressed as V_{TR}) when the MBDCs are operating in under simultaneous power flow from more than one input to the bipolar dc link. All the proposed MBDCs have higher V_{TR} than the counterparts with the proposed MBDC type C having the highest V_{TR}. MBDC types A and D, having the lowest V_{TR} in the proposed families, are two times higher than the V_{TR} obtainable in [34], with [33] offering the overall lowest V_{TR}. The bipolar output voltages proposed in MBDC types A to C as well as [34] are inherently symmetrical, and thus do not need a control system keep the voltages balanced, while a complex closed loop system is required in [33], a simple open loop control of 50% duty cycle in required MBDC types D and E. Further, the modularity of the converters should be taken into comparison, since this proves the possibility of expanding the number of input ports without modifying the structure of the MBDCs. All the proposed MBDC types are modular, and thus their number of inputs can be increased arbitrarily, but both MBDCs in [33, 34], have the maximum number of two inputs. Finally, the independent power flow (IPF) can be carried out arbitrarily from any of the inputs of the proposed MBDCs to the outputs, but the existing MBDCs can achieve IPF in the second input alone. Although the MBDC in [33] has the lowest total component count, it also features the lowest V_{TR}, while the proposed MBDCs have competitive number of components with the significantly high V_{TR}.

V. CONCLUSION

A family of five novel non-isolated multiport dc-dc converters with bipolar symmetric outputs (MBDC types A to E) was proposed in this paper for integrating multiple renewable energy sources to bipolar dc grids. The proposed converters have key merits of high voltage gain or voltage transformation factor, and naturally symmetrical bipolar outputs or requiring a simple open-loop PWM control of 50% duty cycle to keep the output voltages balanced. Further, the number of input ports can be arbitrarily increased to accommodate more renewable energy resources by adding only the respective active switch for the source being introduced. The detailed analysis and performance of the proposed family of MBDCs were numerically verified in simulation and validated experimentally on a hardware test setup based on SiC switches under various conditions. It was demonstrated that the proposed MBDCs have attractive features of high gain, modularity, arbitrary number of ports naturally symmetric outputs, and simple balance control for the asymmetrical members as compared to the counterparts.

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Paper V:

Integrated Multiport DC-DC and Multilevel Converters for Energy Sources

This paper has been published as:

I. N. Jiya, A. Salem and H. Van Khang, "Integrated Multiport DC-DC and Multilevel Converters for Energy Sources," *2022 IEEE Industry Applications Society Annual Meeting (IAS)*, Detroit, Michigan, 2022, pp. 1-7, doi: 10.1109/IAS54023.2022.9939764.

Integrated Multiport DC-DC and Multilevel Converters for Energy Sources

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***Abstract*—This paper presents a novel converter system for integrating multiple renewable energy sources for both dc and ac grids. The proposed converter system is formed by integrating a novel multiport dc converter topology with a multilevel inverter topology, aiming to achieve multiple source integration with low component count and higher efficiency on the multiport converter section and efficient dc to ac conversion on the multilevel inverter section. As compared to counterparts in literature, where each energy source requires its own dc converter and the dc to ac conversion is achieved using a two-level converter, the converter system proposed in this paper has more attractive features of buck-boost operation, better power quality characteristics and low part counts. Within the framework, an auxiliary circuit-based dc link voltage balancing technique is proposed to balance the voltage on the dc link as compared to the more complex control-based balancing scheme. Open and closed loop operations of the converter system are numerically verified using simulations and validated by a high-fidelity hardware-in-the-loop implementation platform.**

Keywords—dc-dc converter, dc link capacitor balancing, multiport converter, multilevel inverter

I. INTRODUCTION

Over the past few years, the imminent depletion of fossil fuels and the adverse environmental effects of their usage to satisfy the increasing energy demands have championed the search for green alternatives [1]. Fuel cells, wind and photovoltaic (PV) systems have been proved to be suitable alternatives to provide the much needed green solutions [2, 3]. The increased penetration of these renewable energy sources (RESs) has led to a paradigm shift in the electrical energy generation and utilization from centralised to distributed generation systems [4]. Distributed generation systems are hence the back-bone of future power systems, which are majorly based on dc microgrids, since they have no issues with reactive power and

synchronisation among many other advantages as compared to the ac microgrids [5, 6]. However, in many conventional power systems, especially in developing economies, there is a high prevalence of ac power systems [7]. Thus, the need to still convert the power generated from RESs from dc to ac cannot be overemphasized.

Multilevel inverters (MLIs) have become one of the most attractive solutions for converting dc to ac at high power levels [8] due to their appealing features such as: low switching losses, small/zero common-mode voltage (CMV), low total harmonic distortion (THD), lower electromagnetic interference, smaller filter component sizes and lower cooling requirements to name just a few [9]. Having all these merits over the traditional two-level inverter has been the motivation for the development of new MLI topologies. Although a lot of work has been and is still being done in proposing novel topologies of MLIs [10–12], one aspect that has received significantly less attention is the conditioning of the input sources to accommodate the integration of RESs. Most existing topologies assume the inputs to be constant dc sources. his is ideal but is impractical in applications because most RESs vary in output voltage during operation [13].

To address this issue, some attempts have been made to propose MLIs, which have a provision to preprocess the outputs of RESs prior to the ac conversion stage [14–18]. In the MLI topologies proposed in [14–17], the preprocessing of the power from the RESs is integrated into the MLI topology in a manner that provides boosting features to the ac output. However, these topologies have two limitations. Firstly, the number of RESs, that can be integrated into the ac grid, is restricted to only one and secondly, they are only capable of boosting the input voltages. To address this, the MLI proposed in [18] integrates two RESs using two cascaded dc-dc converters prior to the MLI stage, which allows for buck-boost operation and multiple inputs. However, with this structure, each RESs requires its own dc converter, leading to high component count, high power losses, higher system cost, lower power density and efficiency. Further, with the introduction of multiple RESs, there is the issue of dc link capacitor voltage balancing. MLIs used for multiple RESs require three dc link capacitors connected in series to equally split the dc link voltage across them [13]. Therefore, there is need to adequately balance the voltage across them to avoid distortions in the output waveforms and preserve the power quality. This usually requires a complex control system to achieve equally balanced dc link voltage across the three capacitors [19].

In this research, a new structure of RES integration is proposed to address the aforesaid problems. A multiport dc converter (MDC) is used to integrate the RESs, thus lower part count is achieved in the preprocessing stage. This leads to lower cost, lower losses, higher efficiency, and power density. Further, an auxiliary circuit is proposed to achieve a less complex dc link capacitor voltage balancing as compared to the control-based balancing technique previously proposed. The proposed configuration is also capable of buck-boost operation, individual and simultaneous power transfer from multiple RESs. The performance and operation of the converter system is numerically verified and validated using a high-fidelity hardware-in-the-loop (HIL) device.

II. PROPOSED INTEGRATED CONVERTERS

Fig. 1 presents the proposed integrated multiport dc and multilevel converter, consisting of a novel multiport dc-dc converter section highlighted in blue, the dc bus output highlighted in purple and the multilevel inverter (previously proposed in [13]) section alongside the ac output highlighted in green. This configuration allows for easy integration of different energy sources with varying voltage levels to dc and ac links independently or simultaneously.

A. Multiport dc converter Topology

The blue shaded region of Fig. 1 presents the proposed unidirectional multiport dc to dc converter (MDC) topology. The dc converter section consists of one inductor, two diodes and N+1 number of reverse blocking transistors, where N is the number of input ports to the multiport converter. Since there are few reverse blocking FETs on the market to realize the reverse blocking transistor, a diode can be connected in series to a regular FET instead. The main selling points of the proposed MDC

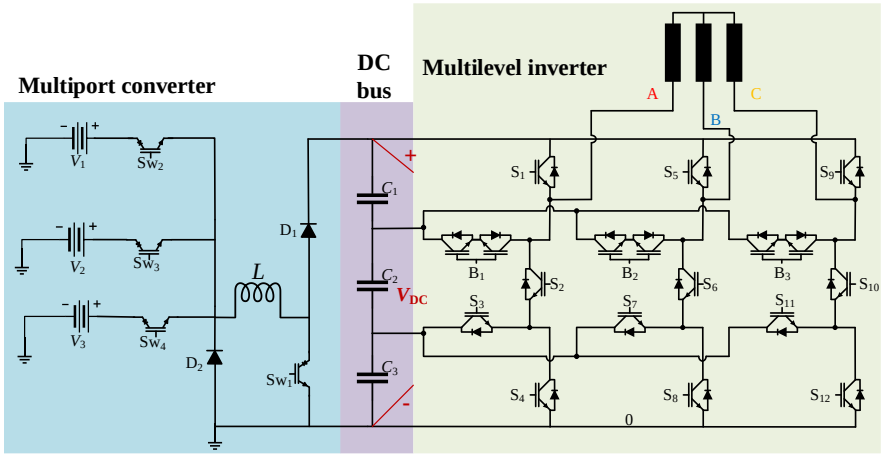


Fig. 1. Schematic of the integrated multiport converters system.

is that contrary to conventional MDCs, which require *N* inductors for *N* input sources, the proposed MDC utilizes only one inductor for any number of input sources, thus the power density is potentially higher in the proposed MDC. Furthermore, only one additional reverse blocking FET is needed when introducing an additional input port.

The MDC can operate in up to seven different unidirectional modes of which four are simultaneous power flow from two or more sources (V_1 & V_2, V_2 & V_3, V_1 & V_3, V_1, V_2 & V_3 respectively). The other three modes represent independent power flow from the three sources (V_1 – V_3) to the dc link. The independent power flow from the sources when examined closely, is very similar to the standard non-inverting buck-boost converter. In this mode, the switching period T_s is divided into two, T_1 and T_2, for the inductor charging and discharging periods, respectively. In the independent power flow mode, this converter can operate in the buck or boost modes depending on the duty ratio '*D*' applied across the switches. Where *D* is the ratio of the inductor charging time to the total switching period, that is $D = T_1/T_S$. Therefore, the conventional equations (1 – 3) describing the relationship between the input and output voltage of the basic buck-boost converter applies to this converter as well for independent power flow from the respective inputs to the output, V_{DC}.

$$V_{DC} = \frac{T_1}{T_2} V_1 = \frac{D}{1-D} V_1 \tag{1}$$

$$V_{DC} = \frac{T_1}{T_2} V_2 = \frac{D}{1-D} V_2 \tag{2}$$

$$V_{DC} = \frac{T_1}{T_2} V_3 = \frac{D}{1-D} V_3 \tag{3}$$

In the simultaneous power transfer mode, as mentioned earlier, two or more sources are required to supply the required energy concurrently. In this study, the

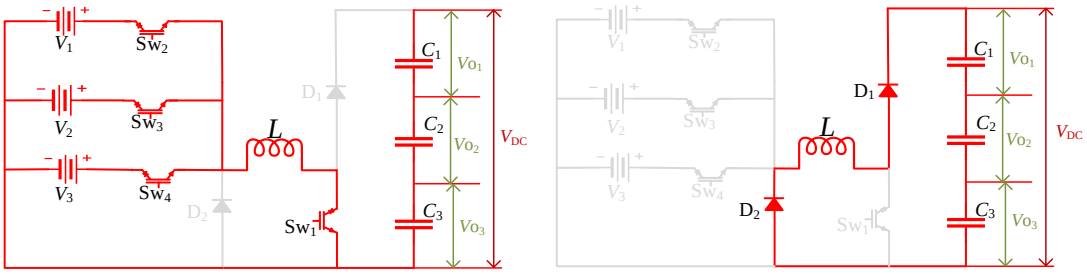


Fig. 2. Path of current flow of the MDC in steady state CCM under simultaneous power transfer for inductor charging and discharging.

MDC is analysed for three inputs, with the conduction modes during the switching states and steady state waveforms are presented in Figs. 2 and 3 respectively. Within this mode, the inductor charging period, T_1 is further subdivided into two or more, depending on the number of simultaneous input sources. During time T_1, switches S_{W2}, S_{W3}, S_{W4} and S_{W1} are all switched ON. However, in the first subdivision of T_1, the voltage across the inductor is the highest source voltage V_1, therefore the inductor charges with a gradient of V_1/L. When the first subdivision period of T_1 is over, S_{W2} is turned OFF while S_{W3}, S_{W4} and S_{W1} remain ON. In the second subdivision of T_1, the voltage across the inductor becomes V_2 while the inductor continues to charge with a gradient of V_2/L. In the third subdivision of T_1, only S_{W4} and S_{W1} remain ON and the voltage across the inductor becomes V_3 while the inductor continues to charge with a gradient of V_3/L. This process will continue for an MDC with more than three inputs in the decreasing order of the magnitude in their input voltages. When the inductor charging period is over, all the active switches (S_{W1} – S_{W4}) of the MDC are OFF, being immediately followed by the discharging period T_2. During T_2, the inductor, L, discharges through the capacitor, C, to the dc bus through D_1 and D_2, so the voltage across the inductor becomes

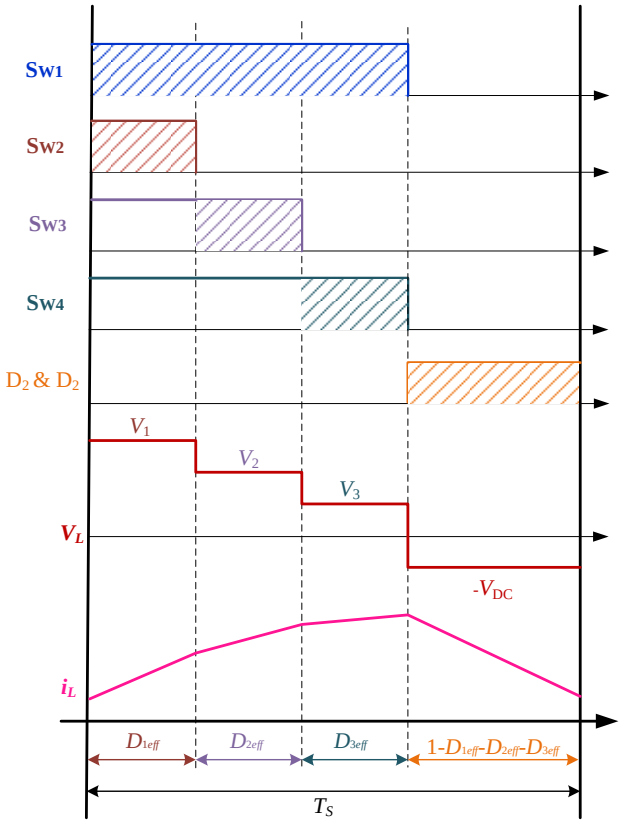


Fig. 3. Steady state CCM waveforms of the MDC under simultaneous power transfer from the three sources to the dc link.

$-V_o$, while the inductor discharges with a slope of $^{-V_o/L}$. The effective voltage across the inductor from each source is given by the product of the effective ON time of that source and its voltage magnitude. As shown in Fig. 3, this effective voltage is $D_{1eff}V_1$ for the first subdivision of the inductor charging time, $D_{2eff}V_2$ for the second subdivision and $D_{3eff}V_3$ for the third subdivision.

For an effective commutation of the switches in under simultaneous power transfer mode, some rules are required to achieve simultaneous power transfer to the load. When the voltages are unequal, if the sources are arbitrarily arranged in order of increasing magnitudes such that $V_1 > V_2 > \cdots > V_N$ for *N* input ports, then the duty cycles of the switches controlling the input sources, i.e S_{W2}, S_{W3} and S_{W4}, must be in such a way that $D_1 < D_2 < \cdots < D_N$, and vice versa. Where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, … , $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. However, if the source magnitudes are equal or $V_1 = V_2 = \cdots = V_N$ for *N* input ports, the duty cycles of the PWM signals must be in such a way that $D_1 = D_2 = \cdots = D_N$ to achieve equal power delivery from the sources. However, if the required power delivery from the sources is unequal, D_1, D_2, …, D_N can be determined in order of increasing magnitude from the respective sources. Furthermore, by applying the volt-second balance to the steady state waveform in Fig. 4, the relationship between the input sources and the output voltage is given by (4) and (5) for *N* number of input sources and the three-input configuration respectively. But if the magnitudes of the input sources are equal and the duty cycles are equal, the relationship between the input and output voltage is given by (6). However, if the voltage of sources is equal but the duty cycles unequal, the relationship between input and output voltage is given by (7), where: $V_{in} = V_1 = V_2$ $D_{max} = max.(D_1, D_2)$.

$$V_O = \frac{\sum_{i=1}^{N}\left(D_{(i)eff}V_i\right)}{1-\sum_{i=1}^{N}D_{(i)eff}} \tag{4}$$

$$V_O = \frac{D_{1eff}V_1 + D_{2eff}V_2 + D_{3eff}V_3}{1-D_{1eff}-D_{2eff}-D_{3eff}} \tag{5}$$

$$V_O = \frac{T_1}{T_2}V_{in} = \frac{D}{1-D}V_{in} \tag{6}$$

$$V_o = \frac{D_{\max}}{1-D_{\max}}V_{in} \tag{7}$$

B. Multilevel Inverter Topology

In Fig. 1, the MLI topology is highlighted in green, consisting of twelve unidirectional switches (S_1-S_{12}) and three bidirectional switches (B_1-B_3). To simplify the gate-drive circuits, the common-emitter structure is adopted to configure the bidirectional switches. The dc-link of the MLI topology is configured using three dc-link capacitors. The inverter switches are controlled to produce four unipolar voltage levels of 0, $E/3$, $2E/3$, and E in the pole voltages V_{A0}, V_{B0}, and V_{C0}. Seven-level bipolar voltages can be generated in the line voltages V_{AB}, V_{BC}, and V_{CA} by subtracting the adjacent pole voltages. For example, V_{AB} is synthesized by subtracting V_{B0} from V_{A0}, producing a seven-level voltage of $-E$, $-2E/3$, $-E/3$, 0, $E/3$, $2E/3$, and E. The operating modes and modulation strategies of the MLI topology is sufficiently addressed in [13].

C. Capacitor Voltage Balancing

The capacitor voltage imbalance is common in four-level inverter topologies, where three capacitors are connected in series to divide the dc-link voltage into three equal parts as shown in Fig. 1. A generalized mechanism for investigating the capacitor voltage imbalance in the four-level topologies was provided in [19]. The three capacitor currents I_{C1}, I_{C2}, and I_{C3} in the dc link of the proposed configuration are not equal, causing a voltage imbalance. The current of the middle capacitor I_{C2} is larger than the currents of other capacitors I_{C1}, and I_{C3}, which are equal. Consequently, the C_1 and C_3 discharge less energy than C_2. Specifically, C_2 discharges faster to zero while the full dc-link voltage V_{dc} is equally shared between C_1 and C_3. Since the capacitor voltages are not balanced because of the over-discharge of C_2. Therefore, by regulating the voltage of C_2, the other capacitors C_1 and C_3 can be balanced. Subsequently, the three capacitor voltages V_{C1}, V_{C2}, and V_{C3}, are equal when V_{C2} is regulated at $V_{dc}/3$. To this end, a control

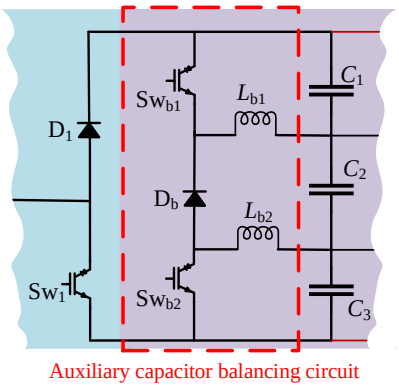


Fig. 4. Schematic of the auxiliary circuit for capacitor balancing.

based voltage balance scheme is used in [13], referred to as the variable-carrier scheme (VCS). The VCS method consists of the modulation signal generation block, carrier signal block, and a PI controller. These three parts are used to generate modulation signals with a third-harmonic injection variable and fixed carrier signals, which are used to regulate C_2 voltage to $V_{dc}/3$.

However, a simpler solution is proposed here with the use of an auxiliary capacitor balancing circuitry to keep the voltage of the three capacitors balanced as shown in Fig. 4. The circuit based balancing technique consist of using two inductors (L_{b1}, L_{b2}) and three switches (one diode, D_b and two MOSFETs, S_{Wb1}, S_{Wb2}). S_{Wb1} and S_{Wb2} are controlled using the same pulse signal, when they are turned ON, the two inductors charged and then discharged through D_b. By this action, the voltage of C_2 is prevented from degrading to 0. A proportional controller selected heuristically and used to determine the duty cycle of S_{Wb1} and S_{Wb2} so that the voltage of C_2 is regulated to $V_{dc}/3$ while both C_1 and C_3 are naturally balanced at $V_{dc}/3$ too under these conditions.

III. RESULTS

The proposed isolated MIC is numerically verified in simulations and validated through hardware-in-the-loop (HIL) implementation using OPAL-RT's OP5700 device running a 64-bit virtex-7 FPGA. Fig. 5 shows the laboratory setup used for the validation and the values of the different component's parameters are presented on Table I. The verification was done in open and closed loop both in simulation and real-time HIL implementation, the results are presented here.

Fig. 6 presents the open loop simulation results of operating the MDC when the input voltages are V_1 = 300 V, V_2 = 250 V, and V_3 = 200 V. The respective duty applied to the switches S_{W2} to S_{W4} are D_1 = 20%, D_2 = 40% and D_3 = 60% (D_{SW2} to D_{SW4}) such that the effective duties, D_{1eff} = D_{2eff} = D_{3eff} =0.2. Under these conditions, the voltage stress of the switches (V_{SW2} to V_{SW4}), inductor (V_L) and the current stress of the switches (i_{SW2} to i_{SW4}), which are also the input currents from the sources (i_{V1} to i_{V3}), are presented, alongside the voltage of the dc link and the three capacitors, V_{DC}, and V_{C1} to V_{C3}, respectively. The dc link voltage is about 372 V and split into three equal parts of 124 V across each of the three dc link capacitors. This is further verified by the HIL implementation result presented in Fig. 7, which are congruent with the results obtained from the analytical simulation. Furthermore, the MLI stage is operated under level-shifted pulse width modulation (LS-PWM) scheme as described in detailed in [13]. The simulation

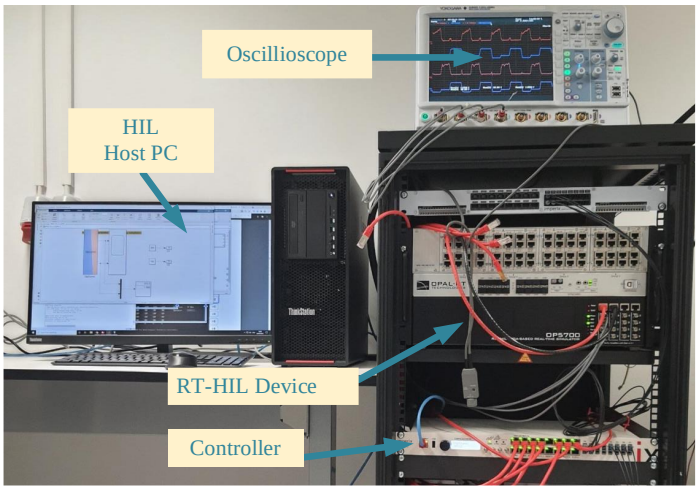


Fig. 5. HIL platform used for validating the integrated converter system.

TABLE I
PARAMETERS USED IN SYSTEM VERIFICATION

Parameter	Value	Unit
Inductor (L)	4	mH
Inductor (L_{b1}=L_{b2})	0.1	mH
Output capacitor (C_1=C_2=C_3)	9.4	mF
Voltage sources (V_1/V_2/V_3)	300/250/200	V
AC load (R – L)	8.1 / 12.5	Ω / mH

and HIL results of the MLI stage is presented in Figs. 8 and 9, respectively. The MLI stage was operated to achieve 50 Hz seven-level output voltages, (V_{ab} and V_{an}) and current (i_a) and the pole voltages (V_{a0}, V_{b0} and V_{c0}) at its' output. Again, the results of the MLI's simulation and HIL implementation are consistent.

To verify the balancing of the voltage across the dc link capacitors, the control-based voltage balancing technique and circuit-based voltage balancing were implemented in both simulation and the HIL platform. The results for both techniques are in Figs. 10 and 11, respectively. The PI parameters of the controller for the control-based balancing technique were heuristically selected as presented in [13]. From Fig. 10 (a), the controller can achieve steady state with the voltage across C_2, V_{C2}, being controlled to about 124.8 V while C_1 and C_3 try to balance out the remaining 247 V naturally, with obvious oscillations in simulation. Similarly in the HIL implementation result, Fig. 10 (b), of control-based voltage balancing, V_{C2}, is controlled to about 121 V while C_1 and C_3 try to balance out the remaining 251 V naturally, also with obvious oscillations. In the circuit-based capacitor balancing technique, a simple proportional controller is heuristically selected to control the active switches (Sw_{b1} and Sw_{b2}) of the auxiliary capacitor

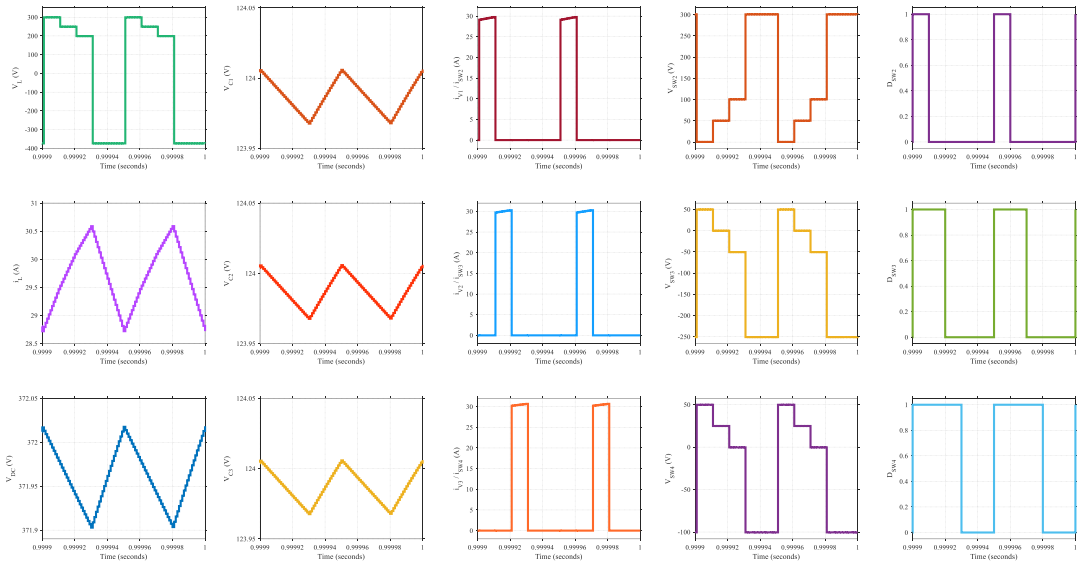


Fig. 6. Open loop simulation results showing key waveforms of the MDC operation when D_1 = 20%, D_2 = 40% and D_3 = 60%.

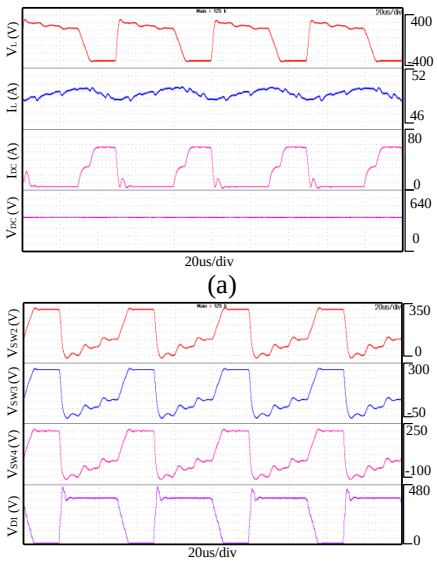


Fig. 7. Open loop HIL implementation results showing key waveforms of the MDC operation when D_1 = 20%, D_2 = 40% and D_3 = 60%.

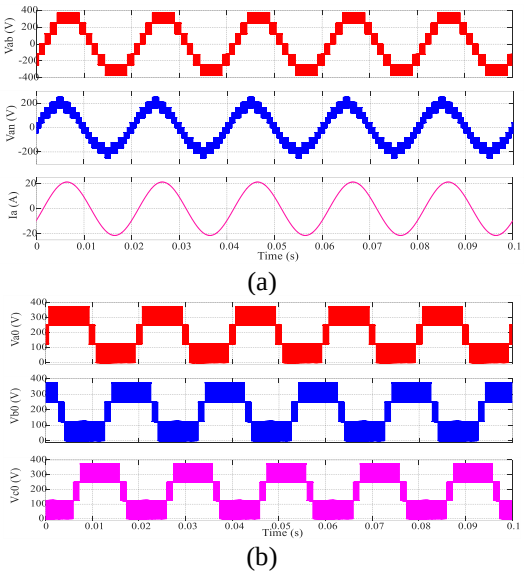
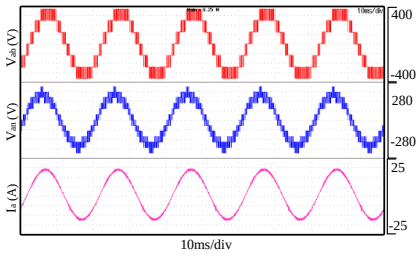
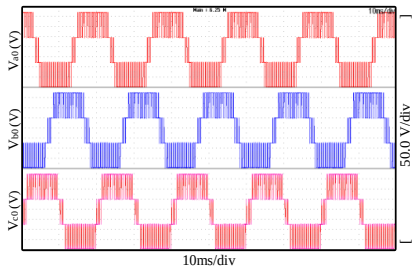


Fig. 8. Simulation results of the MLI when the MDC duty is D_1=20%, D_2=40% and D_3=60% showing (a) output current and voltage waveforms and (b) the pole voltages.

balancing circuit which have the same duty cycle. The simulation result in Fig. 11 (a) show how effectively the auxiliary circuit-based technique achieves capacitor voltage balancing with better accuracy than the control-based technique in Fig. 10 (a). V_{C2} is controlled to about 124.1 V while the remaining 248 V is balanced equally between C_1 and C_3, with oscillations as seen previously in Fig. 10. Further, in Fig. 11 (b), the HIL implementation result shows similar consistency with its simulation result in Fig. 11 (a), V_{C2} is controlled to about 121 V while the remaining 251 V is balanced equally between C_1 and C_3, also with some

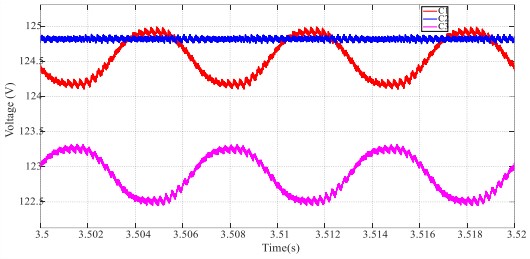


(a)

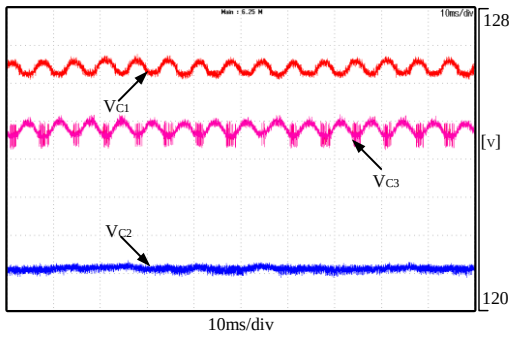


(b)

Fig. 9. HIL implementation results of the MLI when the MDC duty is D_1=20%, D_2=40% and D_3=60% showing (a) output current and voltage waveforms and (b) the pole voltages.



(a)

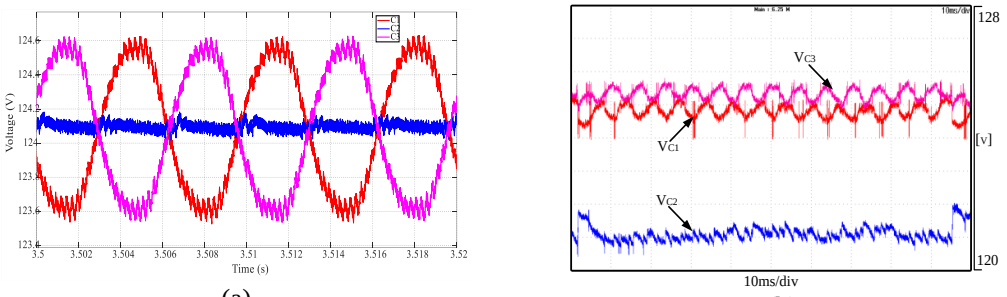


(b)

Fig. 10. Control-based dc link capacitor voltage balancing showing (a) simulation and (b) HIL implementation results.

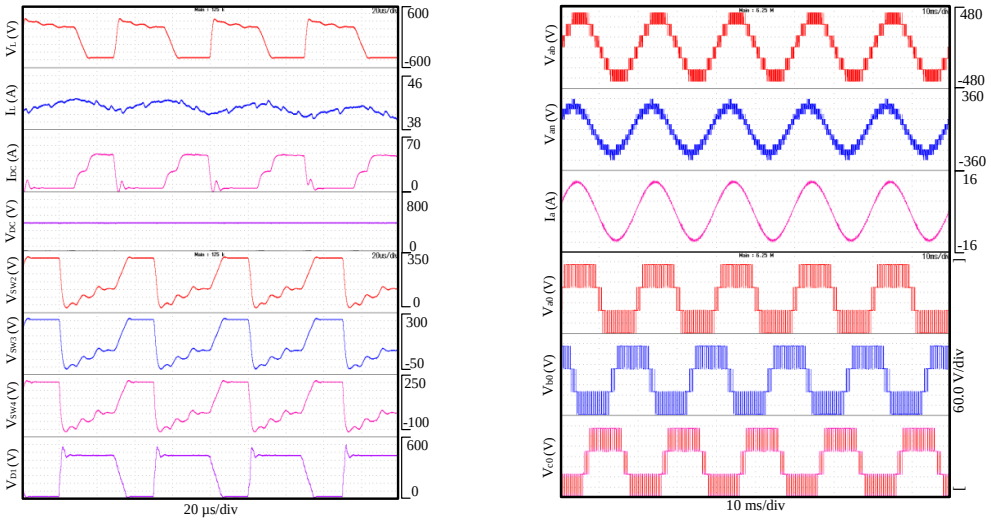
oscillation. Comparing the HIL implementation results of the control-based, Fig. 10 (b), and circuit-based, Fig. 11 (b) techniques, the later can more equally balance the voltage left over between C_1 and C_3 after controlling V_{C2} to a specified value. Further less controller effort is required in the circuit-based topology, but of course requires additional components while the control-based technique requires a complex controller although not requiring any additional components. Thus, a trade-off between control complexity and component count is required for a choice to be made between both techniques.

In addition, the integrated converter system was operated with the MDC in closed loop such that V_{DC} was controlled to 400 V for HIL implementation. The closed loop strategy for MDCs described in [20] was adopted for the MDC in this paper. The PI control variables for controlling the MDC were heuristically selected and desired dynamic performance characteristics achieved. Fig. 12 presented key measurements obtained from the integrated converter system under closed loop operation of the MDC section. Further, the control-based and circuit-based dc link capacitor voltage balancing techniques were further compared under closed loop operation and the results are presented in Fig. 13. Again, the circuit-based balancing technique performs slightly better in equally dividing the dc link voltage across the three capacitors without requiring the complex controller required in the



(a) (b)

Fig. 11. Auxiliary circuit-based dc link capacitor voltage balancing showing (a) simulation and (b) HIL implementation results.



(a) (b)

Fig. 12. Closed loop HIL implementation results showing (a) key waveforms of the MDC operation and (b) output current and voltage waveforms and the pole voltages.

control-based balancing technique. All these results validate the proposed integrated converter system for integrating RESs to both dc and ac grids.

IV. CONCLUSION

A novel integrated MDC and MLI converter system has been proposed in this research. The MDC facilitates the integration of multiple renewable energy sources such as photovoltaics, wind power and fuel cell systems into a dc and ac bus. It involves using less components and complications as compared to the counterparts in literature. The proposed integrated converter system has been analysed for three input sources under simultaneous power flow from the inputs. Further, two methods of dc link capacitor voltage balancing techniques were compared, with the circuit-based balancing technique, showing more attractive features than the control-based voltage balancing technique. The proposed integrated converter system was verified in numerical simulations and on an

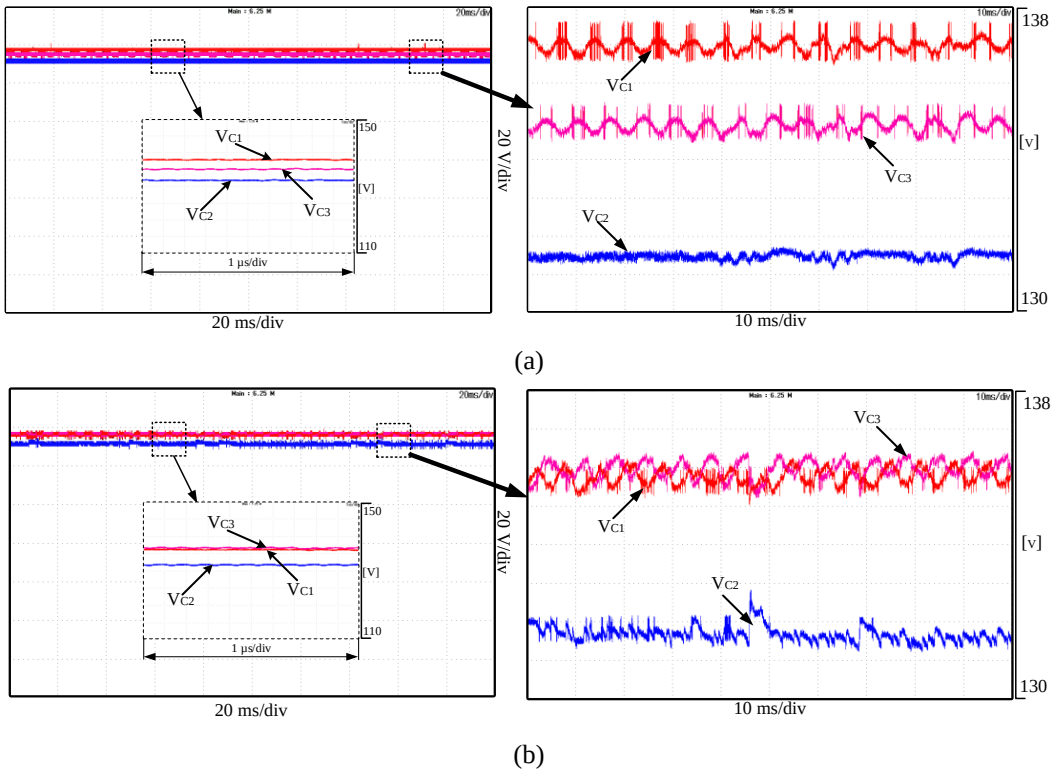


Fig. 13. HIL implementation results under closed operation of the MDC for (a) control-based dc link capacitor voltage balancing and (b) auxiliary circuit-based dc link capacitor voltage balancing.

FPGA-based HIL implementation platform in both in open and closed loop operations.

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Paper VI:

Novel High Gain Multiport Isolated DC-DC Converter with Bipolar Symmetric Outputs

This paper has been published as:

I. N. Jiya, H. Van Khang, N. Kishor and R. Ciric, "Novel High Gain Multiport Isolated DC-DC Converter with Bipolar Symmetric Outputs," *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968834.

Novel High Gain Multiport Isolated DC-DC Converter with Bipolar Symmetric Outputs

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***Abstract*— Due to their superior reliability, efficiency, and robustness as compared to unipolar dc grid systems, bipolar dc grid systems are quickly gaining traction for renewable energy integration. However, progress in developing multiport converters resulting in lower costs, more compact designs, and higher power density in bipolar microgrid systems has been slow. As a result, a new isolated multiport dc-dc converter with bipolar inherently symmetric outputs (MIBDC) is proposed in this study. The suggested converter has a competitive advantage over its few counterparts in terms of the number of input ports, voltage gain, and natural symmetry of the outputs. Furthermore, because the proposed MIBDC uses a fixed transformer with only one primary and secondary winding for any number of inputs, it considerably decreases component count and control complexity. The proposed converter's operation is quantitatively tested in simulation and on OPAL-OP5700 RT's hardware-in-the-loop (HIL) validation platform for independent and simultaneous power transfer from multiple sources with varying voltages.**

Keywords— buck-boost, bipolar dc bus, bipolar outputs, dc-dc converter, isolated converter, hardware-in-the-loop, multiple input converter, multi-source converter, renewable energy sources

I. INTRODUCTION

Over the past few years, the imminent depletion of fossil fuels and the adverse environmental effects of their usage to satisfy the increasing energy demands have championed the search for green alternatives [1]. Fuel cells, wind and photovoltaic (PV) systems have been proved to be suitable alternatives to provide the much needed green solutions [2]. The increased penetration of these renewable energy sources (RESs) has led to a paradigm shift in the electrical energy generation and utilization from centralised to distributed generation systems [3], which are majorly based on dc microgrids. Bipolar dc grids (BDCG) are a three-wire dc bus grid technology that is quickly gaining popularity as a technique to improve dc

microgrids. This rapid acceptance is owing to the improved efficiency of BDCGs, as the current required to transfer the same amount of power is lower than in unipolar dc grids (UDCGs). BDCGs are also more reliable than UDCGs because if one of the poles fails, the other pole can still transmit power, albeit at a lower capacity. Furthermore, because BDCGs have three voltage levels ($\pm\frac{V_o}{2}$ and V_o), converting from dc to ac voltage with multilevel inverters (MLIs) is easier and more reliable than with UDCGs, which only have one voltage level. RESs and dc loads can now be more easily integrated using dc-dc converters due to these appealing properties of BDCGs [4]. Nevertheless, various single-input single-output (SISO) dc-dc converters are required to step-up or step-down the voltage to or from the BDCG system since the voltage of many sources and loads is distinctively varied. As a result, a large number of components, particularly semiconductors, are required, in addition to bulky and complex configurations and high costs that arise amidst worldwide semiconductor chip shortages [5]. Multiport dc-dc converters (MPCs), which are generally derived from conventional SISO converters, have lately been offered as a solution to this problem [6–9].

To this end, a lot of research has gone into proposing several MPCs with and without galvanic isolation. Due to the magnetic separation of input and output given by the magnetic components, isolated MPCs have significant features of soft switching ability, high gain, and safety over non-isolated MPCs. In [6, 7], MPCs with multiple-inputs and single-outputs (MISO) based on half-bridge, full-bridge (FB), dual active bridge (DAB) and multi active bridge (MAB) converters, have been proposed, but their common limitation is the use of multiple windings for the inputs of the transformers or coupled inductors based on flux additivity. This leads to reduced power density, increased size, and control complexity. Further, since multiple windings are required at the primary side of the magnetics for each input source, and multiple clamping circuits could also be required, further increasing component count and potentially control complexity if an active clamping is applied. To address these concerns, the authors in [8, 9] propose isolated MICs with only two windings, one primary and one secondary. However, they are all unsuitable for BDCG systems because they have only one output port. As a solution to this, MPCs with multiple inputs and outputs (MIMO) have been proposed in [10, 11], but these MIMO MPCs are plagued with an issue of cross-regulation of the voltage at the output ports, requiring complex controllers to suppress the cross-regulation problem. This problem birthed the need for bipolar

dc-dc converters (BDCs), which typically have only two symmetrical outputs, one for each pole (positive and negative), respectively. To resolve this, multiport bipolar dc converters (MBDCs) have been proposed recently in [12–15]. The non-isolated MBDCs in [12, 13] have low gain, power density, and only two inputs to the MPC, thus they can't be expanded to have an arbitrary number of inputs, which is one of the key features of MPCs. Although the multiport isolated bipolar dc converters MIBDCs proposed in [14, 15] feature soft switching in some cases, just like the non-isolated counterparts in [12, 13], they both cannot allow for an arbitrary independent power flow from either of the input sources to the bipolar dc bus, aside the requirement for complex control to achieve balanced symmetric output voltages, significant component count, limitation on number of inputs and low voltage gain. These disadvantages underline the demand for novel isolated MIBDCs to fill the need. Furthermore, compared to their unipolar counterparts, fewer isolated MPCs with bipolar naturally symmetric outputs have been proposed in literature.

By adopting a DAB-based and a FB-based topology with a fixed two winding (one primary and secondary winding each) transformer and many ports constructed using pulsing voltage sources, the MIBDC presented in this article addresses the constraints of previous topologies. The component count is kept minimal, while the single inductor is time multiplexed to allow for any arbitrary independent and simultaneous power transfer from multiple sources. The following features distinguish the proposed MIBDC: For whatever number of input sources, it just requires the usage of one primary and secondary winding. It can also transfer power from several sources with variable voltage levels to the dc bus at the same time. With bipolar output voltages and high gain, the proposed MIBDC can perform unidirectional buck and boost operations. Further, it is modular, in which the number of inputs can be increased arbitrarily by simply adding a reverse blocking switch to each one. Within this framework, the proposed MBDC was analysed for two input sources with equal and unequal input voltage levels, tested in comprehensive simulations, and implemented on an in-house high fidelity real-time hardware-in-the-loop (HIL) platform.

II. PROPOSED MIBDC TOPOLOGY

Fig. 1 presents the proposed multiport isolated dc-dc converters with bipolar symmetric outputs (MIBDC). These converters are synthesized by the integration of a traditional DAB or a phase-shifted full bridge (PS-FB) converter, which has

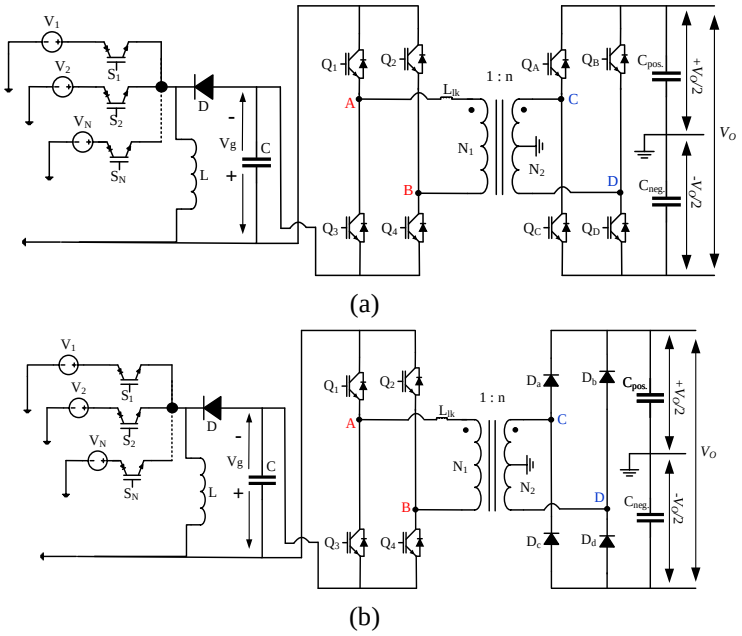


Fig. 1. Proposed (a) dual-active-bridge and (b) full-bridge -based bipolar multiport dc-dc converter.

been modified to use a secondary side center tapped transformer to achieve bipolar symmetry on the outputs. The multiple inputs are achieved through pulsating voltage sources and a time multiplexed inductor charging scheme to control the output voltage and facilitate the inclusion of inputs of varying voltage levels. To reduce the control complexity of the DAB section in Fig. 1 (a), the converter in Fig. 1 (b) is proposed by replacing the secondary active bridge with a diode H-bridge. Thus, it is similar to the conventional PS-FB converter with the introduction of the secondary side center tapping of the isolation transformer to facilitate bipolar outputs. Both topologies in Fig. 1 have the same multi-input power processing mechanism, involving reverse blocking switches S_1 to S_N, one diode, capacitor and inductor, respectively. The use reverse blocking switches facilitate the integration of multiple sources of varying voltage levels under independent and simultaneous power flow from the sources. Furthermore, the converters can provide three voltage levels, $\pm V_o/2$ and V_o, on the dc links. For the steady state continuous conduction mode (CCM) analysis in this paper, the MIBDC proposed in Fig. 1 (b) will be analyzed for two inputs under individual and simultaneous power transfer modes, since the key principles of operation described are essentially applicable from PS-FB to the DAB based MIBDC.

A. Independent Power Flow in Steady State CCM

The independent power flow mode of the proposed converter is characterized by power flow from any of the inputs (V_1 or V_2 for a two-input converter) to the bipolar

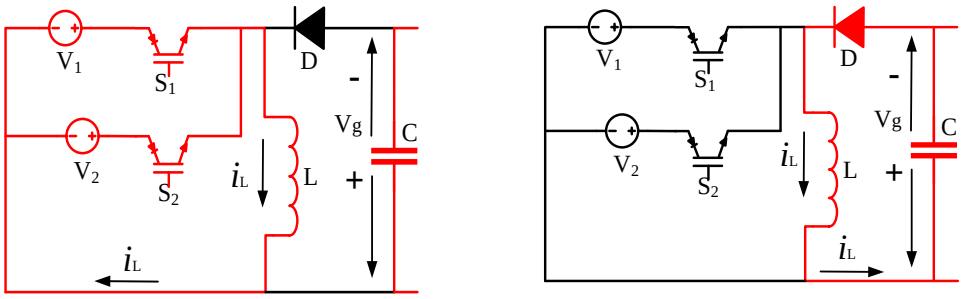


Fig. 2. Path of current flow in in the multiport section during (a) charging and (b) discharging of *L*, for simultaneous power flow with two inputs.

dc bus. The respective switch controlling each input source S_1 for V_1 or S_2 for V_2 is turned ON to charge the inductor, *L*, for a period of DT_S, where D is the duty cycle and T_S is the total switching period. During $(1\text{-}D)T_S$, the OFF time of the respective switch, diode D conducts in the direction as described in Fig. 2 (b) to discharge *L*. Thus, the multiport section operates like a standard inverting buck-boost converter and capacitor C, has a voltage described by (1). While the multiport section is in operation, the PS-FB section is also operating simultaneously as described in Fig. 3. The operation of the PS-FB part is described in detail, in section II. C. Under steady state CCM operation, the relationship between the input voltage and the dc link is described by (2), where Ø is the phase shift and *n* is the turn ratio (N_S/N_P) of the transformer.

$$V_g = (V_{in}D)/(1-D) \tag{1}$$

$$V_o = [(V_{in}D)/(1-D)]2\phi n = 2V_g\phi n \tag{2}$$

B. Simultaneous Power Flow in Steady State CCM

When a power transfer is required from more than one input to the dc link as illustrated in Fig. 2 for two inputs, the converter switches to simultaneous power flow mode. The switches S_1 to S_N controlling all the sources are turned ON at the same time but turned OFF in the order of decreasing magnitude of the respective voltages. Thus, the charging of L is time multiplexed as illustrated in Fig. 3, for the power delivery from two inputs simultaneously.

In steady state CCM as illustrated in Fig. 3, the switching period is divided into two main parts, the charging and discharging times of *L*. The first part is further subdivided depending on the number of inputs of the MIC in simultaneous operation:two divisions (D_{1eff} and D_{2eff}) in this case while the second part

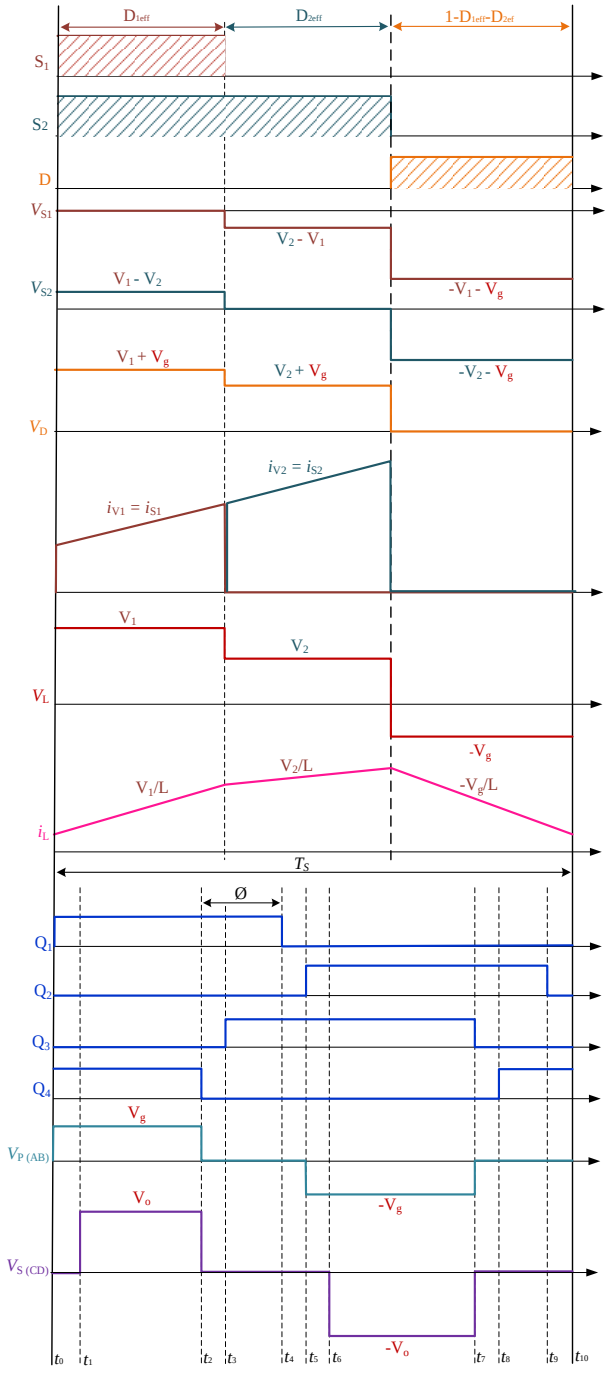


Fig. 3. Steady state key waveforms of the phase-shifted full-bridge based multiport bipolar dc-dc converter.

remains fixed as $(1 - \sum_{i=1}^{N} D_{ieff})$, indicating the discharging time of L. When the switches are turned ON, current flows from the source with the highest potential first or V_1 in this case, so L is charged with a slope of V_1/L during D_{1eff}. When the time D_{1eff} is elapsed, V_2 takes over to continue charging L with a slope of V_2/L during D_{2eff}. This continues up to D_{Neff} with a slope of V_N/L for any number of

inputs. At the end of the charging time, $\sum_{i=1}^{N} D_{ieff}$, L is discharged with a slope of $-V_g/L$. Also, while the multiport section is in operation, the PS-FB section is also operating simultaneously as described in Fig. 3. By applying volt-second balance of the resulting steady state CCM waveform in Fig 3, capacitor C, has a voltage as defined by (3) and the input-output voltage is described by (4).

$$V_g = \left[\left(1-\sum_{i=1}^{N} D_{ieff}\right) \Big/ \left(1-\sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3}$$

$$V_o = \left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1-\sum_{i=1}^{N} D_{ieff}\right)\right] 2\phi n = 2V_g \phi n \tag{4}$$

For an effective commutation of the switches in multi-input mode, some principles need to be respected to achieve simultaneous power transfer to the load. When the voltages are unequal, the magnitude of the sources is arbitrarily arranged in order of decreasing magnitudes such that $V_1 > V_2 > \cdots > V_N$, the duty cycles of the PWM signals of controlling the input sources, e. g S_1 and S_2, must be such that $D_1 < D_2 < \cdots < D_N$, and vice versa, where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ..., $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. However, if the source voltages are equal such $V_1 = V_2 = \cdots = V_N$, duty cycles of the PWM signals must be in such a way that $D_1 = D_2 = \cdots = D_N$ to achieve an equal power delivery from the sources. If the required power delivery from the sources is unequal, $D_1, D_2, \ldots, D_N$ can be determined in order of increasing magnitude of the required power delivery from the respective sources.

C. Transformer Bridge Section

The isolation transformer section of the MIBDC is operated in such a way that the active switches, Q_1 – Q_4 experience zero voltage switching (ZVS). Detailed explanation of this operation is presented in [16] and summarized in this section. The pulse signal for these switches is presented on the steady state waveform in Fig. 3. The total switching period for Q_1 – Q_4 is divided into 10, (t_0 – t_{10}) to accommodate the phase shift ($\emptyset$) and the deadtime required to achieve ZVS. At t_0, Q_1 and Q_4 are ON with Q_1 turned ON at t_0 and Q_1 turned ON at t_8, in the previous cycle, both with ZVS. V_S remains 0, until t_1 when the current in the primary winding reverses to positive and V_S becomes equal to $2nV_g$ or V_o, and V_P is equal to V_g. Diodes D_a and D_d are forward biased to charge $C_{pos.}$ and $C_{neg.}$ up to $\pm V_o/2$, respectively, for the positive and negative poles and V_o across the full dc link

thereby also supplying the load. At t_2, Q_4 is turned OFF, V_P and V_S become 0 and after a deadtime ($t_3 - t_2$), Q_3 is turned ON with ZVS at t_3. At t_4, Q_1 is turned OFF and after the deadtime ($t_5 - t_4$), Q_2 is turned ON with ZVS, V_P becomes $-V_g$ and the primary current begins reversal to negative until t_6 when it is completely negative and V_S also becomes $-V_o$. Between t_3 and t_6, diodes $D_a - D_d$ are reverse-biased, and $C_{neg.}$ and $C_{pos.}$ are discharging to supply the loads until t_6 when D_2 and D_3 are forward biased. At t_7, Q_3 is turned OFF and Q_4 is turned ON after the deadtime ($t_8 - t_7$) at t_8 with ZVS. Q_2 is turned OFF at t_9 and after a deadtime $t_{10} - t_9$, t_0 arrives when Q_1 turns ON again with ZVS, thus t_0 and t_{10} are essentially the same. Between t_6 and t_8, $C_{neg.}$ and $C_{pos.}$ are charging again then discharging to the load between t_8 and t_1 when diodes $D_a - D_d$ are reverse-biased.

D. Voltage Gain

The voltage gain of multiport converters is a little different from the gain of the single input forms from which they are synthesized [17]. Thus, multiport converter gains are best expressed as voltage transformation factor (V_{TR}). For the proposed converters, V_{TR} is expressed as (5). A high gain of up to $20Øn$ can be achieved for the proposed converter at an effective duty cycle (D_{ieff}) of 90%. Thus, the phase shift, $Ø$, and turns ratio, n, can be used to further increase the converter gain if higher gain is required.

$$V_{TR} = V_o \Big/ \left(\sum_{i=1}^{N} V_i D_{ieff} \right) = (2\phi n) \Big/ \left(1 - \sum_{i=1}^{N} D_{ieff} \right) \tag{5}$$

III. RESULTS

The proposed isolated MIC is quantitatively verified in simulation and tested using OPAL-RT's OP5700 device, which runs a 64-bit virtex-7 FPGA. The validation setup in the laboratory is shown in Fig. 4 [17]. The values of the various component's parameters are listed in Table I. The topology of MIBDC was anaysed in closed and open loop operation. Open loop operation was carried out in 5 scenarios, the first two representing independent power flow from the two sources (V_1 and V_2) to the dc link respectively. The last three open loop scenarios represent operation of the MIBDC in simultaneous power flow from both sources with equal and unequal voltage levels, respectively. And lastly, the converter was operated in closed loop to examine the natural symmetry capability of the converter's bipolar outputs.

Figs. 5 and 6, respectively, present the open loop simulation and HIL verification of operating the MIBDC with the first voltage source, V_1, and the second voltage source, V_2, supplying the bipolar dc link independently. For both scenarios, V_1 is set to 100 V, V_2 is 75 V and the results presented include inductor current (i_L) and voltage (V_L), primary (V_P) and secondary (V_S) turns voltage of the transformer, input currents, voltages of S_1 (i_{S1}, V_{S1}), S_2 (i_{S2}, V_{S2}), the dc link (i_{dc} and V_{dc}), and the voltage across the switches of the PS-FB section, $V_{Q1} – V_{Q4}$ and $V_{Da} – V_{Dd}$. In Fig. 5, the results of V_1 alone supplying are presented. To achieve this, the duty cycle, D_1, of the switch, S_1, controlling the first voltage source, V_1, is set to 0.4 while that of S_2, D_2 is set to 0. The load across each pole and the full dc link was set to 200 Ω each. In the simulation in Fig. 5(a), $\pm V_o/2$ and Vo is about ±125 V and 251 V, respectively while $\pm i_o/2$ and i_o is about 0.63 A and 1.3 A, respectively. Further, the HIL results presented in Fig. 5(b) show congruent results with $\pm V_o/2$ and V_o at about ±123 V and 245 V, respectively, and $\pm i_o/2$ and i_o at about ±0.6 A and 1.2 A. In Fig. 6, the results of independent power flow from V_2 are presented. D_1, the duty cycle of S1 was set to 0, while that of S_2, D_2 was set to 0.4. The load across each of the voltage levels was also 200 Ω each. In the simulation results in Fig. 6(a) $\pm V_o/2$ and V_o are about ±93 V and 186 V, respectively, and $\pm i_o/2$ and i_o are about ±0.47 A and 0.93 A, respectively. Again, the HIL results in Fig. 6(b)

TABLE I
PARAMETERS USED IN VERIFICATION

Parameter	Value	Unit
Inductor (L)	1	mH
Capacitors (C=$C_{pos.}$=$C_{neg.}$)	4.7	µF
Voltage sources (V_1/V_2)	100/75	V
Transformer turns ratio (n)	2	
Phase shift ($Ø$)	27	degrees
Switching frequency (Fsw)	20	kHz

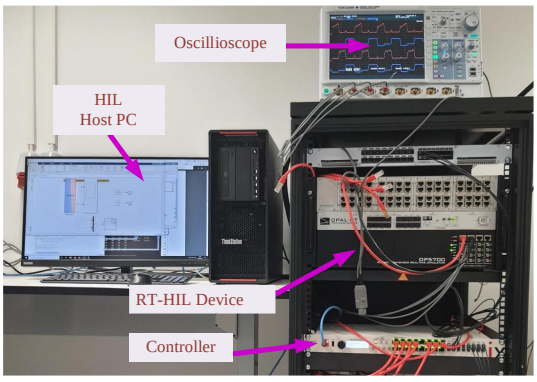
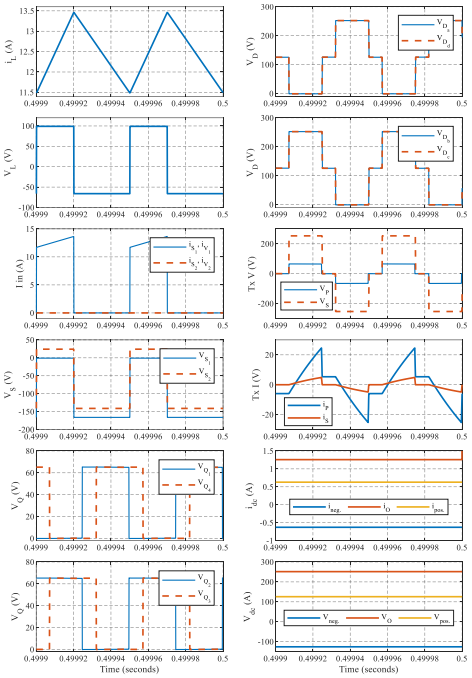


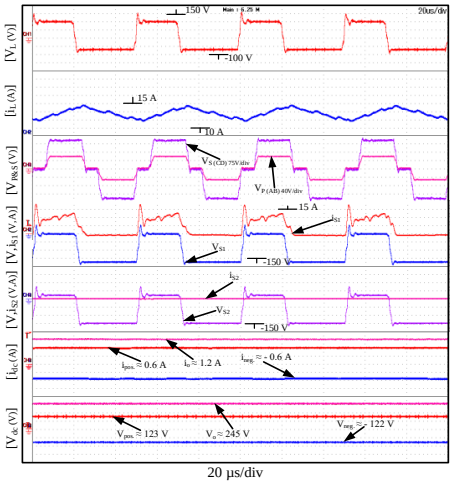
Fig. 4. In-house HIL platform used for validating the MIC.

shows good agreement with $\pm V_o/2$ and V_o being about ±90 V and 180 V respectively and $\pm i_o/2$ and i_o at about ±0.45 A and 0.9 A respectively.

Figs. 7 – 9 present the results of the last three scenarios of open loop operation, i.e. simultaneous power transfer from the two inputs to the bipolar dc link. Figs. 7 and 8 have the same output characteristics since they have the same effective duty, $\sum_{i=1}^{N} D_{ieff}$, of 0.6 and equal input voltages with V_1=V_2=75 V. $\pm V_o/2$ and V_o are about ±212 V and 424 V, respectively, and the currents, $\pm i_o/2$ and i_o are about ±1.06 A and 2.12 A, respectively, for both simulation results in Figs. 7(a) and 8(a). While

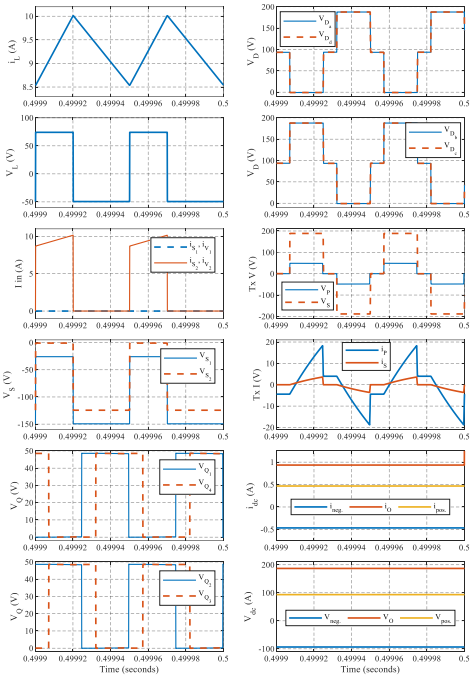


(a)

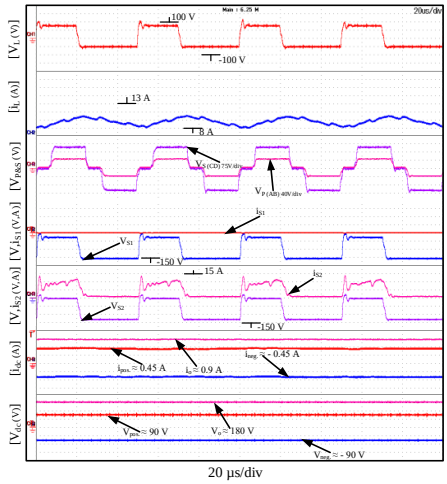


(b)

Fig. 5. Results when only V_1 is supplying the dc bus for (a) simulation and (b) HIL test platform where V_1=100V, V_2=75V, D_1=0.4 and D_2=0.



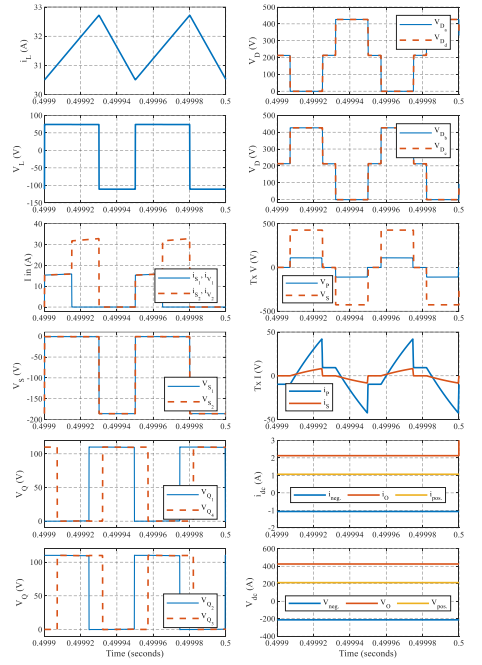
(a)



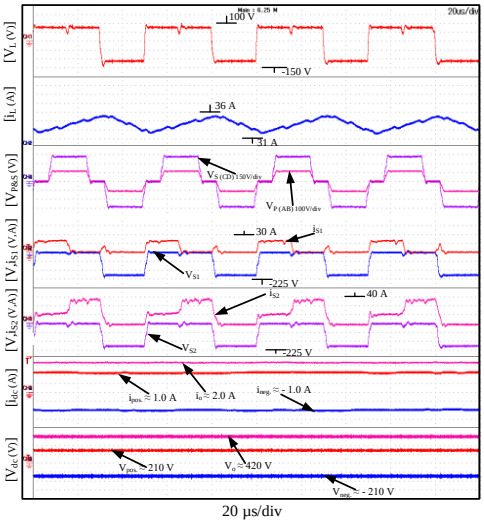
(b)

Fig. 6. Results when only V_2 is supplying the dc bus for (a) simulation and (b) HIL test platform where V_1=100V, V_2=75V, D_1=0 and D_2=0.4.

the HIL verification results in Figs. 7(b) and 8(b) are also consistent with the simulation with $\pm i_o/2$ and i_o being about ±1.0 A and 2.0 A respectively and $\pm V_o/2$ and V_o at about ±210 V and 420 V, respectively. The main difference with both scenarios is that D_1 was set to 0.3 and D_2 to 0.6 in Fig. 7 such that D_{1eff}=0.3 and D_{2eff}=0.6, so since both voltages are equal, while S_1 is ON, S_2 is also ON and both sources are charging the inductor, L, and then when D_1 goes OFF, only D_2 is charging L. Thus, the average i_{S2} is larger than from i_{S1}, while in Fig. 8, D_1=D_2=0.6

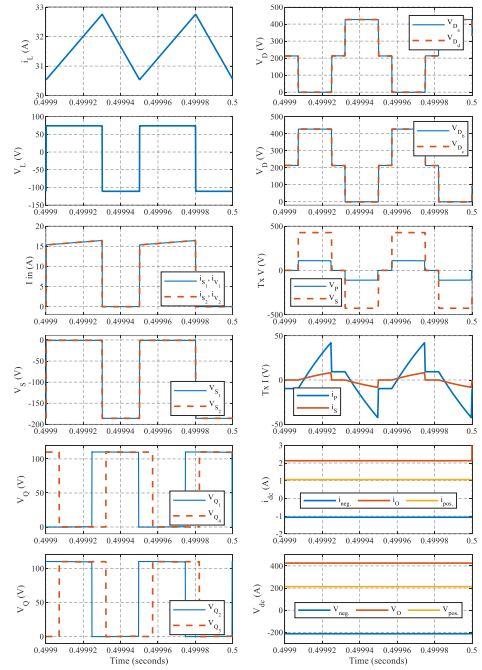


(a)

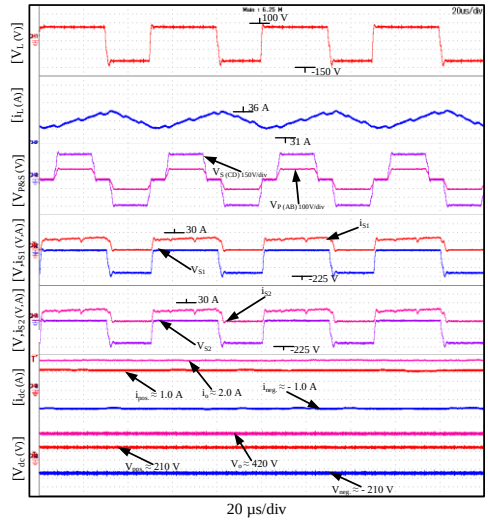


(b)

Fig. 7. Results when both sources are supplying the dc bus for (a) simulation and (b) HIL test platform where V_1=V_2=75V, D_1=0.3 and D_2=0.6.



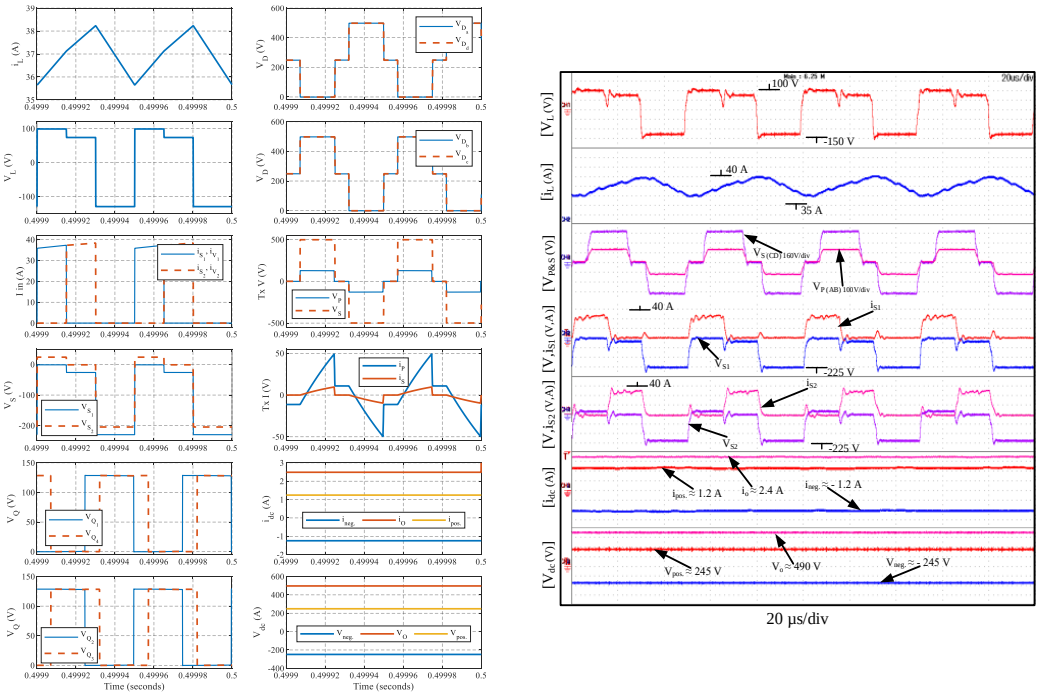
(a)



(b)

Fig. 8. Results when both sources are supplying the dc bus for (a) simulation and (b) HIL test platform where V_1=V_2=75V and D_1=D_2=0.6.

and so since they have equal voltages, both sources are charging the inductor with currents i_{S1}=i_{S2} during the inductor charging. This is an indication of how the duty cycle is used to control the energy delivered by the respective sources. In the case of the fifth scenario in Fig. 9, where the voltages are different such that V_1 = 100V



(a) (b)

Fig. 9. Results when both sources are supplying the dc bus for (a) simulation and (b) HIL platform where V_1=100V, V_2=75V, D_1=0.3 and D_2=0.6.

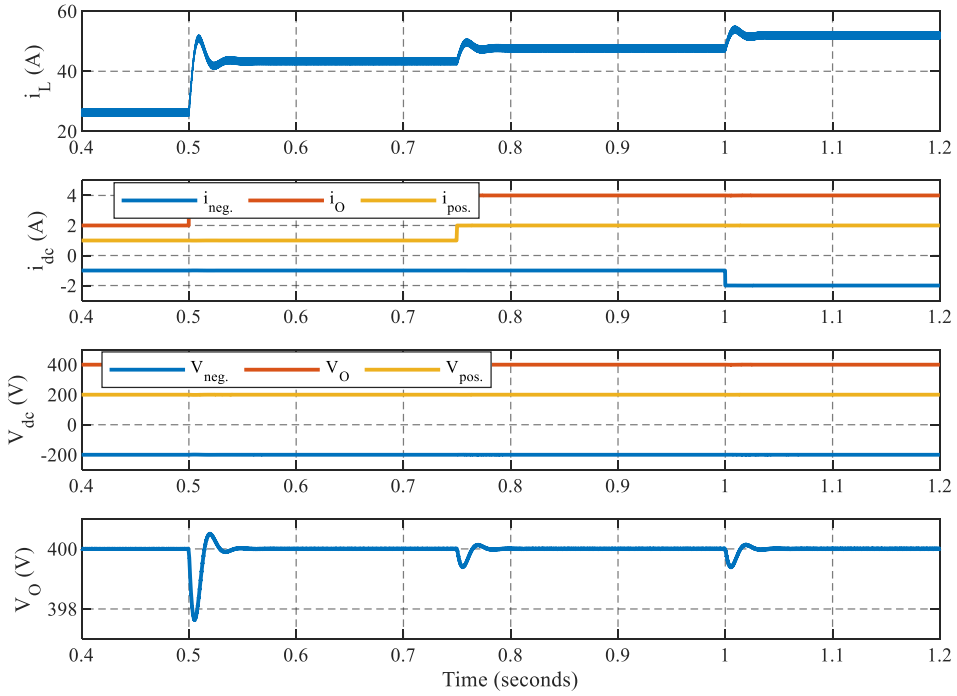


Fig. 10. Voltage symmetry verification of unbalanced load in closed loop.

and V_2 = 75 V, the inductor charging as described earlier in section II B, must be time multiplexed to achieve simultaneous power transfer from both sources to the load. In this case, D_1 was set to 0.3 and D_2 to 0.6 such that $D_{1eff}=D_{2eff}=0.3$. In the simulation results in Fig. 9(a), $\pm V_o/2$ and V_o are ±248 V and 496 V, respectively and $\pm i_o/2$ and i_o are about ±1.24 A and 2.48 A, respectively. Also, the HIL verification results in Fig. 9(b) are consistent with $\pm V_o/2$ and V_o being ±245 V and 490 V, respectively, and the dc link currents at $\pm i_o/2$ and i_o being ±1.2 A and 2.4 A, respectively.

Further, PI gains were heuristically selected to control the MIBDC as previously described in [17] to achieve a constant output voltage of $\pm V_o/2$ and V_o of ±200 V and 400 V respectively. Some of the closed loop dynamics are presented in Fig. 10, specifically the load on the three voltages were randomly varied to examine the natural symmetry characteristics of the MIBDC more closely. The controlled variable was V_o while the positive and negative poles were left uncontrolled to freely balance the voltage across itself. The load on V_o was doubled from about 2 A to 4 A at 0.5 seconds and V_o experiences a dip of less than 3 V after that the controller can bring it back to the target 400 V. And then the load on the positive pole was also doubled from 1 A to 2 A at 0.75 seconds and the negative pole's load also doubled from 1 A to 2 A at 1 second. In the load change for both positive and negative poles, a voltage sag of less than 1 V was experienced on V_o but overall, the load changes on the poles of the MIBDC does not lead to an imbalance in the output voltages, a testament of the natural symmetry of the converter.

IV. CONCLUSION

A novel unidirectional multiport isolated dc to dc converter with bipolar symmetric outputs based on dual active bridge and phase-shifted full bridge topologies has been proposed in this research. The proposed MIBDC has been analyzed and verified for two inputs with equal and unequal input voltages at different duty cycles. The operation of the MIBDC in independent and simultaneous power transfer from the sources to the dc link under different duty cycles was demonstrated. Further, the feature of natural symmetry of the dc link under unbalanced loads at the dc link, a very vital feature of bipolar converters was demonstrated and verified. The results presented in this paper show the verification in simulation and on the in-house hardware-in-the-loop (HIL) platform. The proposed MIBDC can be implemented for energy harvesting in PV farms and other renewable energy systems with DC voltage sources.

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Paper VII:

Multiport DC-DC Converter for Integrating Energy Systems in All-Electric Vehicles

This paper has been published as:

I. N. Jiya, P. Gunawardena, H. Van Khang, N. Kishor and Y. Li, "Multiport DC-DC Converter for Integrating Energy Systems in All-Electric Vehicles," *2023 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, Venice, Italy, 2023, pp. 1-6, doi: 10.1109/ESARS-ITEC57127.2023.10114856.

Multiport DC-DC Converter for Integrating Energy Systems in All-Electric Vehicles

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***Abstract*— In this paper, a new non-isolated multiport dc-dc converter (MPC) of non-inverting buck-boost configuration is proposed for integrating multiple energy resources in automotive applications. A typical example of such automotive application is an electric vehicle (EV), powered by one or more renewable energy sources (RESs) and consisting of one or more energy storage systems (ESSs), e.g. batteries and supercapacitors. The inputs to the MPC are clustered based on source or storage and integrated using uni- or bi-directional switches, respectively. It is capable of bi-directional operation between the storage cluster and the dc link, allowing for a simultaneous transfer of energy from more than one source of varying voltage levels (irrespective of its' cluster) to the dc link. The proposed MPC is analysed for four inputs, comprising of two per cluster in this paper. As compared to existing MPCs in literature, the proposed converter utilizes a fixed number (two) of inductors and is robust such that it requires only one additional switch to integrate any extra energy storage or source in a respective cluster. Different operating modes of the proposed MIC are numerically verified and validated on OPAL-RT's OP5700 hardware-in-the-loop (HIL) platform.**

Keywords— Bidirectional DC-DC power converter, buck-boost, four quadrant switch, multiple input converter

I. INTRODUCTION

The rapidly evolving energy market situation across the globe continues to underscore the need for advancements towards efficient and effective utilisation of renewable or green energy technologies [1, 2]. Due to the intermittent and non-dispatchable nature of renewable energy sources (RES), hybridisation of energy sources and storages has been the theme of intensive research in this field [3]; as it is an effective and economical solution to improve the performance of RE

systems. In addition to finding relevance in dc microgrids, hybrid energy systems have become pivotal in energy systems of all-electric systems especially in zero-emission transportations such as ferry boats [4] and electric vehicles (EVs) [5]. Further, effective implementation and utilisation of RE technologies cannot be achieved without dc-dc converters [6].

The use of single input converters to integrate multiple power sources results in a bulky, unnecessarily complex setup and high cost [7]. Multiport converters (MPCs), both isolated and non-isolated, have been proposed in literature as a potential solution to deal with system integration under high penetration of various RESs and storages [8, 9]. The necessity of galvanic isolation in some hybrid power systems, and high voltage gains are some of the main benefits of MPCs with isolation [10]. Due to the galvanic isolation provided by magnetic components, isolated MPCs are typically complicated to operate and bulky in size [11]. As compared to their isolated counterparts, non-isolated MPCs have several odd advantages, such as ease of miniaturization, and smaller size (features which are very attractive for automotive applications), and in turn results in lower cost and complexity [12].

Some efficient non-isolated MPCs have been presented in [13–16] for integration of sources and storages in EVs and other non-automotive applications, but they often either sacrifice part counts for robustness and complexity or vice-versa. Further, they often either focus on hybridising the RESs and leaving out the energy storage systems (ESS) or the other ways round, thus losing some robustness. Therefore, there is evidently room for improvement in developing highly efficient and robust MPCs to facilitate hybridisation of multiple energy sources and storages [17].

In this research, a novel non-inverting buck-boost MPC is proposed to fill this gap by creating a balance among component count, robustness, and control complexity using clustered input sources, unidirectional and bidirectional switching devices. The application area considered for the proposed MPC is in integrating RESs and ESSs in EVs i.e. the hybridisation of RESs e.g. solar photovoltaic (PV) and fuel cells as well as supercapacitors and batteries as the ESSs to the dc link of the EV. The proposed MPC is capable of bidirectional operation to the ESS cluster and can simultaneously transfer power from any inputs of varying voltage levels to the dc link. It is also capable of exclusive power transfer from the RES to the ESS clusters, while utilising a fixed number of magnetic components as against other existing converters in literature. Further, the proposed MPC is robust such that the

number of inputs can be arbitrarily increased with minimal alterations. The operation of the MPC is numerically verified and validated using high-fidelity real-time hardware-in-the-loop (HIL) platform.

II. PROPOSED MPC TOPOLOGY

Fig. 1 presents the proposed non-isolated MPC, consisting of two inductors, one capacitor, reverse-blocking switches (RBSs) and fully controllable bidirectional switches (FBSs). The proposed MPC is of the H-bridge structure with buck-boost characteristics, cognate to the MPCs proposed in [14, 15]. The input sources are grouped into two clusters with one consisting of the energy sources and the other energy storages. The energy source cluster, which can be used in integrating sources such as solar PVs, is highlighted in blue color in Fig. 1 with the associated inductor. Since the energy sources are unidirectional in nature, RBSs are used to integrate them into the converter system. Since there are rather few options of RBSs on the market, to realize the RBS, a diode can be connected in series to a regular FET instead [18]. Conversely, the energy storage (e.g., battery, supercapacitors etc.) cluster highlighted in red color utilises FBSs since they are bidirectional in nature. Also known as AC switches, bilateral switches, four-quadrant switches, or matrix switches, FBSs can control the on-state current and off-state voltage bidirectionally [19]. As illustrated in Fig. 1, FBSs consist of two gates which direct the flow of current through the switch. New monolithic FBSs, using two RBSs connected in anti-parallel can eliminate two discrete anti-parallel diodes as required in the conventional FBS [20]. The proposed MPC is thus robust, being capable of over twenty different modes of operation for a two-cluster configuration consisting of two inputs per cluster. In this configuration, the MPC operation summarized on Table I can be classified into the single- and multi-input interaction. The single-input interaction covers bidirectional power flow between the dc link and the energy storage cluster (V_3 and V_4.) individually. Similarly, unidirectional power flow from the energy source cluster (V_1 and V_2.) to the dc link and to the energy storage cluster (V_3 and V_4.) individually. The multi-input interaction consists of several combinations of power flow across both clusters to deliver power to the dc link simultaneously. The proposed MPC can also deliver power simultaneously from all or any combination of the inputs to the dc link and simultaneously from the energy source cluster to the energy storage cluster individually.Fig. 1 presents the proposed non-isolated MPC, consisting of two inductors, one capacitor, reverse-blocking switches (RBSs) and fully controllable

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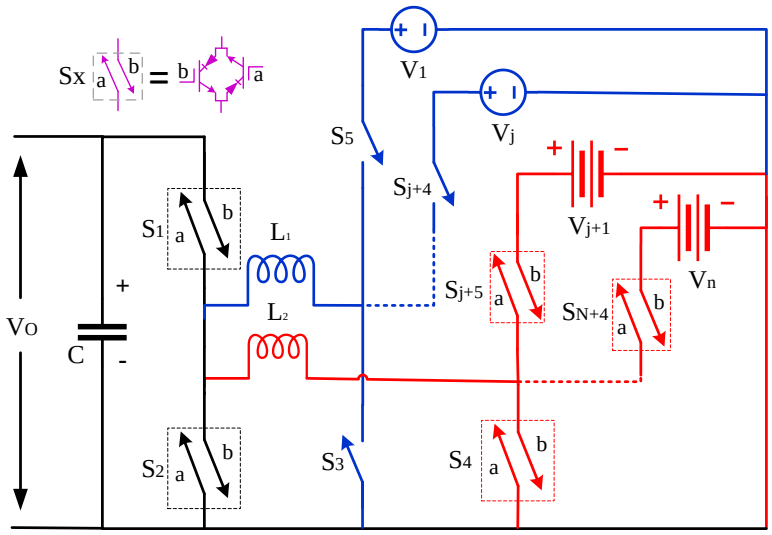

Fig. 1. The proposed MPC for integrating multiple energy sources and storages to the dc link of the EV.

TABLE I
SWITCHING PATTERN FOR THE DIFFERENT MODES OF OPERATION

Mode of Operation	Switching Pattern	
	T_1	T_2
V_1 & V_2 to V_3	S_5, S_6, S_{4b}	S_3, S_{7a}
V_1 & V_2 to V_4	S_5, S_6, S_{4b}	S_3, S_{8a}
V_1 & V_2 to dc link	S_5, S_6, S_{2b}	S_3, S_{1a}
V_3 & V_4 to dc link	S_{7b}, S_{8b}, S_{2b}	S_{4a}, S_{1a}
V_1 & V_3 to dc link	S_5, S_{7b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_2 & V_3 to dc link	S_6, S_{7b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_1 & V_4 to dc link	S_5, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_2 & V_4 to dc link	S_6, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_1, V_2 & V_3 to dc link	S_5, S_6, S_{7b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_1, V_2 & V_4 to dc link	S_5, S_6, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_1, V_3 & V_4 to dc link	S_5, S_{7b}, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_2, V_3 & V_4 to dc link	S_6, S_{7b}, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}
V_1, V_2, V_3 & V_4 to dc link	S_5, S_6, S_{7b}, S_{8b}, S_{2b}	S_3, S_{4a}, S_{1a}

bidirectional in nature. Also known as AC switches, bilateral switches, four-quadrant switches, or matrix switches, FBSs can control the on-state current and off-state voltage bidirectionally [19]. As illustrated in Fig. 1, FBSs consist of two gates which direct the flow of current through the switch. New monolithic FBSs, using two RBSs connected in anti-parallel can eliminate two discrete anti-parallel diodes as required in the conventional FBS [20]. The proposed MPC is thus robust, being capable of over twenty different modes of operation for a two-cluster configuration consisting of two inputs per cluster. In this configuration, the MPC operation summarized on Table I can be classified into the single- and multi-input interaction. The single-input interaction covers bidirectional power flow between the dc link and the energy storage cluster (V_3 and V_4.) individually. Similarly, unidirectional power flow from the energy source cluster (V_1 and V_2.) to the dc link and to the energy storage cluster (V_3 and V_4.) individually. The multi-input interaction consists of several combinations of power flow across both clusters to deliver power to the dc link simultaneously. The proposed MPC can also deliver power simultaneously from all or any combination of the inputs to the dc link and simultaneously from the energy source cluster to the energy storage cluster individually.

In contrast to conventional MPCs, which require n inductors for N input sources and two additional switches [14], the proposed MPC utilizes only one inductor per cluster and for any input sources. It needs only one additional FBS or RBS when introducing an input port to any of the respective clusters. Further, the proposed MPC can integrate both energy sources and storages as against its close competitor in [15] which can only integrate storages. Six key operating modes of the proposed MPC as illustrated in Fig. 2 are analysed for steady state continuous conduction modes (CCM) of operation in the following sub sections.

A. Single Input Interraction in Steady State CCM

The single input interaction between the ports of the MPC basically refer to independent power flow from the input ports to the dc link, the reverse flow of power from the dc link to the energy storage cluster and similarly the individual recharging of the energy storages directly from the energy source cluster. Therefore, the conventional equation (1) describing the relationship between the input and output voltage of the basic buck-boost converter applies to this converter as well for single input interaction modes. Where 'd_x' is the duty ratio applied

across the switches. Where d_x is the ratio of the respective inductor charging time to the total switching period, that is $d_x = T_1/T_S$.

$$V_{out} = \frac{T_1}{T_2} V_{in} = \frac{d_x}{1-d_x} V_{in} \tag{1}$$

B. Multiple Input Interraction in Steady State CCM

In multi-input mode, where both energy sources (cluster 1) V_1 and V_2 are simultaneously supplying the dc bus as illustrated in Figs. 2 (a) and 3 (V_1 & V_2 to dc link). During this mode of operation, the inductor charging period, T_1 is further subdivided into two or more, depending on the number of simultaneous input sources. This study analyses two inputs for the first cluster of the MPC thus only two sub-divisions of T_1 are required. During time T_1, switches S_5, S_6 and S_{2b} are all switched ON. However, in the first subdivision of T_1, the voltage across the inductor is the highest source voltage V_1. When the first subdivision period of T_1 is over, S_5 is OFF while S_6 and S_{2b} remain ON. In the second subdivision of T_1, the voltage across the inductor becomes V_2. This process will continue if the MPC had more than two inputs for the first cluster, in decreasing order of the magnitude in their input voltages. When T_1 is over, S_6 and S_{2b} are OFF, and the discharging

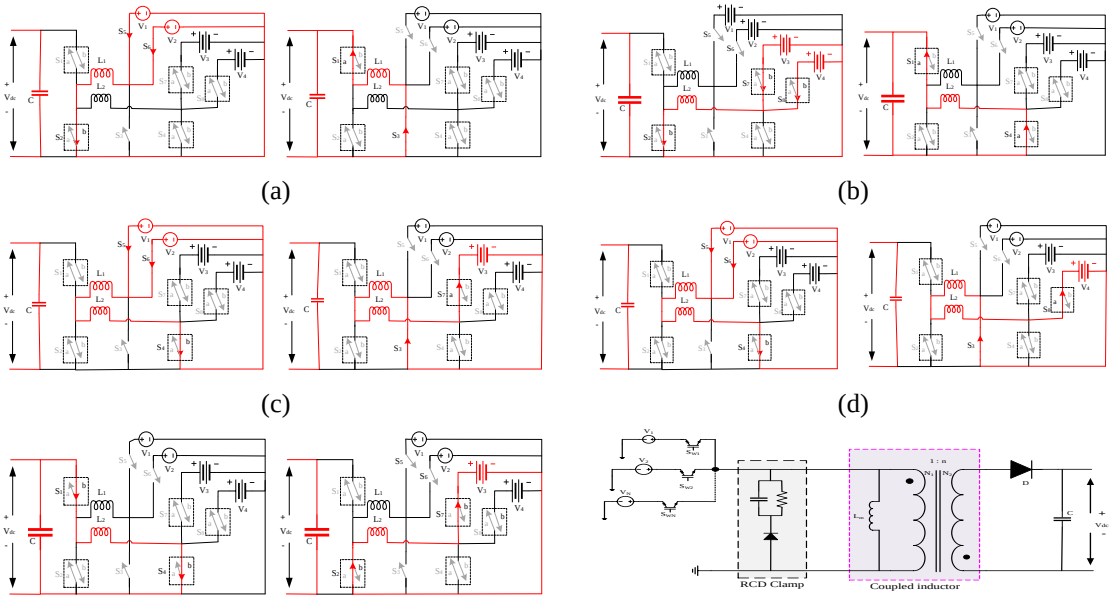

Fig. 2. Path of current flow in the MPC during the charging and discharging of the inductors where (a) is simultaneous power flow from energy source cluster to the dc link, (b) is simultaneous power flow from energy storage cluster to the dc link, (c & d) is simultaneous power flow from energy source cluster to the energy storage cluster respectively, (e) is power flow from the dc link to the first storage device and (f) is simultaneous power flow from both clusters to the dc link.

period T_2 starts. During T_2, L_1 discharges through the capacitor C to the dc bus by turning ON S_{1a} and S_3, so the voltage across the inductor is $-V_o$. The effective voltage across the inductor from each input is given by the product of the effective ON time of that input and its voltage magnitude. As shown in Fig. 3 (V_1 & V_2 to dc link), this effective voltage is $D_{1eff}V_1$ for the first subdivision of the inductor charging time and $D_{2eff}V_2$ for the second subdivision. Therefore, L_1 will charge with a gradient of $\left[D_{1eff}V_1 + D_{2eff}V_2\right]/L_1$ during T_1 while it discharges with a slope of $-V_o/L_1$ during T_2.

Similarly, for simultaneous power flow from both energy storages (cluster 2) V_3 and V_4 are simultaneously supplying the dc bus as illustrated in Figs. 2 (b) and 3 (V_3 & V_4 to dc link) T_1 is also subdivided into two. During T_1, switches S_{7b}, S_{8b} and S_{2b} are all switched ON. In the first subdivision of T_1, the voltage across the inductor is the highest source voltage V_3. When the first subdivision of T_1 is over, S_{7b} is OFF while S_{8b} and S_{2b} remain ON. In the second subdivision of T_1, the voltage across the inductor becomes V_4. During T_2, L_2 discharges through capacitor C to the dc bus by turning ON S_{1a} and S_4, so the voltage across L_2 is $-V_o$. Therefore, as shown in Fig. 3 (V_3 & V_4 to dc link), the effective voltage for the first subdivision of the inductor charging time is $D_{3eff}V_3$ and $D_{4eff}V_4$ for the second subdivision. Therefore, L_2 will charge with a gradient of $(D_{3eff}V_3 + D_{4eff}V_4)/L_2$ during T_1 while it discharges with a slope of $-V_o/L_2$ during T_2.

Likewise, for simultaneous power flow from both clusters to the dc link, V_1, V_2, V_3 and V_4 are simultaneously supplying the dc bus as illustrated in Figs. 2 (f) and 3 (All inputs to dc link). Just as described above for simultaneous power transfer exclusively from each cluster, L_1 and L_2 are simultaneously time multiplexed to achieve concurrent power delivery to the dc link from all input sources. During time T_1, switches S_5, S_6, S_{7b}, S_{8b} and S_{2b} are all switched ON, in the first subdivision of T_1, the voltage across the L_1 and L_2 is V_1 and V_3 respectively. When the first subdivision of T_1 is over for any or both clusters S_5 and S_{7b} is OFF while S_6, S_{8b}, and S_{2b} remain ON until the end of the second subdivision when they are all OFF. During T_2, L_1 and L_2 are discharged through the capacitor C to the dc bus by turning ON S_{1a} S_3 and S_4, so the voltage across the inductor is $-V_o$. Hence, as shown in Fig. 3 (All inputs to dc link), the effective voltage for the first subdivision of L_1 charging time is $D_{1eff}V_1$ and $D_{2eff}V_2$ for the second subdivision. And that of L_2 is $D_{3eff}V_3$ and $D_{4eff}V_4$ for the first and second subdivision respectively. Therefore,

L_1 and L_2 will charge with a gradient of $(D_{1eff}V_1 + D_{2eff}V_2)/L_1$ and$(D_{3eff}V_3 + D_{4eff}V_4)/L_2$ during T_1 while they both discharge with a slope of $-V_o/L_1$ and $-V_o/L_2$ respectively during T_2.

Further, for simultaneous power flow from both energy sources (cluster 1) V_1 and V_2 to the energy storages (cluster 2) V_3 and V_4 as illustrated in Figs. 2 (c & d) and 3 (V_1 & V_2 to V_3 & V_4) respectively, T_1 is also subdivided into two. During T_1, switches S_5, S_6 and S_{4b} are all switched ON. In the first subdivision of T_1, the voltage across L_1 and L_2 is the highest source voltage V_1 and -V_1 respectively. When the first subdivision of T_1 is over, S_5 is OFF while S_6 and S_{4b} remain ON. In the second subdivision of T_1, the voltage across L_1 and L_2 becomes V_2 and -V_2 respectively. Therefore, as shown in Fig. 3, this effective voltage is $D_{1eff}V_1$ for the first subdivision of T_1 and $D_{2eff}V_2$ for the second subdivision. During T_2, L_1 and L_2 charge and discharge respectively to the energy storage cluster by turning ON

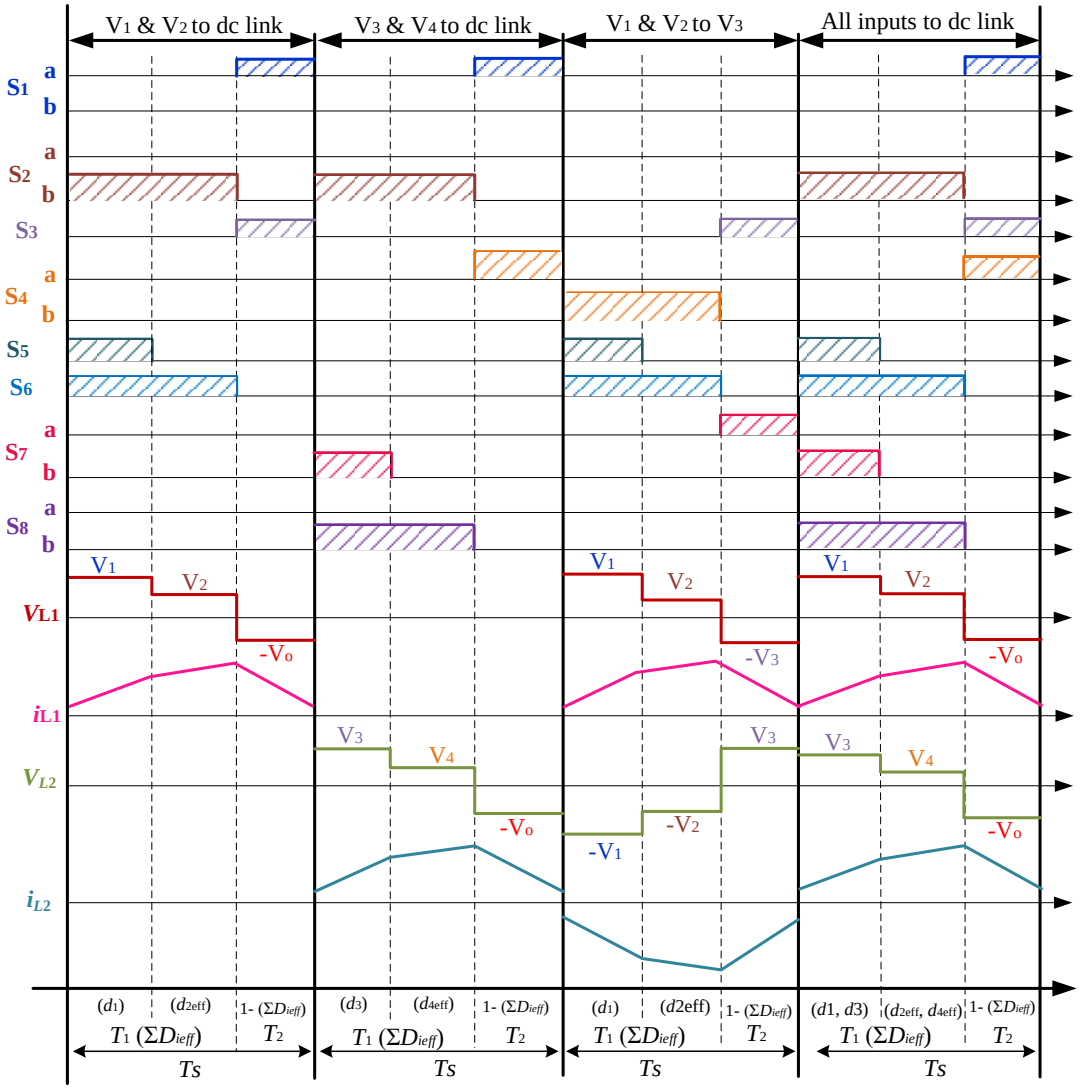

Fig. 3. Steady state waveforms of the MPC operation in CCM for key modes of operation.

S_3 and S_{7a} or S_{8a} depending on which energy storage device is being recharged (V_3 or V_4 respectively). Therefore, the voltage across L_1 and L_2 respectively during T_2 is $-V_3$ and V_3 or $-V_4$ and V_4 depending on which energy storage device is being recharged (V_3 or V_4 respectively). Thus, L_1 and L_2 will charge and discharge respectively with a gradient of $(D_{1eff}V_1 + D_{2eff}V_2)/L_1$ and $-(D_{1eff}V_1 + D_{2eff}V_2)/L_1$ during T_1 while during T_2 they discharge and charge with a slope of $-V_3/L_1$ or $-V_4/L_1$ and V_3/L_2 orV_4/L_2, depending on the energy storage device being charged.

By applying the volt-second balance to the steady state waveforms for multi-input interaction in Fig. 3, the relationship between the input sources and the output voltage is given by (2 – 3) for power delivery to the dc link exclusively from cluster 1 and 2 respectively and by (4) for when both clusters are supplying the dc link. For inter-port interaction, i.e. when the energy storages (cluster 2) are being recharged directly from cluster 1, the relationship between the source voltages and energy storage devices is described by (5).

$$V_O = \left[\sum_{i=1}^{j}\left(D_{(i)eff}V_i\right)\right] \Big/ \left[1 - \sum_{i=1}^{j} D_{(i)eff}\right] \tag{2}$$

$$V_O = \left[\sum_{i=j+1}^{N}\left(D_{(i)eff}V_i\right)\right] \Big/ \left[1 - \sum_{i=j+1}^{N} D_{(i)eff}\right] \tag{3}$$

$$V_O = \frac{\max.\left[\sum_{i=1}^{j}\left(D_{(i)eff}V_i\right), \sum_{i=j+1}^{N}\left(D_{(i)eff}V_i\right)\right]}{1 - \left[\max.\left(\sum_{i=1}^{j} D_{(i)eff}, \sum_{i=j+1}^{N} D_{(i)eff}\right)\right]} \tag{4}$$

$$V_3 \text{ or } V_4 = \left[\sum_{i=1}^{j}\left(D_{(i)eff}V_i\right)\right] \Big/ \left[1 - \sum_{i=1}^{j} D_{(i)eff}\right] \tag{5}$$

C. Commutation of Switches in Multi-Input Mode

For effective commutation of switches in multi-input interaction, some principles need to be respected to achieve simultaneous power transfer to the dc link or energy storage cluster (cluster 2). If the magnitude of the input voltages per cluster is arbitrarily arranged in order of decreasing magnitudes such that $V_1 > V_2 > \cdots > V_j$ for cluster 1 and $V_{j+1} > V_{j+2} > \cdots > V_N$ for cluster 2, the duty cycles of the PWM signals of controlling the input ports per cluster, must be in such a way that $D_1 < D_2 < \cdots < D_j$ for cluster 1 and $D_{j+1} < D_{j+2} < \cdots < D_N$ for cluster 2 and vice

versa. Where, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ... , $D_j = D_{1eff} + D_{2eff} + \cdots + D_{jeff}$ and $D_{j+1} = D_{j+1eff}$, $D_2 = D_{j+1eff} + D_{j+2eff}$, ... , $D_N = D_{j+1eff} + D_{j+2eff} + \cdots + D_{Neff}$ respectively for clusters 1 and 2. However, if the voltage magnitudes of any clusters are equal such that $V_1 = V_2 = \cdots = V_j$ then the duty cycles of the PWM signals must be in such a way that $D_1 = D_2 = \cdots = D_j$ in order to achieve equal power delivery from each of the sources. If the required power delivery from the sources is unequal, then D_1, D_2, ... , D_j can be determined in order of increasing magnitude from the respective sources.

D. Voltage Transformation Factor

The voltage gain of multiport converters is different from the gain of the single input forms from which they are synthesized since they can operate in a parallel configuration with multiple voltages involved [15]. Thus, multiport converter gains are best expressed as voltage transformation factor (V_{TR}). This is the relationship between the output voltage and its input voltages considering the duty of the switches controlling each respective input port to the MPC. For the proposed MPC, V_{TR} is defined by (6 – 8), for gain due to cluster 1 and 2 supplying the dc link and the interaction between cluster 1 and 2 respectively. Although V_{TR} for the proposed MPC is like the gain of a conventional boost converter, it is vital to note that the input voltages, compared to the output voltage, is the sum of the input voltages scaled by ON time of their respective switches ($\sum_{i=1}^{N} V_i D_{ieff}$). Thus, the typical analysis for the gain relationships of the basic converters cannot be applied for this MPC.

$$V_{TR-1} = V_o \Big/ \left[\sum_{i=1}^{j} D_{(i)eff} V_i \right] = 1 \Big/ \left[1 - \sum_{i=1}^{j} D_{(i)eff} \right] \tag{6}$$

$$V_{TR-2} = V_o \Big/ \left[\sum_{i=j+1}^{N} D_{(i)eff} V_i \right] = 1 \Big/ \left[1 - \sum_{i=j+1}^{N} D_{(i)eff} \right] \tag{7}$$

$$V_{TR} = V_3 or V_4 \Big/ \sum_{i=1}^{j} \left(D_{(i)eff} V_i \right) = 1 \Big/ 1 - \sum_{i=1}^{j} D_{(i)eff} \tag{8}$$

III. RESULTS

The proposed MPC topology was verified in simulation and validated on a HIL real-time validation platform using OPAL-RT's OP5700 device running a 64bit virtex-7 FPGA. Table II presents the selected components and parameters used and Fig. 4, presents the test setup used for the verification of the proposed MPC.

TABLE II
SWITCHING PATTERN FOR THE DIFFERENT MODES

Parameter	Value	Unit
Inductance (L_1/L_1)	1000/1000	µH
Output capacitor (C)	4.7	mF
Voltage sources (V_1/V_2/V_3/V_4)	100/50/150/75	V
Output voltage (V_o)	200	V
Load resistor	1000	Ω
Switching frequency (F_{sw})	20	kHz

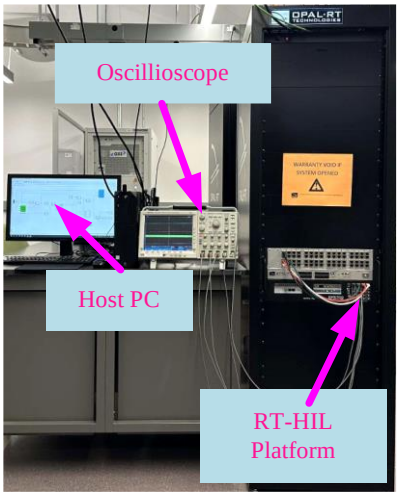

Fig. 4. In-house HIL platform used for validating the MPC.

Open loop verifications were performed by operating the MPC in various operation modes at different duty cycles, with some results presented in Fig. 5. This was done to ensure that the MPC's performance in simulation and HIL verification matched the expected analytical results. Notably, in Fig. 5 (a), D_2 and D_3 are fixed to 0.3 with D_4 is fixed at 0.6 while D_1 is varied from 0.1 to 0.9. Since the voltages in cluster 1 is less than that of the inputs in cluster 2 for in this case, a downtrend is observed in V_{TR} until the duty of 0.6 from which point the uptrend starts for both clusters. Similarly, in Fig. 5 (b), D_1 and D_3 are fixed to 0.3 and D_4 is fixed at 0.6 while D_2 is varied from 0.1 to 0.9. Again, a downtrend is observed between the D_2 of 0.3 and 0.6 due to the voltages in cluster 1 being less than that of cluster 2. Further, in all the cases considered, cluster 1 has a visibly higher V_{TR} than cluster 2 because their voltages are much lower than that of the inputs in cluster 1. Should this be reversed, V_{TR} of cluster 2 will also be visibly higher than that of cluster 1. Overall, from the results in Fig. 5, in all the cases considered, the trends are all congruent for analytical calculation, simulation and HIL verification. This is despite the expected losses in the detailed simulation and HIL verification at high (>0.8) duty cycles.

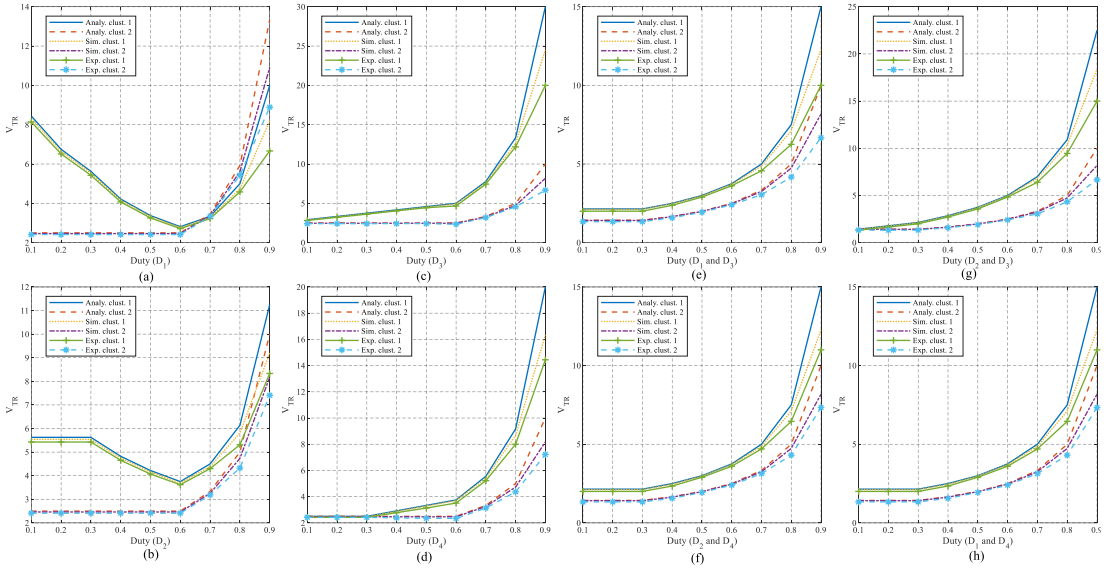

Fig. 5. Verification of the MPC with the obtained V_{TR} per cluster from analytical calculation, detailed simulation, and HIL experimental results for (a) D_2=D_3=0.3, and D_4=0.6, (b) D_1=D_3=0.3, and D_4=0.6, (c) D_1=0.3, and D_2=D_4=0.6, (d) D_1=D_3=0.3 and D_2=0.6, (e) D_1=D_3=0.3, (f) D_2=D_4=0.3, (g) D_2=D_3=0.3 and (h) D_1=D_4=0.3.

Closed loop verifications were also performed on the proposed MPC under the various modes of operations. The results presented in Fig. 6 verify some of the MPC's operation under simultaneous power transfer, showing the waveforms for inductor voltages (V_{L1} & V_{L2}) and currents (i_{L1} & i_{L2}), output current (i_o) and voltage (V_o), and the duty cycles controlling the input sources (D_1, D_2, D_3 & D_4) respectively. Figs. 6 (a) – (f) present the results of simultaneous power transfer from the inputs to the dc link, exclusively from cluster 1; cluster 2; V_1 and V_3; V_1, V_2 and V_4; V_1, V_3 and V_4; and from all inputs respectively. Noticeably, since cluster 1 and 2 are exclusively supplying power to the dc in Figs. 6 (a) and (b) respectively, the respective inductor voltage and current for the cluster not supplying the dc link results to zero. Further, when power is transferred simultaneously from both clusters as in Figs. 6 (c) – (f), the inductor current from either one of the clusters plateaus when the inductor stops charging while waiting for charging in to complete in the alternate inductor. In all the cases, V_o was set to a target of 200 V and hence the average io was about 2 A with acceptable ripples in i_L, i_o and V_o.

IV. CONCLUSIONS

In this research, a novel non-inverting, non-isolated buck-boost multiport dc-dc converter (MPC) has been proposed for integrating RESs and ESSs to the dc link of EVs. This is to achieve increased robustness, compactness and efficiency in the

EV's power system. The proposed MPC uses bi- and uni-directional switches to integrate clusters of energy storage and sources respectively for automotive applications. It also utilizes few passive components, by requiring only one

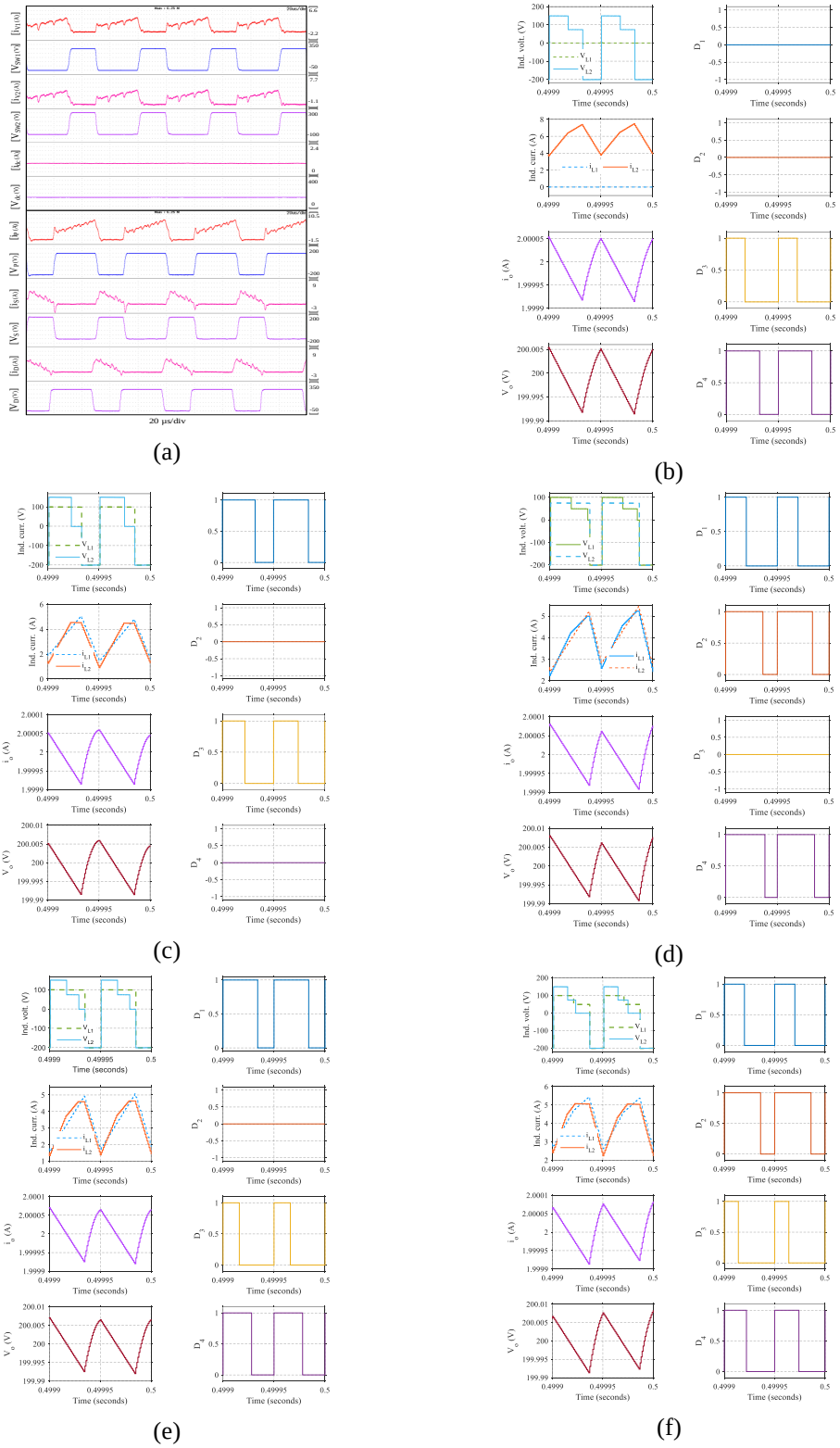

Fig. 6. Closed loop verification results of the MPC operation when the dc link is supplied form (a)V_1 and V_2 (b) V_3 and V_4 (c) V_1 and V_3, (d) V_1, V_2 and V_4, (e) V_1, V_3 and V_4 and (f) All four inputs.

inductor per cluster and one capacitor for any number inputs. The proposed MPC is also capable of exclusive power transfer from the RES to the ESS clusters. It has been analysed for four inputs (two inputs per cluster) under independent and simultaneous power flow from the inputs to the dc link. The proposed MPC was numerically verified and validated in open and closed loop operations on OPAL-RT's OP5700, an FPGA based HIL platform. The applicability of this MPC is not limited to multiple energy source and storage hybridization in automotive applications but can also be adapted for hybrid energy systems in other applications such as dc microgrids.

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Paper VIII:

Novel Isolated Multiport DC Converter with Natural Bipolar Symmetry for Renewable Energy Source Integration to DC Grids

This paper has been submitted as:

I. N. Jiya, H. Van Khang, P. Gunawardena, N. Kishor and Y. Li, "Novel Isolated Multiport DC Converter with Natural Bipolar Symmetry for Renewable Energy Source Integration to DC Grids," in *IEEE Access*, (*Submitted*).

Novel Isolated Multiport DC Converter with Natural Bipolar Symmetry for Renewable Energy Source Integration to DC Grids

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***Abstract*— Due to their greater reliability, efficiency, and resilience as compared to unipolar dc grid systems, bipolar dc grid systems are swiftly gaining popularity for the integration of renewable energy sources. However, development of multiport converters for bipolar microgrid systems is still progressing slowly in terms of reducing costs or improving power density and compact designs. This paper proposes a multiport isolated dc-dc converter with naturally symmetric bipolar outputs (MIBDC). With respect to the number of input ports, voltage gain, and output symmetry that the proposed converter naturally possesses, it outperforms its few competitors. Additionally, the proposed MIBDC significantly reduces component count and control complexity by employing a fixed transformer with only one primary and secondary winding for any number of inputs. The suggested converter's performance in both open and closed loops is evaluated quantitatively in simulation and experimentally using OPAL-OP5700 RT's hardware-in-the-loop (HIL) platform under various situations.**

Index Terms— buck-boost, bipolar dc bus, bipolar outputs, dc-dc converter, isolated converter, hardware-in-the-loop, multiple input converter, multi-source converter, renewable energy sources.

I. INTRODUCTION

The hunt for green alternatives has gained traction in recent years due to the impending exhaustion of fossil fuels and the damaging environmental effects of using them to meet rising energy demands. [1]. It has been demonstrated that fuel cells, wind, and photovoltaic (PV) systems are appropriate alternatives to offer the urgently required green solutions [2]. The rising use of these renewable energy

sources (RESs) has caused a paradigm change in the production and use of electrical energy, moving it from centralized to distributed generating systems [3], many of which are often based on dc microgrids. The three-wire dc bus grid technology known as bipolar dc grids (BDCG) is gradually gaining acceptance as a method to enhance dc microgrids. This quick adoption is a result of BDCGs' greater efficiency, as they use less current to transport the same amount of electricity than unipolar dc grids (UDCGs) do. Additionally, BDCGs are more dependable than UDCGs because even if one of the poles fails, the remaining pole may still transfer electricity, although at a reduced capacity. Further, converting from dc to ac voltage with multilevel inverters (MLIs) is simpler and more reliable with BDCGs than with UDCGs. This is because BDCGs have three voltage levels ($\pm\frac{V_o}{2}$ and V_o) and UDCGs have only one level. Due to these desirable characteristics of BDCGs, RESs and dc loads may now be more effortlessly integrated utilizing dc-dc converters [4]. However, because the voltage of the multiple sources and loads differs significantly, many single-input single-output (SISO) dc-dc converters are needed to step-up or step-down the voltage to or from the BDCG system. Due to global shortages of semiconductor chips, several components, particularly semiconductors, are therefore needed in addition to bulky and complicated setups and high costs [5].

Consequently, a solution to the aforementioned issues with SISO dc-dc converters has been proposed: multiport dc-dc converters (MPCs), which are often developed from traditional SISO converters [6–9]. There are numerous MPCs with and without galvanic isolation that have been proposed as a result of extensive research into MPCs. Isolated MPCs provide substantial advantages over non-isolated MPCs in terms of soft switching capability, high gain, and safety thanks to the magnetic isolation of input and output provided by the magnetic components. In [6, 7], MPCs with multiple-inputs and single-outputs (MISO) based on half-bridge, full-bridge (FB), dual active bridge (DAB) and multi active bridge (MAB) converters, have been proposed. However, a common limitation of these converters is the use of multiple windings for the inputs of transformers or coupled inductors based on flux additivity. As a result, the size and control complexity rise and the power density decreases. Numerous clamping circuits may be necessary due to the need for multiple windings on the primary side of the magnetics for each input source, which would increase component count and perhaps control complexity if an active clamping is being used. The authors in [8, 9] suggest isolated MPCs with

just two windings, a primary winding and a secondary winding, to allay these issues. Given that they all have a single output port, they are all inadequate for BDCG
systems. In order to address this, MPCs with multiple inputs and outputs (MIMO) have been proposed in [10, 11]. However, these MIMO MPCs are afflicted by cross-regulation of the voltage at the output ports, necessitating the use of sophisticated controllers. Due to this issue, bipolar dc-dc converters (BDCs) were developed. These converters normally only have two symmetrical outputs, one for each pole (positive and negative, respectively). To that end, BDCs have been proposed in [12–16], but as they are all single input converters, they share the same problems as SISO converters, which have been described previously. Multiport bipolar dc converters (MBDCs) have recently been suggested in [17–20] as a solution to this problem. The non-isolated MBDCs in [17, 18] have low gain, poor power density, and only two inputs to the MPC; as a result, they cannot be expanded to include an arbitrary number of inputs, which is one of the main characteristics of MPCs. Due to the lack of magnetic separation, they also pose a safety risk. Even though the multiport isolated bipolar dc converters (MIBDCs) in [19, 20] are the only MIBDCs that have been suggested in the literature thus far, in certain circumstances, their feature soft switching in some cases is just like their non-isolated counterparts in [17, 18]. Despite the need for sophisticated control to maintain balanced symmetric output voltages, none of them can support arbitrary independent power flow from either of the input sources to the bipolar dc bus. Further, they both have a finite number of inputs and low voltage gains. To address these drawbacks, novel MIBDCs are necessary. Moreover, there have been less isolated MPCs with bipolar naturally symmetric outputs proposed in literature than there have been for their unipolar equivalents. Further, the implementation of maximum power point tracking (MPPT) in MPCs for the integration of multiple RESs continues to pose a challenge. This is evidenced in [21–23], in which MPPT is implemented for only one input source or in a rather complex way, where one controller is required for each input.

The MIBDC developed in this article solves the limitations of prior topologies by adopting a DAB-based and FB-based topology with a fixed two winding (one primary and secondary winding each) transformer and several ports built utilizing pulsing voltage sources. A single inductor is time multiplexed to provide any arbitrary independent and concurrent power transmission from numerous sources

while the component count is maintained to a minimum. The proposed MIBDC is unique in the following ways:

1) Regardless of the number of input sources, only one primary and secondary winding is required.
2) It can transmit power from the inputs to the dc bus independently and concurrently.
3) With bipolar output voltages and high gain, it can perform unidirectional buck and boost operations.
4) When additional input is introduced, a reverse blocking switch can be added to raise the number of inputs at will.
5) The symmetrical nature of the bipolar output voltages is intrinsic.
6) The converter simply needs a single input single output (SISO) controller, such as the common double loop PI controller, and has a very simple control framework.
7) In addition, a distributed MPPT (DMPPT) approach is suggested to lessen complexity and make it possible to use a single MPP controller for any number of inputs.

Within this framework, the new MBDC was analyzed for two input sources with equal and different input voltage levels, put through extensive simulations, and experimentally verified. The initial idea of the MIBDC proposed in this work has been presented in [24]. In this paper, the detailed analysis and features are numerically verified and results from experimental validation using the HIL test rig is presented. HIL verification has been proved to accurately and sufficiently prove the operation of power converters [25] and as such is implemented in the verification of the proposed MIBDC.

II. PROPOSED MIBDC TOPOLOGY

The proposed multiport isolated dc-dc converters with bipolar symmetric outputs are shown in Fig. 1. These MIBDCs are constructed by combining a conventional DAB or a phase-shifted full bridge (PS-FB) converter with a secondary side center tapped transformer to produce outputs with bipolar symmetry. To regulate the output voltage and make it easier to include inputs of different voltage levels, the numerous inputs are achieved using pulsing voltage sources and a time multiplexed inductor charging technique. The converter in Fig. 1 (b) is proposed as a way to simplify the control of the DAB section in Fig. 1 (a) by swapping out the secondary active bridge in Fig. 1 (a) with a diode H-bridge in Fig. 1 (b). As a result, it is

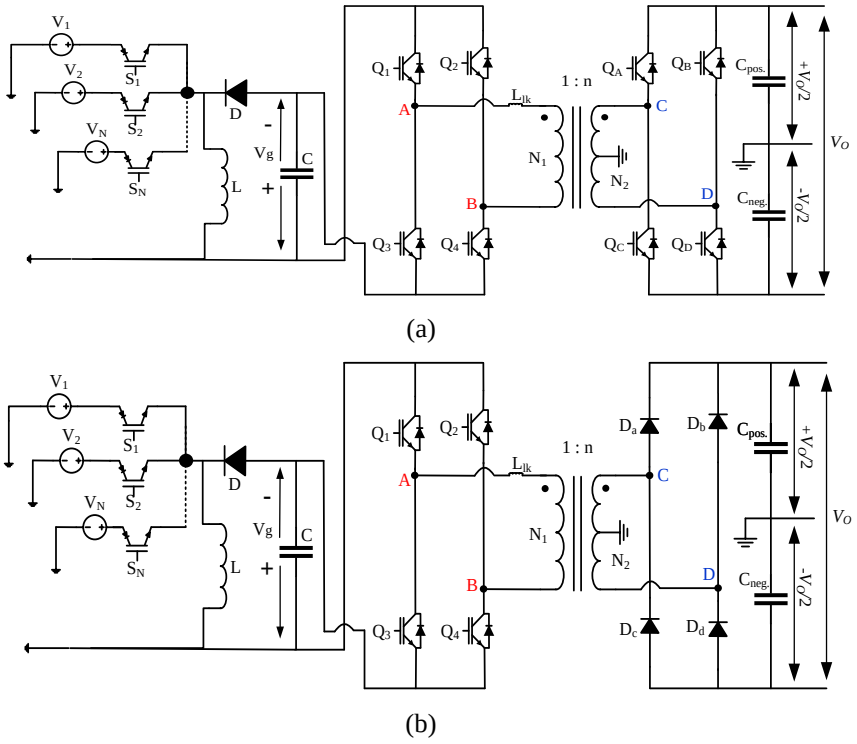

Fig. 1. Proposed (a) dual-active-bridge and (b) full-bridge -based bipolar multiport dc-dc converter.

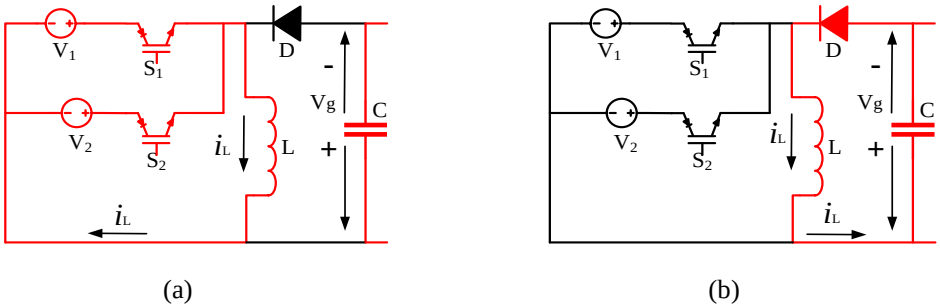

Fig. 2. Path of current flow in in the multiport section during (a) charging and (b) discharging of *L*, for simultaneous power flow with two inputs.

similar to a standard PS-FB converter with the addition of secondary side center tapping of the isolation transformer to enable bipolar outputs. Both topologies in Fig. 1 have the same multi-input power processing mechanism, involving reverse blocking switches S_1 to S_N, one diode, capacitor, and inductor, respectively. Reverse blocking switches are used to make it easier to integrate several sources with different voltage levels while maintaining independent and simultaneous power flow from the sources. Additionally, the converters may supply $\pm V_o/2$ and V_o on the dc lines at three different voltage levels. Since the key operating principles described are essentially transferable from the PS-FB to the DAB based MIBDC, the MIBDC proposed in Fig. 1 (b) will be analyzed for two inputs under independent and simultaneous energy transfer configurations for the steady state continuous conduction mode (CCM) analysis in this paper.

A. Independent Power Flow in Steady State CCM

In the case of two-inputs to the proposed MIBDC, power can flow from either of the inputs (V_1 or V_2) to the bipolar dc bus in the independent power flow mode of the proposed MIBDC. In order to charge the inductor, L, for a duration of DT_S, where D is the duty cycle and TS is the total switching period, the corresponding switch controlling each input source, S_1 for V_1 or S_2 for V_2, is switched ON. Diode, D, conducts in the direction shown in Fig. 2 (b) to discharge L during $(1\text{-}D)T_S$, the switch's OFF period. Resultantly, the multiport portion functions like a typical inverting buck-boost converter, and capacitor C has a voltage that matches the description in (1). The PS-FB part and the multiport section both function simultaneously when the multiport section is active, as shown in Fig. 3. The MIBDC's isolation transformer section is run in a fashion that causes zero voltage switching on the active switches Q_1 through Q_4 (ZVS). A thorough explanation of the ZVS function is presented in [26]. The steady state waveform in Fig. 3 displays the pulse signal for these switches. To account for the phase shift ($\emptyset$) and the deadtime necessary to accomplish ZVS, the total switching period for Q_1 through Q_4 is divided into 10, (t_0 to t_{10}). The connection between the input voltage and the dc link is represented by (2), where n is the turn ratio (N_S/N_P) of the transformer, during steady state CCM operation.

$$V_g = (V_{in}D)/(1-D) \tag{1}$$

$$V_o = \left[(V_{in}D)/(1-D)\right]2\phi n = 2V_g\phi n \tag{2}$$

B. Independent Power Flow in Steady State CCM

The converter shifts to simultaneous power flow mode when energy from more than one input has to be transferred to the dc link, as shown in Fig. 2 for two inputs. The switches S_1 to S_N that control all the sources are turned ON simultaneously but are thereafter switched OFF in the sequence of the various voltages' descending magnitudes. As a result, the charging of L is time multiplexed, as shown in Fig. 3, permitting the simultaneous transfer of power from two inputs.

According to Fig. 3, the charging and discharging durations of L make up the two main segments of the switching period in steady state CCM. The second component stays set as $(1 - \sum_{i=1}^{N} D_{ieff})$, showing the discharging time of L. The first part is further split based on the number of inputs of the MIBDC operating simultaneously: two divisions (D_{1eff} and D_{2eff}) in this case, since the MIBDC is being analyzed for two inputs. The current flows from the source with the highest

potential first when the switches are turned ON, which is V_1 in this case. As a result, L is charged with a slope of V_1/L during D_{1eff}. After D_{1eff}, V_2 assumes control and starts charging L with a slope of V_2/L during D_{2eff}. With a slope of V_N/L for any number of inputs, this goes on until D_{Neff}. At the conclusion of the charging period, L is discharged with a slope of $-V_g/L$. Additionally, the PS-FB part is functioning concurrently with the multiport section, as shown in Fig. 3. Through implementing volt-second equilibrium to the resultant steady state CCM waveform in Fig. 3, capacitor C's voltage is described by (3) and the input-output voltage is specified by (4).

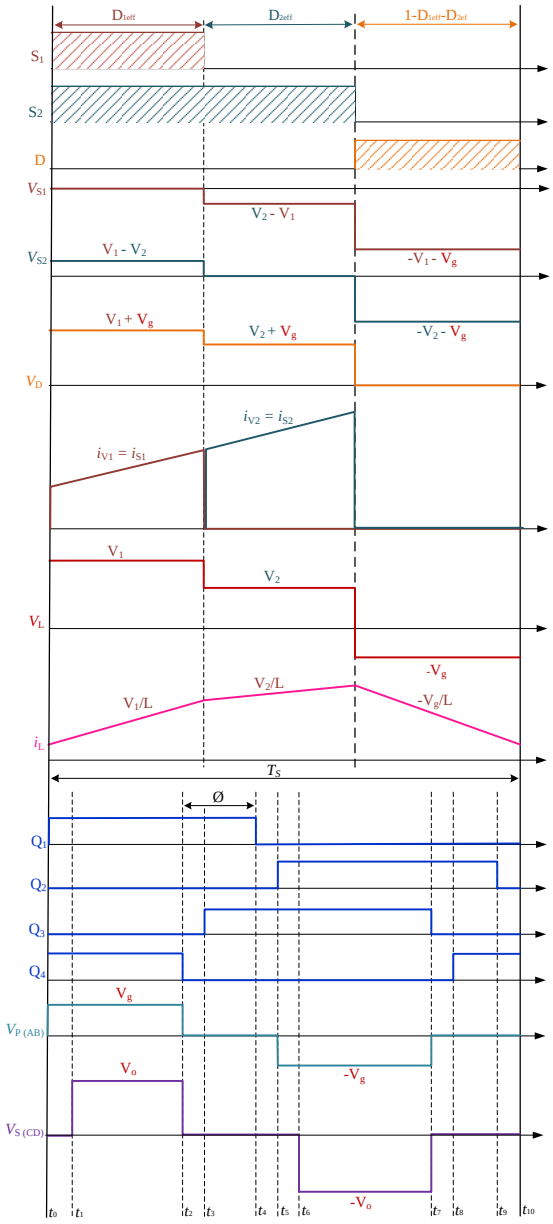

Fig. 3. Steady state key waveforms of the phase-shifted full-bridge based multiport bipolar dc-dc converter.

$$V_g = \left[\left(1-\sum_{i=1}^{N} D_{ieff}\right) \Big/ \left(1-\sum_{i=1}^{N} D_{ieff}\right)\right] \tag{3}$$

$$V_o = \left[\left(\sum_{i=1}^{N} V_i D_{ieff}\right) \Big/ \left(1-\sum_{i=1}^{N} D_{ieff}\right)\right] 2\phi n = 2V_g \phi n \tag{4}$$

To accomplish simultaneous power transmission to the load, certain criteria must be adhered to for the switches to commutate effectively in multi-input mode. When the voltages are not identical, the sources' magnitudes are randomly placed in decreasing order so that $V_1 > V_2 > \cdots > V_N$. Further, it is required that the duty cycles of the PWM signals used to regulate the input source switches, e.g. S_1 and S_2, be such that $D_1 < D_2 < \cdots < D_N$, and vice versa, where $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}$, ..., $D_N = D_{1eff} + D_{2eff} + \cdots + D_{Neff}$. To obtain equal power supply from the sources, the duty cycles of the PWM signals must be set so that $D_1 = D_2 = \cdots = D_N$ if the source voltages are equal, such that $V_1 = V_2 = \cdots = V_N$. In the event that the sources' necessary power delivery is not equal, the magnitudes of $D_1, D_2, \ldots, D_N$ can be computed in the sequence of the required power delivery from each source.

C. Voltage Gain

When compared to the single input forms from which they are developed, the voltage gain of multiport converters is somewhat different [27]. Therefore, voltage transformation factor (V_{TR}) is the ideal way to describe multiport converter gai. VTR is expressed as in the case of the proposed converters (5). At an effective duty cycle (D_{ieff}) of 90%, the proposed converter may produce a high gain of up to 20$\emptyset n$. Thus, if a bigger gain is necessary, the phase shift ($\emptyset$) and turns ratio (n) can be employed to further improve the converter gain.

$$V_{TR} = V_o \Big/ \left(\sum_{i=1}^{N} V_i D_{ieff}\right) = (2\phi n) \Big/ \left(1-\sum_{i=1}^{N} D_{ieff}\right) \tag{5}$$

D. Control Structure

Fig. 4 shows the control structure of the proposed MIBDC. The control layer consists of the secondary controller (with the DMPPT controller), the double loop PI controller, the power management controller (PMC), phase shift (PS) controller and the respective pulse width modulators (PWM). The secondary controller sets the output voltage reference ($V_{g\text{-}ref}$) of the multiport section, depending on the required operating mode of the MBDC and the MPP of input sources. The MPP

controller is also responsible for the proportion of power flow from the sources when operating in a simultaneous power flow mode. To do this, the MPP controller determines scaling factors k_1 to k_{N-1}, which are obtained by implementing an DMPPT algorithm for sources (V_1 to V_{N-1}). Fig. 5 shows the flowchart of DMPPT, in which the classic perturb and observe (P&O) algorithm is implemented. The output of the DMPPT P&O algorithm is k_1 to k_{N-1}. V_O and i_L are used to determine the control variable β, which is the time required to charge the inductor(s). The PI gains of the double loop PI controllers are selected heuristically. The PMC based

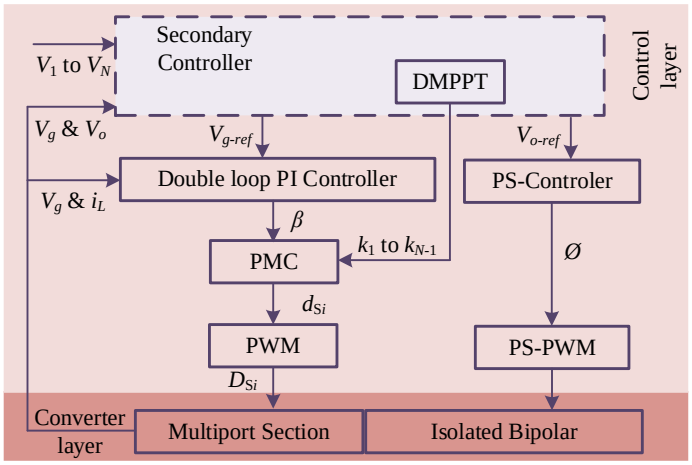

Fig. 4. Control structure of the proposed MIBDC.

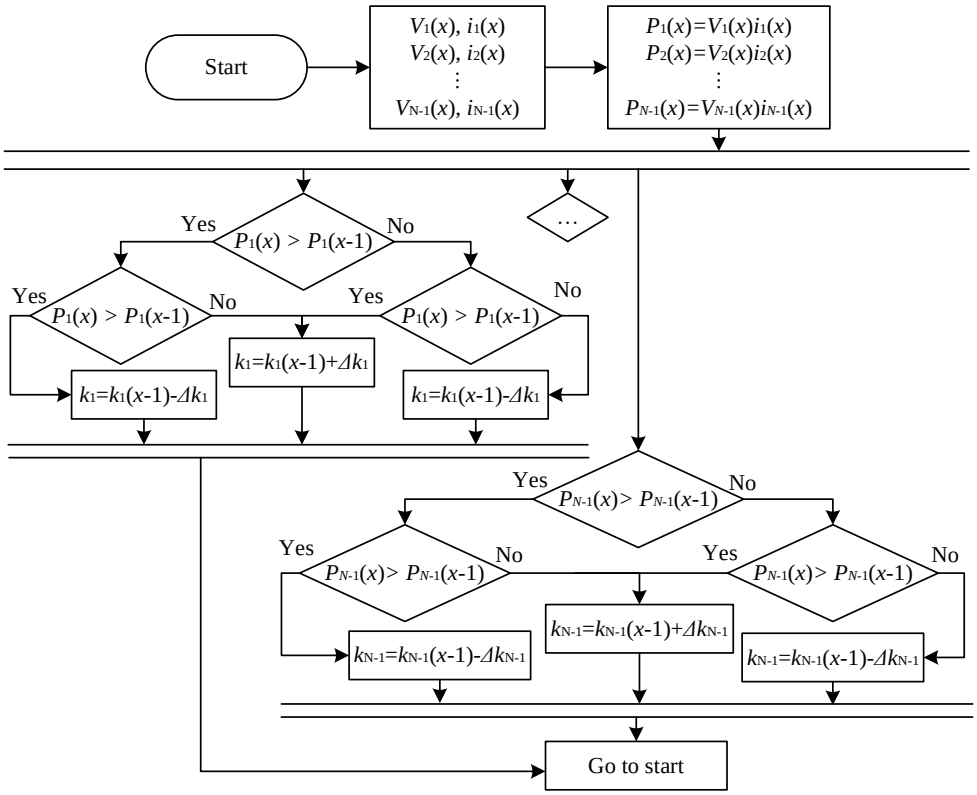

Fig. 5. Flowchart of DMPPT controller of the proposed MIBDC.

on the scaling instructions (k_1 to k_{N-1}.) from the DMPPT controller determines $D_{1eff} - D_{Neff}$ and the respective duty cycles according to (6). Further, the PS-controller provides the required phase shift (Ø) required to keep the output voltage of the isolated bipolar section constant based on the target output voltage ($V_{o\text{-}ref}$).

$$\left.\begin{aligned} D_{1eff} &= k_1\beta \\ &\vdots \\ D_{N-1eff} &= k_{N-1}\beta \\ D_{Neff} &= \beta - \sum_{i=1}^{N-1} D_{ieff} \end{aligned}\right\} \quad , \quad \left.\begin{aligned} d_1 &= D_{1eff} \\ d_2 &= D_{1eff} + D_{2eff} \\ &\vdots \\ d_{N-1} &= \sum_{i=2}^{N-1} D_{ieff} \\ d_N &= \sum_{i=1}^{N} D_{ieff} \end{aligned}\right\} \tag{6}$$

E. Fault Tolerant Operation for Critical Loads

One key advantage of bipolar dc power systems over the unipolar counterparts is the increased reliability of power supply for critical load units. This is demonstrated by the ability to continue to supply power to the critical load unit in the event of a failure or open circuit fault in any of the lines of the bipolar system. Fig. 6 presents the schematic of a bipolar to unipolar dc-dc converter required to achieve this. The bipolar to unipolar dc-dc converter is essentially a cascade of two synchronous buck converters and its operation is similarly so. The switching

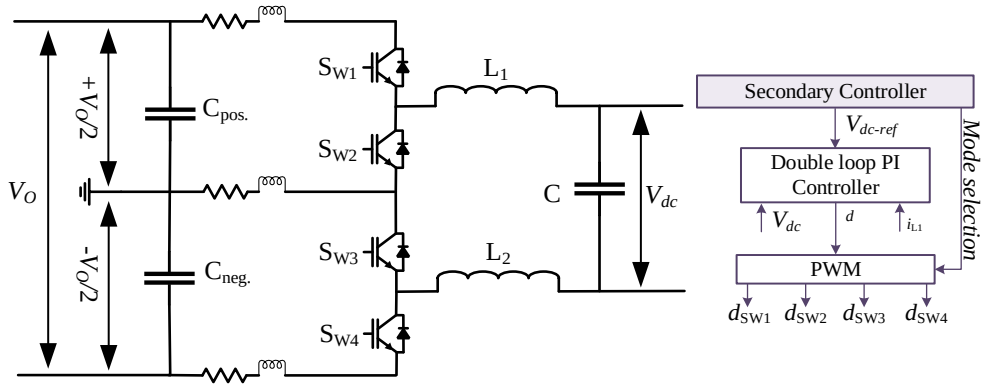

Fig. 6. Schematic of bipolar to unipolar dc-dc converter for critical loads.

TABLE I
CONDUCTION OF DEVICES IN THE BIPOLAR TO UNIPOLAR DC-DC CONVERTER FOR CRITICAL LOADS

State	T_1	T_2
Healthy state	S_{W1} S_{W4}	D_{W2} D_{W3}
Failure in positive line	S_{W4}	D_{W2} D_{W3}
Failure in negative line	S_{W1}	D_{W2} D_{W3}
Failure in neutral line	S_{W1} S_{W4}	D_{W2} D_{W3}

pattern of the converter is presented in Table I for the healthy state and fault states. The input-output voltage relationship of the converter is described by (7), which is basically the same as a traditional buck converter's. The input voltage (V_{in}) in this case depends on the state of the bipolar dc, under healthy state and failure in the neutral line, V_{in} is equivalent to V_o while it is equivalent to $V_o/2$ in the other two fault states.

$$V_{dc} = V_{in} D \tag{7}$$

III. RESULTS

Utilizing the OPAL-RT OP5700 device, which runs a 64-bit Virtex-7 FPGA, the proposed isolated MIBDC is quantitatively verified in simulation and validated experimentally. Fig. 7 depicts the configuration for the laboratory experimental validation. Table II provides the parameter values for each component. In both closed and open loop operations, the topology of the MIBDC was evaluated. Five scenarios involving open loop operation were run, the first two of which represented independent power flows from the two sources (V_1 and V_2) to the dc link, respectively. The MIBDC is operated in both simultaneous power flows from

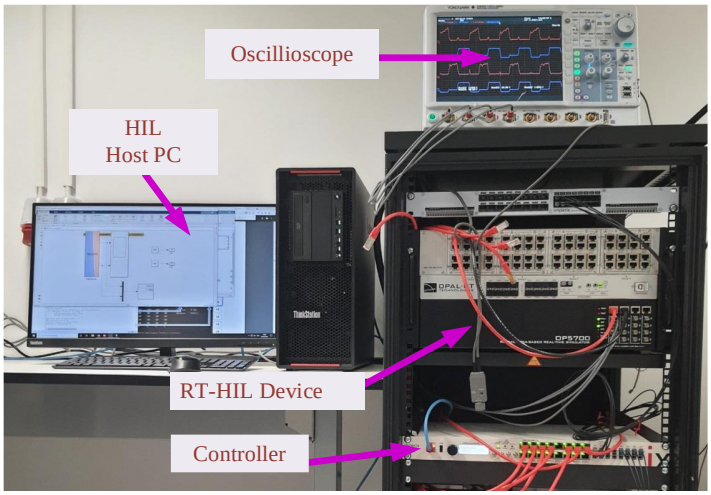

Fig. 7. In-house HIL platform used for validating the MIC.

TABLE II
PARAMETERS USED IN VERIFICATION

Parameter	Value	Unit
Inductor (L)	1	mH
Capacitors (C=$C_{pos.}$=$C_{neg.}$)	4.7	µF
Voltage sources (V_1/V_2)	100/75	V
Transformer turns ratio (n)	2	
Phase shift ($Ø$)	27	degrees
Switching frequency (Fsw)	20	kHz

both sources with equal and uneven voltage levels in the remaining three open loop situations. Finally, the converter was run in a closed loop to test the bipolar outputs' capacity to naturally maintain symmetry.

A. Open Loop Verification of Single Input Operation.

The open loop verification of running the MIBDC with the first voltage source, V_1, and the second voltage source, V_2, providing the bipolar dc link separately is shown in Figs. 8 and 9, respectively. For both scenarios, V_1 is set to 100 V, V_2 is 75 V and the results presented include inductor current (i_L) and voltage (V_L), primary (V_P) and secondary (V_S) turns voltage of the transformer, input currents, voltages

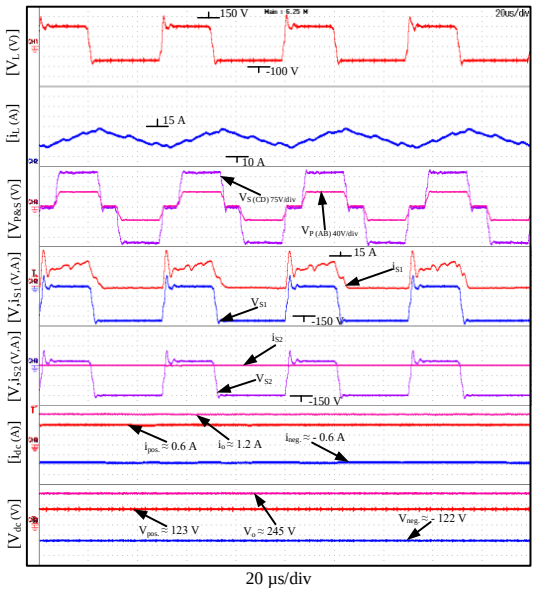

Fig. 8. Results when only V_1 is supplying the dc bus where V_1=100V, V_2=75V, D_1=0.4 and D_2=0.

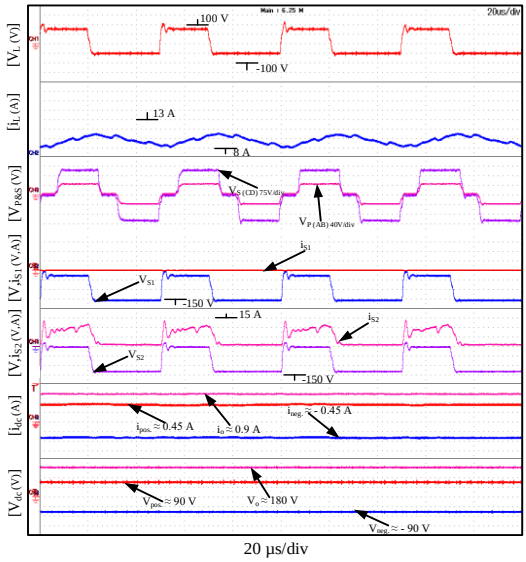

Fig. 9. Results when only V_2 is supplying the dc bus where V_1=100V, V_2=75V, D_1=0 and D_2=0.4.

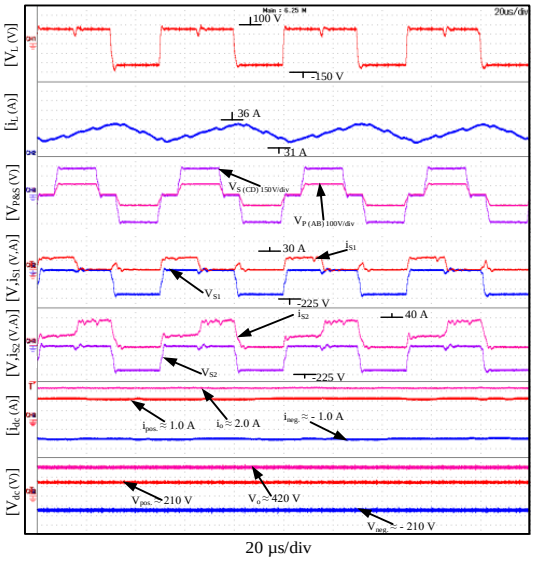

Fig. 10. Results when both sources are supplying the dc bus where V_1=V_2=75V, D_1=0.3 and D_2=0.6.

of S_1 (i_{S1}, V_{S1}), S_2 (i_{S2}, V_{S2}), the dc link (i_{dc} and V_{dc}), and the voltage across the switches of the PS-FB section, $V_{Q1} - V_{Q4}$ and $V_{Da} - V_{Dd}$. The result of V_1 alone delivering power to the dc link is shown in Fig. 8. To do this, S_1's switch duty cycle, D_1, which controls the first voltage source, V_1, is set to 0.4, while S_2's duty cycle, D_2, is set to 0. There was a 200 Ω load over each pole and the full dc link. The results shown in Fig. 8 match numerical solutions with $\pm V_o/2$ and V_o at about ±123 V and 245 V, respectively, and $\pm i_o/2$ and i_o at about ±0.6 A and 1.2 A. In Fig. 9, the results of independent power flow from V_2 are presented. D_1, the duty cycle of S1 was set to 0, while that of S_2, D_2 was set to 0.4. The load across each of the voltage levels was also 200 Ω each. Again, the results in Fig. 9 show good agreement with numerical solutions In Fig. 9, the independent power flow results from V_2 are shown. D_1, S_1's duty cycle was set to 0, and S_2's duty cycle was set to 0.4. The load was 200 Ω across each voltage level as well. Once more, the results in Fig. 9 exhibit strong congruence with numerical results such that $\pm V_o/2$ and V_o being about ±90 V and 180 V respectively and $\pm i_o/2$ and i_o at about ±0.45 A and 0.9 A respectively.

B. Open Loop Verification of Simultaneous Operation.

The outcomes of the final three open loop operating scenarios—i.e., the simultaneous transmission of power from the two inputs to the bipolar dc link—are shown in Figs. 10 through 12. Since Figs. 10 and 11 have the same effective

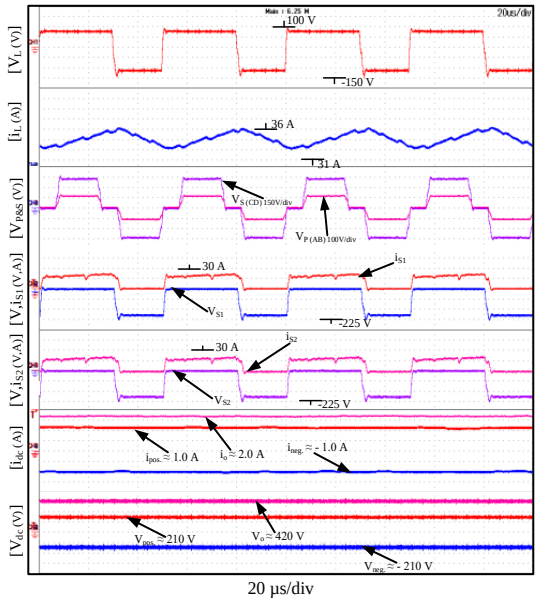

Fig. 11. Results when both sources are supplying the dc bus where V_1=V_2=75V and D_1=D_2=0.6.

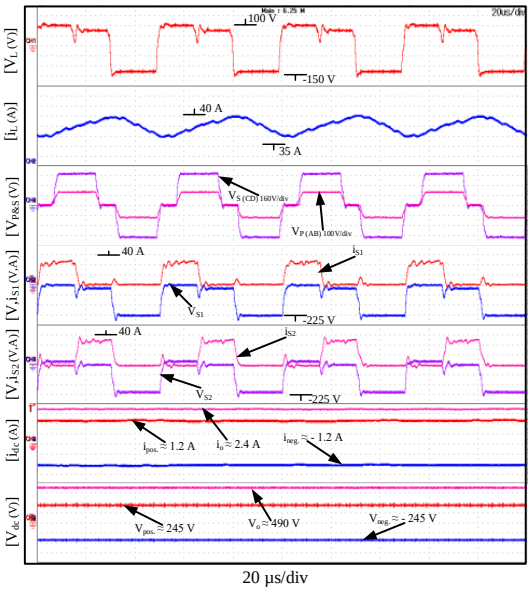

Fig. 12. Results when both sources are supplying the dc bus where V_1=100V, V_2=75V, D_1=0.3 and D_2=0.6.

duty, $\sum_{i=1}^{N} D_{ieff}$, of 0.6 and equal input voltages with V_1=V_2=75 V, their output characteristics are the same. As a consequence, both of the results in Figs. 10 and 11 are in agreement with the numerical solutions with $\pm i_o/2$ and i_o being about ±1.0 A and 2.0 A respectively and $\pm V_o/2$ and V_o at about ±210 V and 420 V, respectively. The main difference with both scenarios is that D_1 was set to 0.3 and D_2 to 0.6 in Fig. 10 such that D_{1eff}=0.3 and D_{2eff}=0.6, so since both voltages are equal, while S_1 is ON, S_2 is also ON and both sources are charging the inductor, *L*, and then when D_1 goes OFF, only D_2 is charging *L*. Thus, the average i_{S2} is larger than from i_{S1}, while in Fig. 11, D_1=D_2=0.6 and so since they have equal voltages, both sources are charging the inductor with currents i_{S1}=i_{S2} during the inductor charging. This demonstrates how the duty cycle is employed to regulate the amount of energy supplied by the various sources. When the voltages are changed in the fifth scenario of Fig. 12 so that V_1 = 100 V and V_2 = 75 V, it is necessary to time multiplex the inductor charging. This is as mentioned previously in section II B in order to send power from both sources to the load simultaneously. In this case, D_1 was set to 0.3 and D_2 to 0.6 such that D_{1eff}=D_{2eff}=0.3. Typically, Fig. 12's performance is in line with numerical solutions with $\pm V_o/2$ and V_o being ±245 V and 490 V, respectively, and the dc link currents at $\pm i_o/2$ and i_o being ±1.2 A and 2.4 A, respectively.

C. Closed Loop Verifications of the MIBDC.

Additionally, in order to operate the MIBDC as previously explained and produce a constant output voltage of $\pm V_o/2$ and V_o of ±100 V and 200 V respectively and later stepped to ±125 V and 250 V respectively. In Fig. 13, some of the closed loop dynamics are shown. To more thoroughly analyze the MIBDC's inherent symmetry properties, the load on the three voltage levels was arbitrarily adjusted. The control target was V_o while the positive and negative poles were left uncontrolled to freely balance the voltage across themself. The load on V_o was doubled from about 1 A to 2 A at 8s and V_o experiences a dip of less than 3 V after that the controller can bring it back to the target 200 V. And then the load on the positive pole was also doubled from 0.5 A to 1 A at 12s and the negative pole's load also doubled from 0.5 A to 1 A at 16s. A voltage sag of less than 1 V was seen on V_o during the load transition for both the positive and negative poles of the MIBDC, but generally, the load changes do not result in an imbalance in the output voltages, which is evidence of the converter's inherent symmetry. A further testament of the MIBDCs' controller is demonstrated in the startup dynamics,

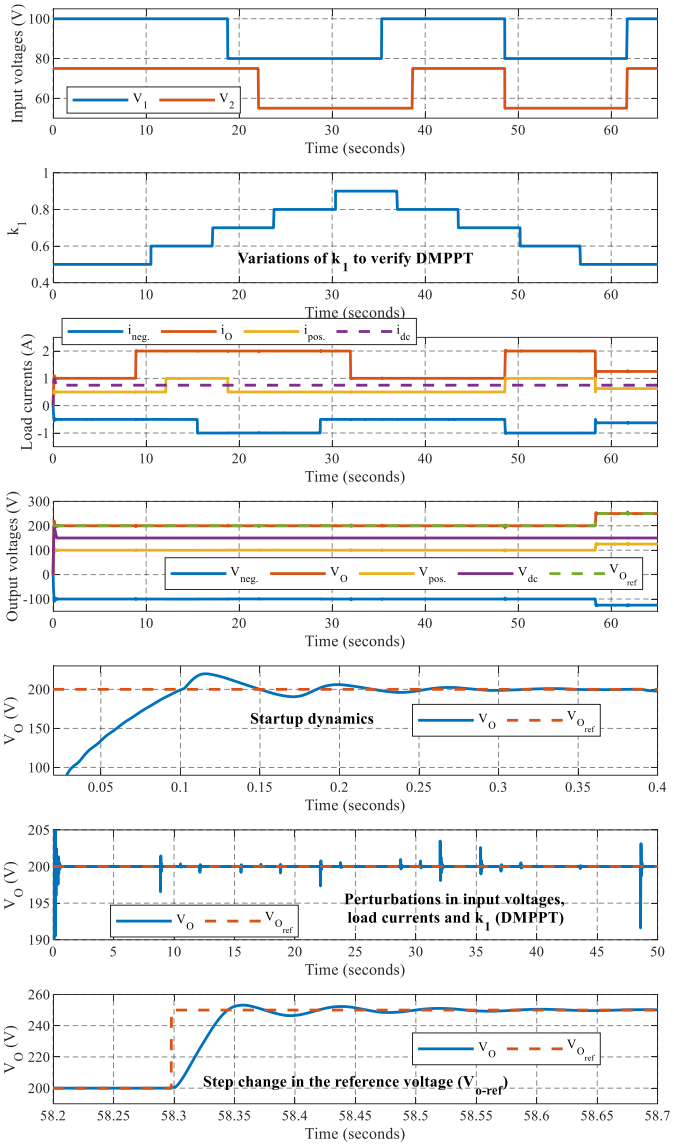

Fig. 13. Closed loop performance of the MIBDC under perturbations in the input voltages, load currents and output reference voltage.

where minimal overshoot is observed with a rise time, time constant and settling time of 75ms, 25ms, and 0.25s respectively. Also, a fast response to step change of 50ms is also observed at 58s. Furthermore, the value of k_1 is varied to demonstrate the ability of the MIBDC to use the MPPT to control the power delivered from the input sources without affecting the output voltages. Furthermore, all these perturbations do not impact the voltage (V_{dc}) or current (i_{dc}) of the critical load. Further, the converter operation under different mode transition is verified with results in Fig. 14. The first column presents transitions in the input voltages (V_1 and V_2) from equal (80 V) to unequal (100 V & 75 V) and back to equal (80 V) voltages. The second and third column represent transitions from V_2 alone supplying the dc link to simultaneous power flow to V_1 alone supplying the

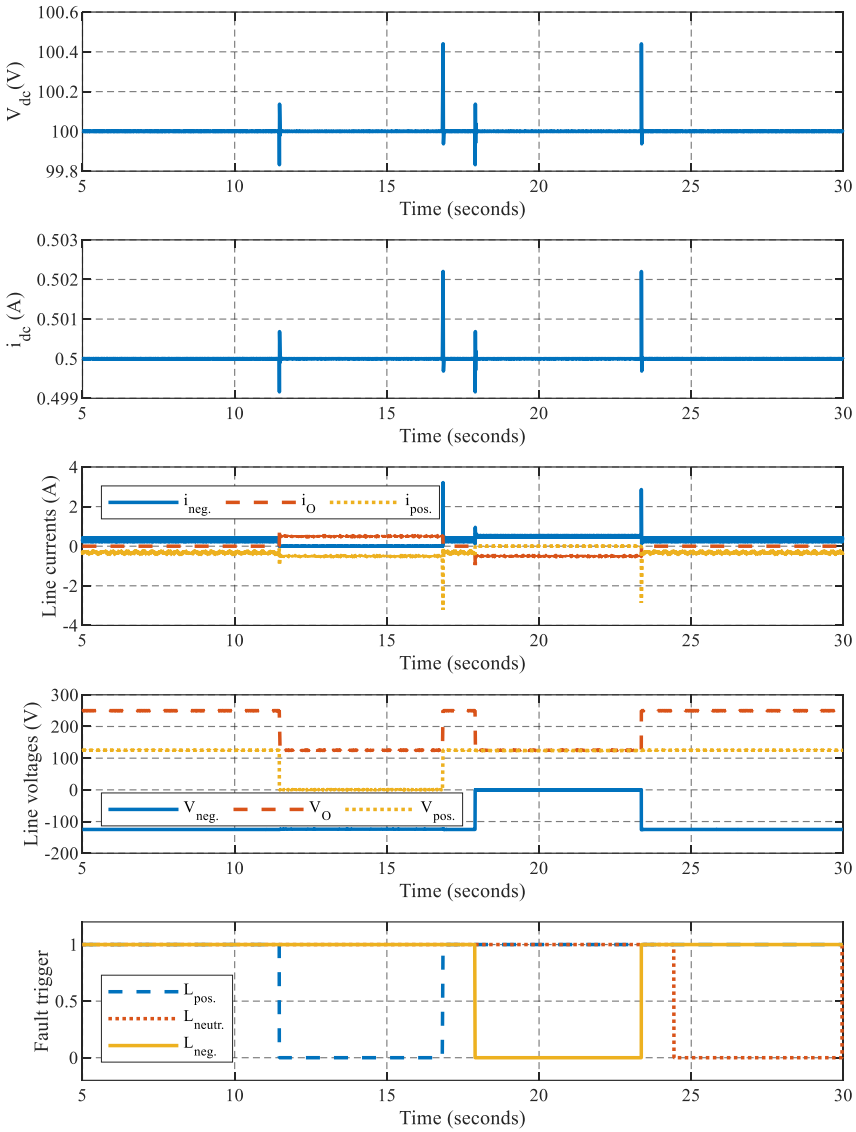

Fig. 15. Closed loop performance of the bipolar to unipolar converter under line failures.

dc link under equal and unequal voltages respectively in the second and third column. Under all these mode transitions the controller can maintain the output voltages at the target of 200 V and ±100 V. Lastly, in Fig. 15, the operation of the bipolar to unipolar converter is verified. Open circuit faults [28] are introduced sequentially in the positive, negative, and neutral lines respectively. Under these faults, the converter can continue to deliver power to the critical load with no significant impact on the quality of the voltage (V_{dc}) or current (i_{dc}) of the critical load.

D. Closed Loop Verifications of the MIBDC.

The power losses (P_L) in MIBDC can be estimated using (10), consisting of the inductor and transformer winding (P_W) and core (P_C) losses [32], capacitor losses

(P_{Cap}), MOSFET switching (P_{swMOS}) and conduction (P_{onMOS}) losses [33], and the losses in the diode (P_D). Where T_S is the switching period, R_{ESRL} is the inductor's equivalent series resistance (ESR), $\hat{i}_L$ is the inductor average current, Δi_L is the inductor ripple current, $K, \beta \& \alpha$ are Steinmetz parameters, R_{ESRC} is the capacitor ESR, V_{DS} is the MOSFET drain to source voltage, i_{DS} is the MOSFET drain to source current, t_{on} & t_{off} is the MOSFET ON and OFF time, R_{DSon} is the MOSFET on state resistance, D is its respective duty cycle, V_F and i_F are the diodes' forward voltage and current respectively.

$$P_L \approx \left\{ \begin{array}{l} \underbrace{\frac{1}{T_S}\int_0^{T_S} R_{ESR}\left(i_L{}^2 + \frac{\Delta i_L{}^2}{12}\right)}_{P_W} + \underbrace{K\Delta i_L^{\beta} F_{SW}^{\alpha}}_{P_C} + \underbrace{R_{ESRC}\left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}_{P_{Cap}} \\ + \underbrace{\frac{1}{2} V_{DS} i_{DS} F_{SW}\left(t_{on} + t_{off}\right)}_{P_{swMOS}} + \underbrace{R_{DSon} i_{DS}^2 D}_{P_{onMOS}} + \underbrace{\frac{1}{T_S}\int_0^{T_S} V_F i_F^2}_{P_D} \end{array} \right\} \quad (10)$$

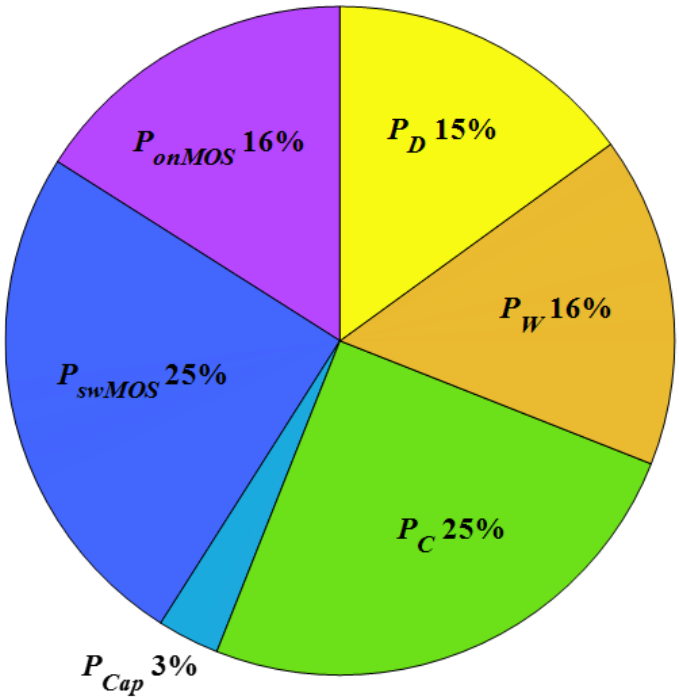

Fig. 16. Loss distribution in the proposed MIBDC.

Based on (10), the loss distribution in the proposed MIBDC is calculated and presented in Figure 16. P_W accounts for 16%, P_C is 25%, P_{swMOS} is 25%, P_{onMOS} is 16%, P_D is 15% and P_{Cap} is about 3%. The switches and magnetics account for more than 95% of the losses. Therefore, carefully selecting and designing the switches and magnetics are vital to maintaining a high efficiency in the proposed MIBDC.

IV. COMPARISON WITH RELATED BIPOLAR MULTIPORT CONVERTERS

TABLE III
COMPARISON OF THE PROPOSED FAMILY OF MIBDCS WITH EXISTING MIBDCS.

Parameters		Part Count						No. of inputs	IPF	SPF	Modulable?	Output voltage-symmetry	Soft switching
		S	D	L	C	Tx	T						
[19]		6	2	3	2	1	14	2	No	Yes	No	Asymmetrical	ZCS+ZVS
[20]		6	4	2	2	1*	15	2	No	Yes	No	Symmetrical	ZCS+ZVS
Proposed	DAB	N+8	0	1	3	1*	N+13	N	Yes	Yes	Yes	Symmetrical	ZCS+ZVS
	FB	N+4	4										

N=Number of inputs, IPF=Independent power flow, PFP=PF between ports, SPF=Simultaneous PF, S=Active switch, D=Diode, L=Inductor, C=Capacitor, Tx=Transformer, T= Total, *=IPF is only possible from the second input port, $^{+}$=PFP is only possible from the first to the second input port and not vice versa, Sw.= Switching.

Table III presents the comparison of the proposed MIBDC with the recently proposed MIBDCs in [19, 20]. The basis for selecting these MIBDCs for comparison is that, to our knowledge, they are the only existing MIBDCs in literature. Table III is arranged in the order of increasing part count, when considering two inputs to the MIBDCs. The proposed MIBDC in [19] has the lowest part count by just 1 but its' output voltage is not inherently symmetrical. And so, a further controller is required to maintain the voltage symmetry on the bipolar outputs. For two inputs, the MIBDCs proposed in this paper has the same part count and symmetrical characteristics as the MIBDC in [20]. But has a key advantage of modularity such that the number of input ports can be arbitrarily increased just by introducing one additional reverse blocking switch. Further, the MIBDCs proposed in [19, 20] both have a limitation on number of inputs and low voltage gain, areas in which the MIBDCs in this paper are triumphant. Finally, the independent power flow (IPF) can be carried out arbitrarily from any of the inputs of the proposed MIBDCs to the outputs, but the existing MIBDCs can achieve IPF from the second input alone.

V. CONCLUSION

Using dual active bridge and phase-shifted full bridge topologies, an unique unidirectional multiport isolated dc to dc converter with bipolar symmetric outputs has been proposed in this study. Analysis and verification of the proposed MIBDC have been performed for two inputs with equal and unequal input voltages at various duty cycles. It was demonstrated how the MIBDC performed during the independent and concurrent power transfer from the sources to the dc link in both open and closed loop. Additionally, two crucial characteristics of bipolar converters—reliability under critical unipolar loads and natural symmetry of the

dc link under unbalanced loads—were analysed and validated. The results presented in this paper show the experimental validation on the in-house hardware-in-the-loop (HIL) platform. The suggested MIBDC can be used for energy harvesting in PV farms, mini-wind farms, and other dc-voltage-based renewable energy systems.

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