New Multilevel Inverter Topology with Reduced Component Count

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***Abstract*—This paper introduces a new topology of modular multilevel inverters, being suitable in medium and high voltage applications. As compared to the existing circuits, the proposed topology has advantages of high 'levels/components' ratio, increasing the output voltage levels without increasing the voltage stress across the used switches, structure simplicity, isolation features, and modularity. These merits allow it to fit well in high-reliability medium-power applications, which require fast troubleshooting and maintenance flexibility. Operating principles of the proposed scheme are detailed in low frequency and pulse width modulation. Simulation and experimental results validate the effectiveness of the circuit under different modulation and load conditions. Further, a comparative study between the proposed topology and other existing multilevel topologies was conducted and summarized in this paper.**

Index Terms— Converter control, multilevel converters, pulse-width modulation, staircases modulation, voltage source inverters.

I. Introduction

Modular multilevel inverters (MMLIs) have got great attention in both academia and industry due to their advantages such as high modularity, dynamics, power quality, low total harmonic distortion (THD), and low *dv/dt*. Such merits make MMLIs more suitable for an efficient and reliable power converter in renewable energy (RE) than counterparts, i.e. two-level, Quasi-Z-Source and matrix converters [1, 2]. Neutral point diode clamped (NPDC), flying capacitors (FC), and cascades H-bridge (CHB) converters have been developed for years to increase voltage levels, but increasing the voltage levels results in a higher number of components, typically switching devices, electrolytic capacitors, power diodes, and DC power supplies. Further, control complexity, fault-detection difficulty, short lifetime, and low efficiency have been the main drawbacks in the existing solutions. Producing new high-power switching devices and developing new multilevel inverters (MLIs) have been solutions to overcome the mentioned demerits [3-5]. Several topologies for MLIs have been intensively developed and reported in literature [6-13]. However, the existing circuits face certain challenges such as high component count, using electrolytic capacitors, limited output voltage levels, and control complexity.

In this paper, a new topology for modular multi-level converters is proposed to reduce component count and control complexity. The proposed circuit can galvanically isolate the source and the load by using a transformer bank. Although

the proposed circuit can operate in both symmetrical or asymmetrical modes, an only symmetrical configuration is studied in this paper. The proposed topology is compared to transformer-based and existing similar multilevel topologies. The comparative study shows that the proposed converter can further reduce the required components for producing the same output voltage levels as compared to the counterpart. Performance of the proposed topology under different load conditions using low-frequency modulation (LFM) and pulse width modulation (PWM) is verified via simulations and experimentally validated.

II. THE PROPOSED MULTILEVEL TOPOLOGY

A. GENERALIZED CONFIGURATION

The proposed topology consists of two stages: the main stage and repeated one. A N-level configuration is depicted in Fig. 1. The main stage comprises two DC power supplies and eighteen power switching devices connected to a medium frequency transformer bank. The medium frequency transformer provides isolating and stepping-up features, increasing the applicability for the proposed circuit.

The main stage operates as a base platform for generating five voltage levels while the repeated stage works as a level-generator stage, which can be repeated to increase the output levels. The relationship between the output voltage level number N and the utilized components can be defined by using the proposed equations (1)-(3).

$$N_{\text{Total}} = 3.5N + 5.5 \tag{1}$$

$$N_{\text{DC}} = 1.5N - 5.5 \tag{2}$$

$$N_{\text{SW}} = 2N + 8 \tag{3}$$

where N_{Total}, N_{DC}, and N_{SW} are the total component count, DC power supplies count and switching device count, respectively. For example, if only five voltage levels are required, the total number of the components will be twenty-three (two DC power supplies, eighteen switching devices, and three medium frequency transformers).

B. FIVE-LEVEL CONFIGURATION

The scaled-down circuit described in Fig. 2 is considered as a study case in this paper. The circuit uses only the main stage without any repeated stages, producing five voltage levels across the pole terminals AA, or BB, or CC and nine levels across the load terminals.

III. MODULATION STRATEGIES FOR THE PROPOSED TOPOLOGY

Modulation techniques for multi-level converters are usually classified based on many aspects. One of these aspects is the frequency of the switching signals that are produced by the modulation techniques. The switching algorithms can be implemented by using low-frequency modulation (LFM) strategies, i.e. selective

harmonic elimination (SHE) and staircases modulation (SCM) or based on high-frequency modulation (HFM) strategies, e.g. level-shifted, phase-shifted pulse width modulation schemes. The proposed topology is modulated by LFM and level-shifted PWM [1, 12].

A. LOW-FREQUENCY MODULATION

To control the proposed MLI in a way to produce high-quality sinusoidal output voltage a switching scheme based on LFM is designed according to Table I. This table has 28 switching states, and it shows the switching patterns for the used switches. By following these low-frequency patterns, multilevel voltage waveforms can be produced across the pole and load terminals.

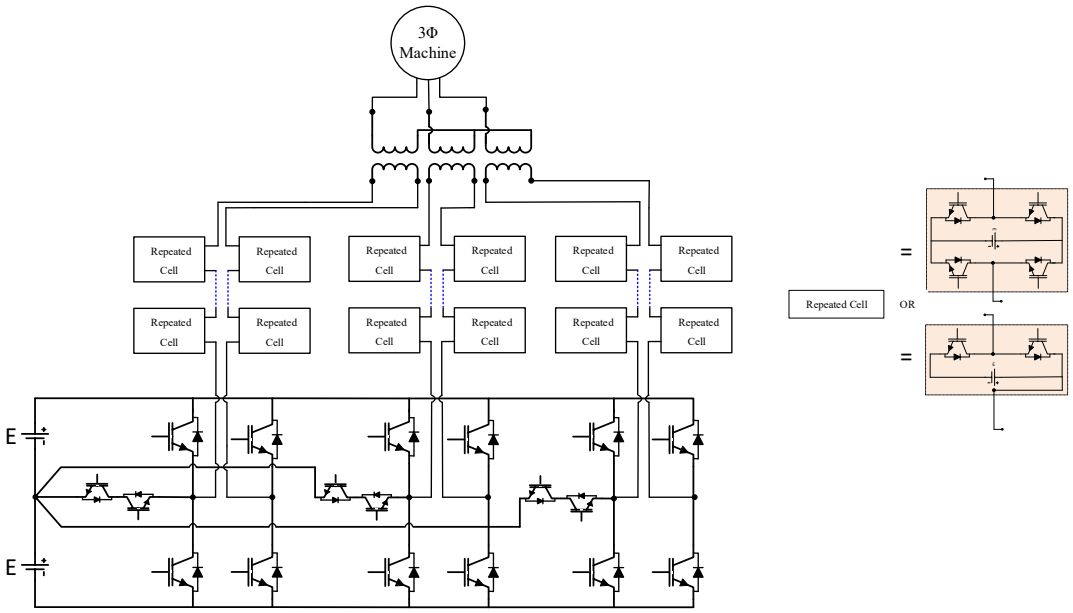


Fig. 1: The generalized configuration of the proposed topology.

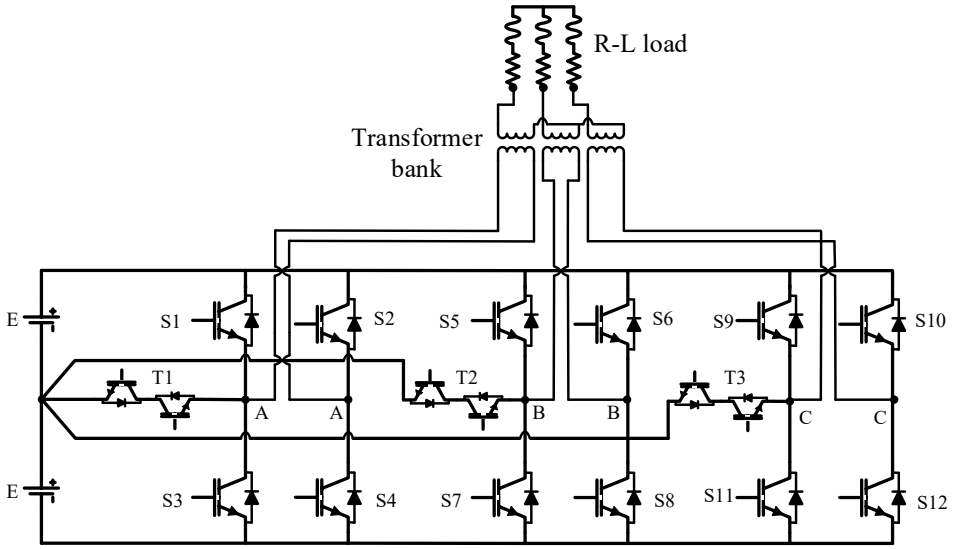


Fig. 2: The scaled-down configuration of the proposed topology.

TABLE I: THE SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGES
(■ ON, □ OFF)

V_{AA}	2E	2E	2E	2E	2E	2E	E	0	-E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-E	0	E	2E	2E	2E	2E	2E
V_{BB}	-2E	-E	0	E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	E	0	-E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E
V_{CC}	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-E	0	E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	E	0	-E	-2E
T_1							■		■													■		■					
S_1	■	■	■	■	■	■																			■	■	■	■	■
S_2									■	■	■	■	■	■	■	■	■	■	■	■	■								
S_3								■		■	■	■	■	■	■	■	■	■	■		■								
S_4	■	■	■	■	■	■	■	■														■	■	■	■	■	■	■	■
T_2		■		■												■		■											
S_5					■	■	■	■	■	■	■	■	■	■	■														
S_6	■	■															■	■	■	■	■	■	■	■	■	■	■	■	■
S_7	■		■													■		■	■	■	■	■	■	■	■	■	■	■	■
S_8			■	■	■	■	■	■	■	■	■	■	■	■	■	■													
T_3											■		■													■		■	
S_9														■	■	■	■	■	■	■	■	■	■	■	■				
S_{10}	■	■	■	■	■	■	■	■	■	■	■																	■	■
S_{11}	■	■	■	■	■	■	■	■	■	■		■															■		■
S_{12}												■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		

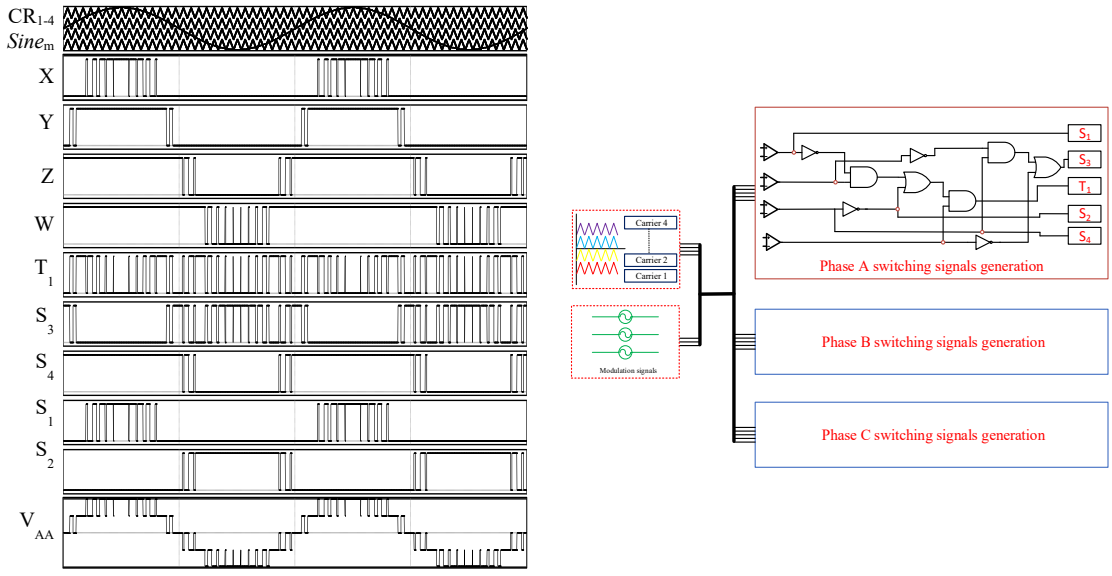
B. LEVEL-SHIFTED PULSE WIDTH MODULATION

Fig. 3 shows a switching scheme based on level-shifted pulse width modulation (LSPWM) and the key signals for phase A in the proposed circuit. For the purpose of producing five voltage levels using LSPWM, four carrier signals CR_1, CR_2, CR_3, and CR_4 are required as (4) [12]. These four carrier signals are equal in the magnitude, frequency, and phase angle.

$$N_{\text{carrier}} = N - 1 \tag{4}$$

The carrier signals are compared with three-phase modulation signals $Sine_{\text{m}}$, which are sinusoidal and have a phase shift of 120°. This is mandatory to produce three-phase balanced output sinusoidal voltages. Four control signals, *X*, *Y*, *Z*, and *W* are formed in the comparison process in the switching procedure. The switching pulses are formed by different logical operations on these four Boolean signals to make sure that switched multi-level sinusoidal signals are obtained on the output terminals.

Fig. 3 (a) shows only waveforms of phase A, while waveforms for phase B and C are the same with a phase shift of 120°. The switching scheme implementation is described in the proposed equations (5)-(9) and graphically shown in Fig. 3 (b).



(a) (b)

Fig. 3: The switching scheme for the proposed configuration. (a) Switching patterns and the resulted voltage V_{AA}. (b) Switching scheme implementation.

$$S_1 = X \tag{5}$$

$$S_2 = \overline{Z} \tag{6}$$

$$S_3 = \left(\overline{Y} \cdot Z\right) + \overline{W} \tag{7}$$

$$S_4 = Z \tag{8}$$

$$T_1 = \left(\left(\overline{X} \cdot Y\right) + \overline{Z}\right) \cdot W \tag{9}$$

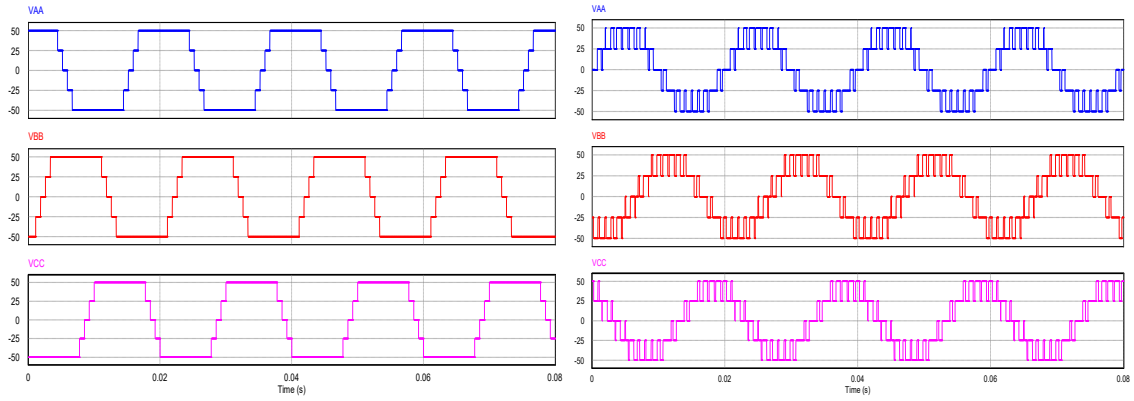
IV. Results and Discussions

A. Simulation Results

The proposed topology is simulated to verify its operating principle and to demonstrate the key waveforms. The simulation model based on the five-level case study in Fig. 2. It uses two symmetrical DC power supplies of 25 V. By controlling the proposed inverter using LFM and LSPWM, a nine-level voltage will be generated across the output terminals, the converter feeds power to an inductive load of 0.9 lagging power factor, R = 10 Ω, L = 75 mH. In LSPWM, the carrier frequency is equal to 1 kHz, and the modulation index (MI) is set to one (MI= 2*|$sine_m$|/|(CR_1+CR_2+CR_3+CR_4) |).

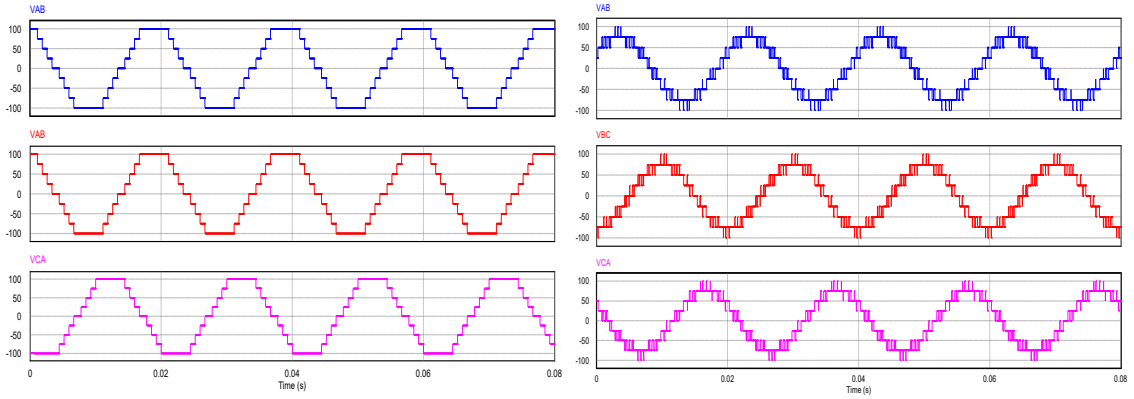
The operating principle is based on generating three five-level voltage waveforms V_{AA}, V_{BB}, and V_{CC} across terminals AA, BB, and CC, respectively. These waveforms must be shifted in phase to produce balanced three-phase voltages V_{AB}, V_{BC}, and V_{CA}, (e.g. $V_{AB} = V_{AA} - V_{BB}$). By using this technique there is no need for an end-side H-bridge that is commonly used for producing bipolar

voltages waveforms, so the voltage stress and switches are reduced. The pole-voltage waveforms are depicted in Fig. 4, including five voltage levels: *2E* ,*E*, *0*, *-E*, and *-2E* where *E*=25 V. By subtracting these three voltages waveforms from each other, three-phase balanced nine-level voltages are produced across the load terminals as described in Fig. 5, including three waveforms with nine steps



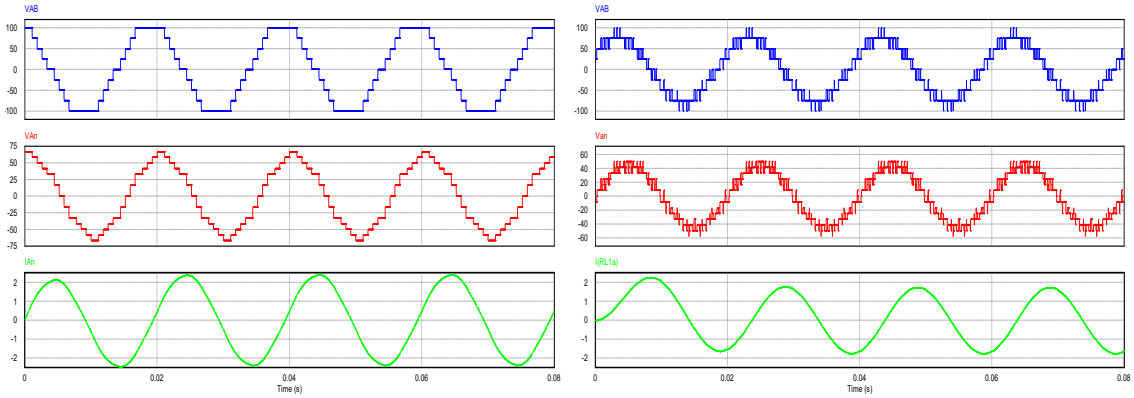
(a) (b)

Fig. 4: Pole voltages waveforms V_{AA}, V_{BB}, and V_{CC}. (a) Low-frequency modulation. (b) Level-shifted PWM.



(a) (b)

Fig. 5: Output voltages waveforms V_{AB}, V_{BC}, and V_{CA}. (a) Low-frequency modulation. (b) Level-shifted PWM.



(a) (b)

Fig. 6: Output waveforms under R-L load V_{AB}, V_{An}, and I_{An}. (a) Low-frequency modulation. (b) Level-shifted PWM.

4E ,3*E*, *2E* ,*E, 0*, *-E*, *2E* ,-3*E*, and *-4E*. Moreover, Fig. 6 not only shows the output voltages and load current but also shows the phase voltage V_{AN} having thirteen levels of $\frac{8}{3}E$, $\frac{7}{3}E$, $\frac{6}{3}E$, $\frac{5}{3}E$, $\frac{4}{3}E$, $\frac{2}{3}E$, 0, $\frac{-2}{3}E$, $\frac{-4}{3}E$, $\frac{-5}{3}E$, $\frac{-6}{3}E$, $\frac{-7}{3}E$, and $\frac{-8}{3}E$.

B. EXPERIMENTAL RESULTS

To validate the performance of the proposed topology, a laboratory setup was built and implemented to confirm the simulation results. Fig. 7 shows the in-house experimental setup, containing the proposed MLI, DC sources, three transformers, dSPACE's MicroLabBox controller, measurement tools and probes. Twelve IGBT modules - SKM300GA12E4 with built-in freewheeling diodes were used to produce a five-level MLI. These IGBT modules were controlled through twelve SKHI 10/12 R driver boards. The specifications of the simulation system are modified in order to match the currently available equipment in the laboratory. The experimental system parameters are listed in Table II. Figs. 8, 9 and 10 show the key waveforms at each stage of the proposed converter. The obtained waveforms show that the proposed MLI can produce five voltage levels under control of both low frequency and PWM switching schemes. Further, the effect of transformers on the output line voltages was indicated in Figs. 9 and 10.

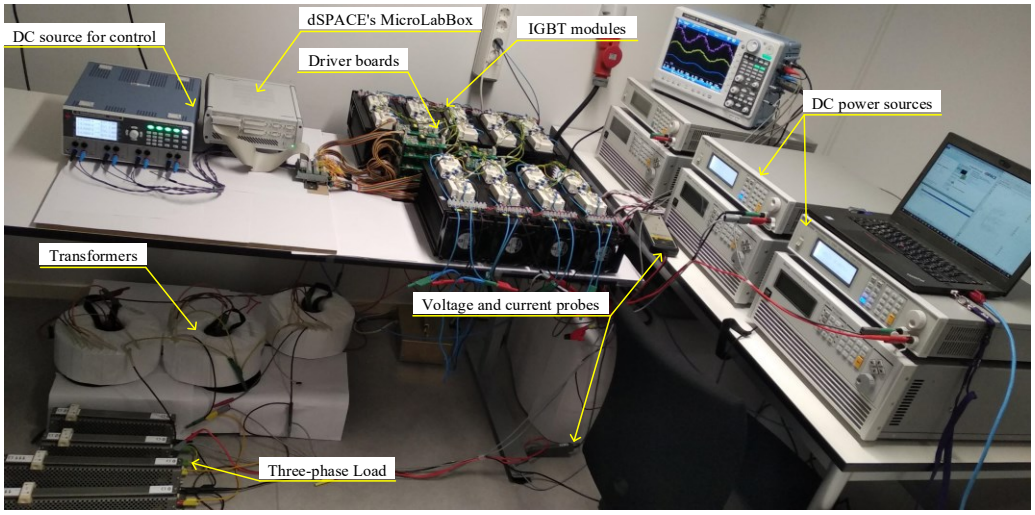
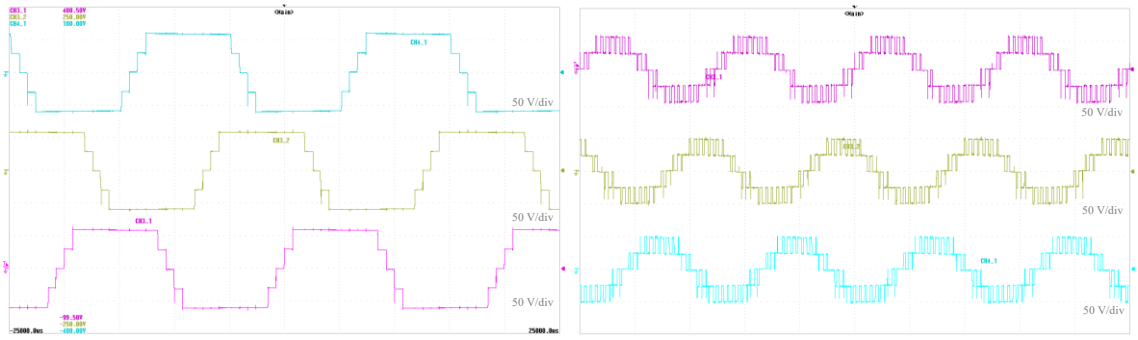


Fig. 7: Laboratory prototype of the proposed topology

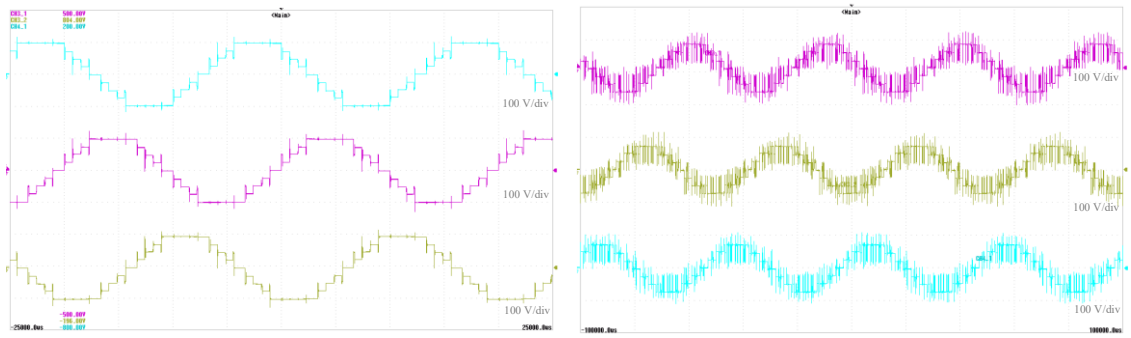
TABLE II: SPECIFICATIONS FOR EXPERIMENTAL SETUP

Parameter	Value	Unit
DC voltage source E	25	V
Load R	100	Ω
Switching Frequency F_s	1000	Hz
Sampling Time T_s	30	µs
Modulation Index MI	0.85	–
1-phase transformer (5 KVA)	240/240	V



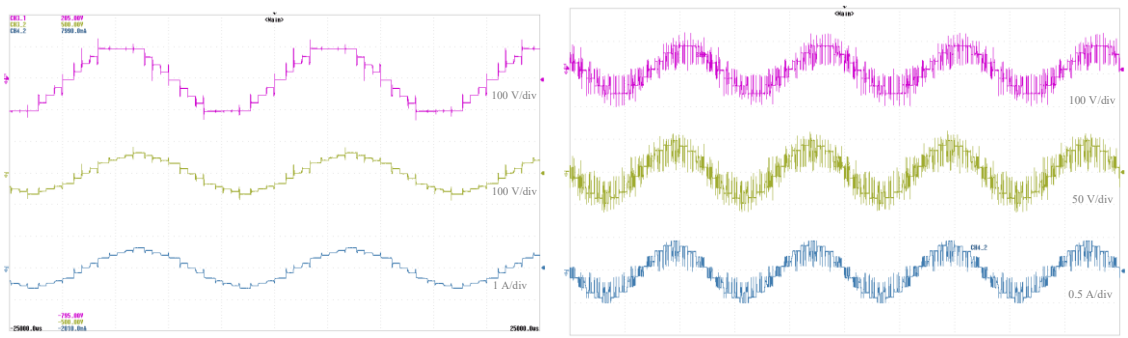
(a) (b)

Fig. 8: Pole voltages V_{AA}, V_{BB}, and V_{CC}. (a) Low-frequency modulation. (b) Level-shifted PWM



(a) (b)

Fig. 9: Output line voltages waveforms V_{AB}, V_{BC}, and V_{CA}. (a) Low-frequency modulation. (b) Level-shifted PWM.



(a) (b)

Fig. 10: Output waveforms under resistive load V_{AB}, V_{AN}, and I_{AN}. (a) Low-frequency modulation. (b) Level-shifted PWM.

V. Comparison of Five-Level Configurations

Recently, several MLI topologies have been introduced in [6-13] to reduce the total number of the used components. A comparison between the proposed topology and the existing ones with the same output voltage levels are summarized in Table III to illustrate the merits of the proposed configuration. The comparative study shows that the proposed structure has various significant merits: low component count, without using electrolytic capacitors for its operation or additional circuit for balancing process, resulting in higher reliability and lifetime, lower control complexity. Moreover, the proposed configuration is a diode-free

topology, enhancing efficiency, since power diodes consume higher energy than other semiconductor devices. From the applications point of view, the proposed MLI has a modular structure feature, allowing the output voltage levels to increase without increasing voltage stress across the switching devices. Further, both complete isolation and flexible output voltage value are guaranteed by using transformers bank, which is very useful in upgrading existing systems. To sum up, the proposed topology is an attractive solution in applications that require a high-reliability degree, simple control and multi-level output voltages with isolation features.

TABLE III: COMPONENTS REQUIREMENT FOR FIVE-LEVEL THREE-PHASE CONVERTERS

Topology	DC Sources	Switches	Diodes	Capacitors	Transformers	Total	CLF* Factor
[10] 5L-Topolgy 4	1	68	0	3	0	72	14.4
[10] 5L-Topolgy 3	1	62	0	1	2**	66	13.2
Neutral point Clamped	1	24	36	4	0	65	13.0
[10] 5L-Topolgy 1	1	50	2	0	0	53	10.6
[6] 5-level topology	6	24	12	6	0	48	9.6
[10] 5L-Topolgy 2	1	44	0	2	0	47	9.4
[9]	1	36	0	8	0	45	9.0
[10] Stacked multicell converter (SMC)	2	36	0	6	0	44	8.8
[8]	1	24	6	5	0	36	7.2
Half H-Bridge	12	24	0	0	0	36	7.2
[13]	10	24	0	0	0	34	6.8
[12]	4	27	0	0	0	31	6.2
[7]	1	24	0	2	3	30	6.0
[6]	9	18	3	0	0	30	6.0
Full H-Bridge	6	24	0	0	0	30	6.0
Proposed Topology	2	18	0	0	3	23	4.6

*components per level factor [13], ** power inductors, not transformer

VI. CONCLUSION

In this study, a new modular multilevel topology suitable for high-voltage medium power applications was proposed. Although the proposed topology can produce N-level, only five-level version was studied and validated in this paper. For the purpose of illustrating operating principles of the proposed topology, both pulse width and low-frequency modulation strategies are successfully developed and implemented. Further, the simulation results were experimentally validated by using an in-house lab setup. Moreover, a comparative study between the proposed circuit and other multilevel inverter topologies was conducted and summarized. Compared to the existing five-level topologies, the proposed topology has the merits of using low component count for producing the same number of output voltage level. Finally, several significant limitations due to using transformers such as size, noise, and presence of leakage or parasitic inductance, etc. need to be considered in certain applications.

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