Novel Three-Phase Multilevel Inverter with Reduced Components for Low- and High-Voltage Applications

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Abstract—**This paper presents a novel multilevel topology for three-phase applications, having three-level and hybrid N-level modular configurations, enabling low-, medium-, and high-voltage operations. The proposed topology has several attractive features, namely reduced component count, being capacitor-, inductor-, and diode-free, lowering cost, control-complexity, and size, and can operate in a wide range of voltages and powers. Selected simulation and experimental results are presented to verify the performance of the proposed topology. Further, the overall efficiency of the topology and loss distribution in switches are studied. Finally, the key features of the proposed topology in terms of component count, blocking voltage, and DC-link requirements are highlighted via a comparative study.**

Index Terms—DC-AC power converters, low-frequency modulation, multilevel inverters, pulse width modulation.

I. INTRODUCTION

Multilevel inverters (MLIs) have played a key role in modern DC-AC converters or energy conversion systems due to their attractive features of modularity, high switching redundancy, voltage scalability, low harmonics contents in output waveforms and low dv/dt stress [1-22]. These features make MLI-based DC-AC systems having low total harmonic distortion (THD), low filter requirements, low electromagnetic interference (EMI), high-voltage high-power capacities, fault-tolerant operation, and utilising low-voltage switches for high-voltage applications. However, MLIs suffer from complex control strategies and high component count, resulting in high cost, bulky size, reduced efficiency and reliability. Three conventional MLI topologies, namely cascaded H-bridge (CHB) MLI [23], neutral point clamped (NPC) MLI [24], and flying capacitor (FC) [25] have been a baseline for research and development of MLIs over past decades. Reducing total component count and simplifying the control requirements by reducing active switches and flying capacitor count have been attractive topics to lower required sensors and sophisticated gate drivers or reduce the size and cost of the converters [1-12]. Configurations, advantages, and disadvantages of these recently developed circuits are highlighted hereafter, and more details can be found in [1-12].

The authors in [1] presented a capacitor-based three-level unit, consisting of three switches, two capacitors, and four diodes, being repeated for generating higher voltage levels. In each unit, the DC source is used for charging the two capacitors, and never directly connected to the load. Consequently, the voltage levels across the unit terminals are 0, V_{C1}, and V_{C2}, where V_{C1} and V_{C2} are the voltage across the two capacitors, and each of them is equal to half of the DC source voltage. The main merits of this structure are summarized as low switch count, medium voltage stress across the semiconductor components, symmetrical and asymmetrical operation capabilities, generating both positive and negative voltages without a polarity changer, and low count of switches in the current paths. However, the topology requires four power diodes and two capacitors per each unit, resulting in negative effects on size, cost, and lifetime of the inverter.

To address the problem of using capacitors in [1], the authors in [2] presented a capacitor-free circuit, integrating the conventional half-bridge (HB) with a new two-level structure to construct a three-phase MLI. This design can generate N voltage levels by increasing the number of connected HB cells in cascade. The two-level structure consists of three modified full H-bridge (MFHB) and one main DC source of V_{M}. The output voltages of this structure are limited by only two levels of 0 and the maximum voltage V_{M}. Each MFHB has eight semiconductor devices (four diodes and four switches) connected in parallel with the main DC source. The cascaded HB part is used for generating any voltage level between 0 and V_{M}, in which one HB is needed for each level, i.e. one DC source and two switches. This topology has features of a reduced component count, being inductor-, capacitor-free, and extendable for producing N levels. Further, the DC sources in HB stage can be isolated or non-isolated, simplifying the realisation of these sources. On the other hand, its main disadvantages include using several power diodes and DC sources, resulting in high losses and cost. Further, significant voltage stress across all semiconductor devices in the two-level structure due to extra HB cells. Such drawbacks restrict the topology's voltage level number and reduce its reliability, especially in high-voltage applications.

Hybrid MLIs, requiring multiple DC sources like the presented topologies in [1, 2], were reported and discussed in [3, 4, 6]. The topologies in [3, 4] have similar structures with two stages, high-frequency stage (HFS) and low-frequency stage (LFS). The HFS is responsible for generating both zero- and positive-voltage levels, being called as a level generator (LG), while LFS is used to change the polarity every half cycle to produce bipolar output voltages, being called as a polarity changer (POCH). In these topologies, a full H-bridge is used as a POCH while HB or switched-diodes (SD) cells are used to construct the LG stage. The SD's cell is formed by one DC source, one switch, and one diode, saving one switch as compared to the HB with the same number of DC sources, but it requires one diode for each cell. Many isolated DC sources and twelve high-voltage switches are required in the second stage, i.e. the POCH, in which their voltage rating is a function of the cell number in the LG stage. Accordingly, the presented topologies have a high loss in the second stage, restricting them to be used in low-voltage applications alone, for example, in PV farms, where implementing a high number of isolated DC sources becomes easier. Structure simplicity, capacitor- and

inductor-free features, operating in both symmetrical and asymmetrical modes, and reduced component count are the key advantages of these MLI topologies. To reduce high-voltage switches in [3, 4], the authors in [5] presented a topology using two switches for changing the polarity instead of four switches. Although the topology in [5] requires the same number of DC sources like the topologies in [3, 4], it needs six capacitors, increasing the footprint and control complexity of the converter.

Towards both low- and high-voltage applications, the authors in [6] presented a three-phase hybrid MLI configuration, consisting of three units: two-level three-phase VSI, three single-phase three-level FHB and three two-level HB. The authors suggested that repeating the second unit increases the voltage levels. Generating three levels in the topology would need four DC sources and twelve switches. Modularity is the key feature of this topology, so high voltages can be obtained without increasing the voltage stress across switches, making the topology suitable in high-voltage high-power applications. However, requiring many isolated DC sources and high switch count in the conduction paths are its main drawbacks.

To avoid using multiple DC sources, single-source topologies like T-type and NPC MLIs were proposed to use as three-level inverters [9]. Due to the lower count of power electronics components in the current paths, the T-type MLI has a lower conduction loss than NPC. For example, any positive or negative voltage level in the T-type inverter needs only one switch in the current path while two switches are required in case of NPC regardless of the voltage level. However, the switching loss in NPC is lower than that in T-type because the switch blocking voltages of the NPC are lower than those in the unidirectional switches of T-type MLI [9] as well explained in [26, 27]. The authors in [7-9] presented modified circuits to overcome some drawbacks of both T-type and NPC MLIs. The modified circuit in [7] reduces the switch count to nine instead of twelve in the conventional T-type MLI. However, it requires twelve diodes, two capacitors and one DC source for generating three voltage levels. The designed circuit is only applicable to low-voltage applications as the main six switches block the full DC-link voltage, like conventional T-type inverters. Although the count or number of switches is reduced, the total power electronics components are increased in the current path, resulting in a high conduction loss. A diode-free T-type MLI, using 18 switches, two capacitors, and one DC source, is presented in [8] as a solution of reducing conduction losses of the topology in [7], but it doubles the switch count. The presented topology uses only active switches, removing the power diodes from the bidirectional-switch structures in [7]. Accordingly, zero-vector current paths will not involve any power diode, reducing the conduction losses. As compared to T-type MLIs, NPC inverters have a higher uneven loss distribution among power electronic components or unequal junction temperature rises, reducing the switching frequency and power rating of the converter [9, 28]. To solve the mentioned problems, the authors in [9] presented a hybrid active neutral point (hybrid-ANPC) topology, generating three voltage levels by using three legs of six switches, two capacitors, and one DC source. Despite increasing the power

density, the proposed topology requires a higher count of switches and gate drivers' circuits than those in the conventional NPC MLIs.

The mentioned MLI configurations use complementary switches, causing shoot-through problems or reducing the circuit reliability. Implementing a dead-time through hardware or software is to avoid the shoot-through, but might distort the output waveforms and increase the converter losses due to the poor characteristics of freewheeling diodes [29]. To overcome these issues, a family of dual-buck MLIs (DB-MLIs) is presented in [10], aiming to split each leg into two new legs formed by diodes and switches. These legs are connected through a coupled inductor network for forming phase voltages. Additionally, three diodes are required to link each phase to the DC-link. The presented topology has two DC ports for connecting low- and high-voltage sources at the same time, allowing for using two renewable energy sources (RESs) with different output voltages. In case of using a single low-voltage DC source, a boost converter (BC) is required to implement the high-voltage source. The BC is bypassed based on the instantaneous AC output voltage value. The presented topology requires nine switches, nine diodes, two isolated DC sources, and three coupled inductors, resulting in a converter with a bulky size, high cost, and low efficiency. Other two asymmetrical MLIs with dual DC-ports are presented in [11], which are based on NPC, and T-type configurations. Using the same DC-link structure for the dual-DC port MLI in [10] allows them to feed power to a load from low- and high-voltage DC sources. Both configurations in [11] require extra three switches but do not use any coupled inductor to produce the same number of voltage levels in [10]. Further, the T-type-based configuration does not need any diode while NPC-based configuration needs three additional diodes. Unlike the topology in [10], a dead-time is recommended to be used in [11] for avoiding short-circuit faults.

The above review of the recently developed multilevel inverters proves that the existing MLIs are still bulky due to a high number of components, and restricted by voltage level applications, namely low or high voltage level alone. An initial study of a novel three-level MLI with a reduced component count was presented in [30] based on simulation results. This manuscript details the low-voltage configuration of the previous work and presents a new *N*-level hybrid configuration for high-voltage applications. Further, the switching algorithm for low-frequency modulation (LFM) is modified in order to control the RMS value, level count, and frequency of the output voltage online. Additional simulation results are presented for both configurations. Within this framework, the proposed low-voltage configuration is experimentally validated through an in-house test setup. Finally, the key features of the proposed topology are proven via a comparison with other topologies in [1-12].

II. THE PROPOSED MULTILEVEL INVERTER

In this section, the circuit description and switching schemes of the proposed topology are introduced and discussed in detail.

A. CIRCUIT DESCRIPTION

The low-voltage configuration of the proposed topology is shown in Fig. 1, which is a transformerless MLI and does not require any flying capacitor (FC), or power diode or coupled inductor (CI) in its operation, allowing for a high-efficiency and compact design. Each phase consists of only four switches, being distinctively connected for constructing a three-level unit. Further, to reduce the DC source count, the three-phase legs share the same DC-link. The DC-link is formed by connecting two symmetrical DC sources of E in series. However, these DC sources can be replaced by batteries or AC voltage sources followed by rectifiers or different RESs, e.g. PV strings and fuel cells.

Twelve power switches S_1 to S_{12} are used to create different paths from the two DC sources to the load. Therefore, the DC sources can be arranged in different ways for producing five levels $2E$, E, 0, $-E$, and $-2E$ in the line voltage. For example, when S_1, S_6, S_8, and S_9 are in ON-state, and the remaining switches are in OFF-state, the line voltages V_{AB}, V_{BC}, and V_{CA} are equal to $2E$, $-2E$ and 0, respectively. Fig. 2 shows the switching modes for the proposed circuit when producing five voltage levels in the line voltage V_{AB}, along with the conduction paths for the forward and reverse currents in red and blue lines, respectively. These switching modes have been selected in a way to prevent any appearance of a positive voltage across built-in diodes of the switches. As a result, the DC sources are protected from short-circuit faults. Further, for the same reason, some selected switching states are removed from the control algorithms of the inverter. For example, in phase A, $(S_1$-$S_3)$, (S_1, S_2, S_4) and (S_3, S_4) cannot be in ON-state at the same instance.

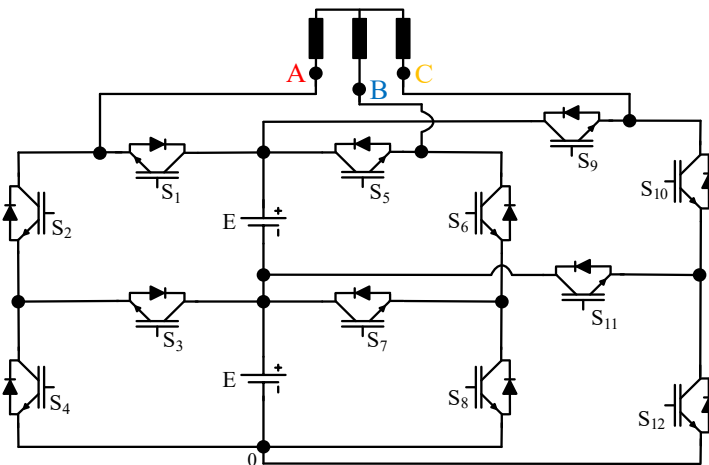Fig. 1. Low-voltage three-level configuration of the proposed topology.

In addition to the low-voltage configuration of the proposed inverter, the N-level hybrid configuration for high-voltage applications is proposed as shown in Fig. 3, using the three-level configuration as a fixed stage and a new three-phase module as a repeated stage. Each module has three basic cells or one cell for each phase. Each basic cell requires eight switches and two DC sources. It can produce five voltage and seven voltage levels for symmetrical and asymmetrical DC sources, respectively. As shown in Fig. 1, the basic cell is formed by using the DC-link and either (leg A + leg B) or (leg B + leg C) or (leg C + leg A), this is the two-phase

version of the fixed stage. The basic cell is formed in a way to allow it to be used in the two proposed configurations, reducing manufacturing, maintenance, voltage upgrading cost and time.
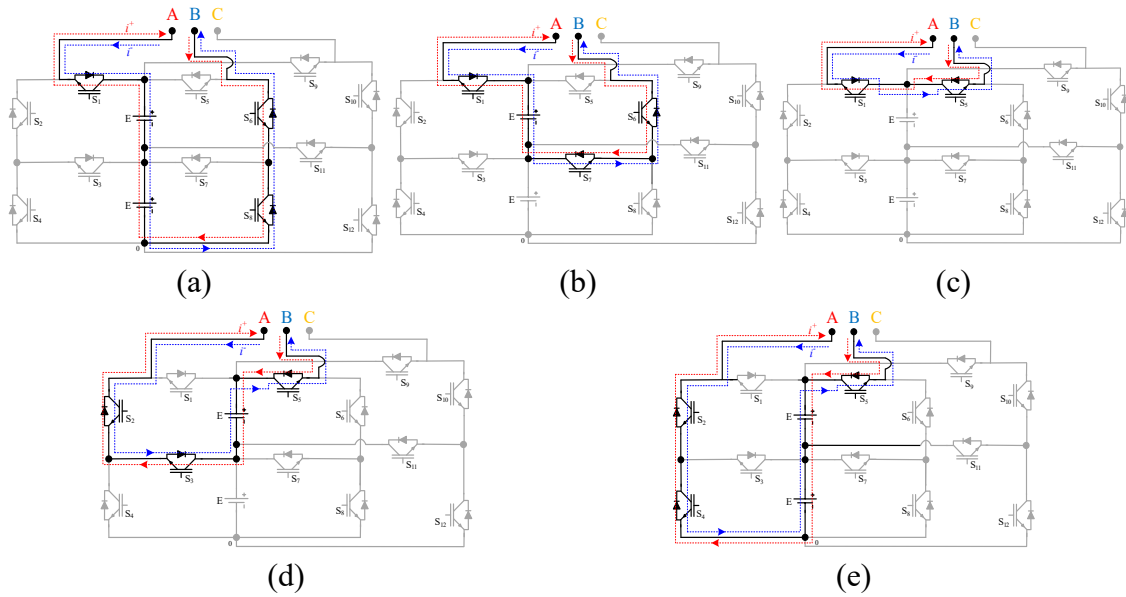

Fig. 2. The switching modes for the low-voltage configuration. (a) $V_{AB} = 2E$. (b) $V_{AB} = E$. (c) $V_{AB} = 0$. (d) $V_{AB} = -E$. (e) $V_{AB} = -2E$.
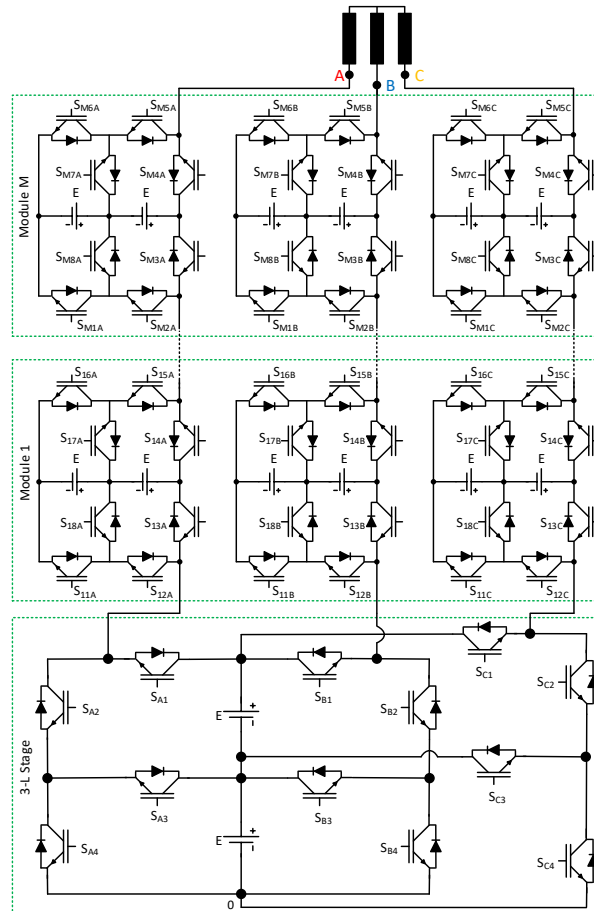

Fig. 3. N-level high-voltage configuration of the proposed topology.

In the hybrid configuration of the proposed topology, the voltage levels can be enlarged to N levels without increasing the voltage stress across the switches due to the modularity feature. The counts of the three-phase modules M, switches N_{SW}, and DC sources N_{DC} in term of voltage levels N, are presented in (1) - (3). For producing seven levels in the pole voltage, only one module is needed as calculated in (1). Consequently, eight symmetrical DC sources and thirty-six switches are required according to (2) and (3), respectively.

$$M = 0.25N - 0.75 \qquad (1)$$

$$N_{DC} = 1.5N - 2.5 \qquad (2)$$

$$N_{SW} = 6N - 6 \qquad (3)$$

It is worth mentioning that the switch count for each module can be reduced to eighteen instead of twenty-four switches. This can be obtained by merging the three switches S_{M5A}, S_{M6A}, and S_{M7A} in each basic cell to be one switch and changing the switching algorithm a little bit. For example, in the first module (i.e. $M = 1$), S_{15A}, S_{16A}, and S_{17A} can be merged to be one switching device with a higher blocking voltage ($2E$ instead of E). Accordingly, the total number of required switches could be reduced, as calculated in (4) for symmetrical operation.

$$N_{SW} = 4.5N - 1.5 \qquad (4)$$

B. MODULATION STRATEGIES

The low-voltage configuration as shown in Fig. 1 has 64 switching states, but only twelve states are required and summarized in Table I, being used in the switching algorithms for two modulation techniques. These twelve switching states are selected in a way to prevent any switching paths to form a closed loop for the DC sources. Further, to reduce the conduction losses, reducing the count of ON-switches in the conducting path for each level was taken into consideration when selecting these switching states. Table I shows that the switching states of S_3 and S_4 are labelled with 'X' letter for producing $2E$ in pole A. 'X' letter means these switches can be either in ON- or OFF-state, but the switching cycles are minimised to reduce the switching loss. For this reason, the switching algorithms were designed to keep the same previous states of S_3 and S_4 to be their new switching states, i.e. X-state will be ON if the previous state was ON, and vice versa. For example, in S_4, the previous switching state was OFF, so the new state is selected to be OFF.

Fig. 4 shows the switching patterns for the LFM and highlights the three-pole voltage waveforms V_{A0}, V_{B0}, and V_{C0}. The LFM uses three rectified sinusoidal waveforms with amplitudes of 1. These waveforms are compared to two signals, 'Zero-reference' and a proposed modulator signal (called as H), to generate L_1-L_6. The value of the modulator signal H can be varied from 0 to 1 for obtaining different numbers of voltage levels. Therefore, the proposed modulator H adds more flexibility for the online control of both level number and root mean square (RMS) value of the output voltages. Implementing Boolean operations on L_1 and

L_2, as described in (5)-(6), results in the switching signals for phase A. For phases B and C, the procedures are similar except a phase-shift of 120°.

TABLE I
SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGE OF
PHASE A (X: ON OR OFF)

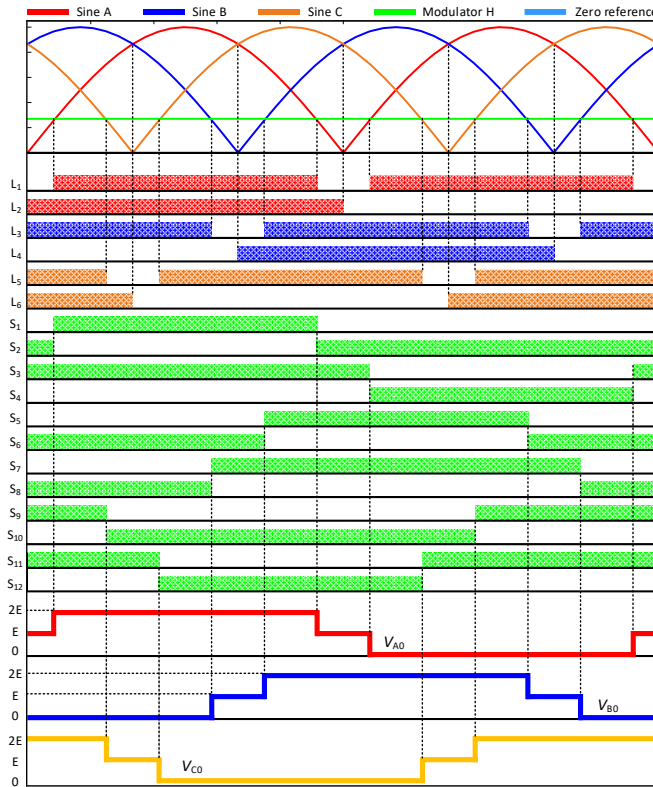| V_{A0}	S_1	S_2	S_3	S_4
	Pole A			
E	OFF	ON	ON	OFF
$2E$	ON	OFF	X	X
$2E$	ON	OFF	X	X
$2E$	ON	OFF	X	X
$2E$	ON	OFF	X	X
$2E$	ON	OFF	X	X
E	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON

Fig. 4. LFM switching scheme for the proposed inverter.

$$\overline{S_1}, S_2 = \overline{L_1 \times L_2} \tag{5}$$

$$\overline{S_3}, S_4 = L_1 \times \overline{L_2} \tag{6}$$

Switching signals of the high-voltage configuration can be generated based on Table II, listing the full switching states for producing seven voltage levels. It shows twenty-seven states, seven primary states (written in blue) and twenty redundant states, providing some flexibility in the switching algorithms, balancing power losses of switches and increasing the reliability. The reason for selecting the seven primary states is to minimise the count of ON-switch in conduction paths and reduce the conduction losses. For example, six possible switching states can be used to produce a $2E$ level, but the second state with three ON-switches is selected and marked as a primary state, reducing the conduction losses by at least 40% when producing $2E$ since the other five states use either five or six ON-switches.

TABLE II
SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGE FOR SEVEN-LEVEL
CONFIGURATION OF THE PROPOSED TOPOLOGY

V_{A0}	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{11A}	S_{12A}	S_{13A}	S_{14A}	S_{15A}	S_{16A}	S_{17A}	S_{18A}
	Phase A, fixed stage				**Phase A in the first module**							
4E	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
3E	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF
	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
	OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
2E	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON
	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON
	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
E	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON
	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON
	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF
	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON
	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
E	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON
	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
-2E	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF

In addition to LFM, the LS-PWM scheme was implemented as shown in Fig. 5. Using two carrier signals C_{R1} and C_{R2} and three sinusoidal waveforms S_{M1}, S_{M2},

and S_{M3} generates the required switching pulses for the switches in the low-voltage configuration. The signals of S_{M1}-S_{M3} have the same magnitude and shape with a phase-shift of 120° among them. Fig. 5(a) shows the generation process of switching pulses for the four switches in phase A. The Y and Z signals are generated by comparing the S_{M1} with the two carrier signals. Afterwards, different Boolean operators are used for extracting the correct switching signals from Y and Z, as seen in Fig. 5(b). Similarly, the switching pulses for the high-voltage configuration can be generated based on Fig. 5, but the number of carrier signals is increased to six instead of two. Accordingly, six controlling signals labelled by X_1 to X_6 from top to down are generated by comparing the sinusoidal modulation signals with six carrier signals. The switching pulses of phase A are obtained by implementing the Boolean operations on the six controlling signals as summarised in (7)-(15).
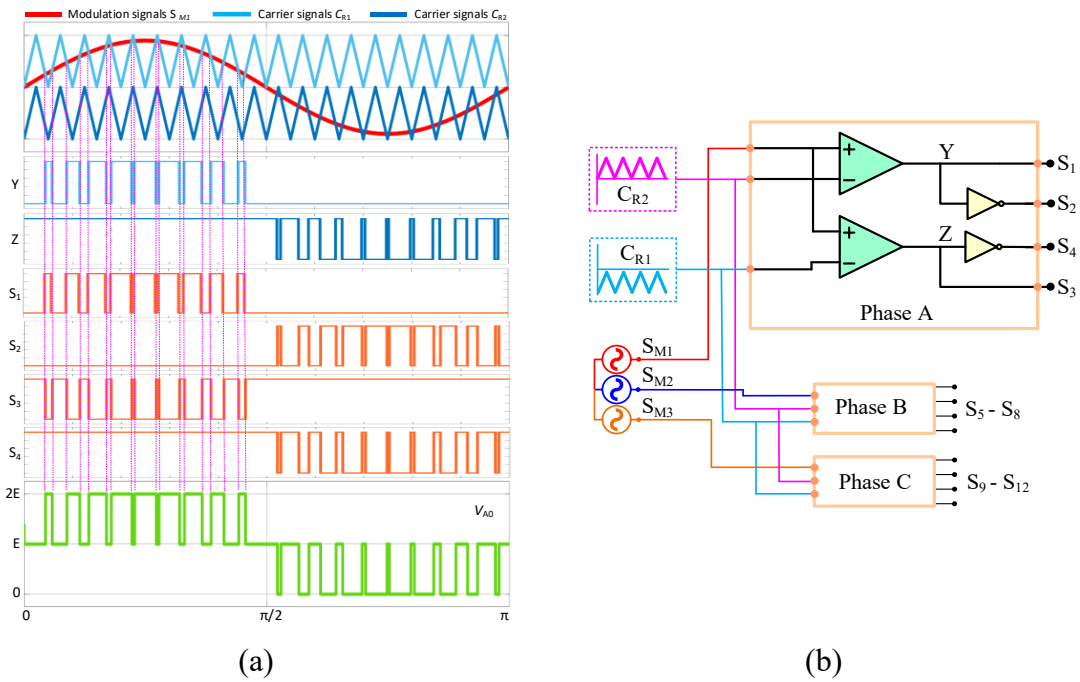

Fig. 5.   LS-PWM switching scheme for the low-voltage configuration. (a) Key waveforms. (b) Switching logic.

$$S_{A1}, \overline{S_{A2}} = X_3 \tag{7}$$

$$S_{A3} = \overline{X_3} \times X_4 \tag{8}$$

$$S_{A4} = \overline{X_4} \tag{9}$$

$$S_{11A} = X_1 \tag{10}$$

$$S_{12A}, \overline{S_{13A}} = X_2 \tag{11}$$

$$S_{14A}, \overline{S_{15A}} = X_5 \tag{12}$$

$$S_{16A} = \overline{X}_6 \tag{13}$$

$$S_{17A} = \overline{X}_5 \times X_6 \tag{14}$$

$$S_{18A} = \overline{X}_1 \times X_2 \tag{15}$$

III. SIMULATION AND EXPERIMENTAL RESULTS

To verify the operating principles of the proposed circuit, both switching schemes are simulated in Matlab/Simulink and experimentally validated on a laboratory prototype. For building the low-voltage prototype, twelve insulated-gate bipolar transistors (IGBT) modules with built-in freewheeling diodes are used, in addition to two DC voltage sources. The complete in-house setup is captured and showed in Fig. 6. The digital controller -dSPACE MicroLabBox is used to implement the switching algorithms for both LFM and LS-PWM. Two primary DC sources are used for supplying the electrical power to the three-phase load through twelve IGBT modules SKM300GA12E4, in which each IGBT is controlled through a SKHI 10/12 R gate-driver board and attached to a heatsink for reducing the temperature of the IGBT's internal junction. Further, the test setup includes secondary devices such as low-power DC source for driver boards, oscilloscope, voltage- and current-probe. Table III lists specifications of the studied cases in simulations and experimental tests.
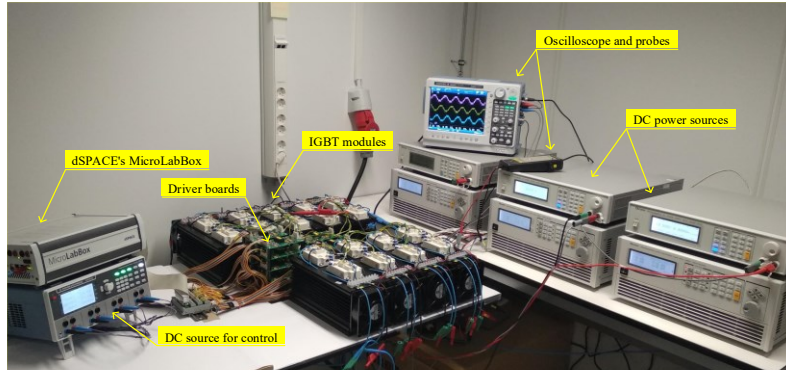

Fig. 6. The in-house experimental setup.

TABLE III
SYSTEM SPECIFICATIONS AND USED COMPONENTS

Description	Value/ Part number	Unit
DC voltage source (E)	70	V
Load R, X_L	30, 31.41	Ω
Carrier frequency (F_S)	1000	Hz
Modulation signal frequency (F)	50	Hz
Modulation index (M_I), LS-PWM	0.9	−
Modulator signal (H), LFM	0.27	−
Sampling time (T_S)	15	μs
Switching device	SKM300GA12E4	−
Gate-driver board	SKHI 10/12 R	−
DC voltage source	62024P-100-50	−

Figs. 7(a) and 8(a) show the simulation waveforms of the pole voltages V_{A0}, V_{B0}, and V_{C0} for LFM and LS-PWM, respectively. Each waveform has three voltage levels of 0, E, and $2E$, in addition to a phase-shift of 120° for the two other pole voltages. The waveforms of experimental tests are presented in Figs. 7(b) and 8(b), matching well the obtained simulation results in Figs. 7(a) and 8(a). In the experimental results, the 'voltage-per-division' setting was changed from standard values into flexible ones to make sure that the obtained results fit the oscilloscope screen. Figs. 9 and 10 depict the balanced three-phase line voltages V_{AB}, V_{BC}, and V_{CA}, where five voltage levels of $2E$, E, 0, $-E$, and $-2E$ were produced by maintaining the pole voltages in the same conditions as shown in Figs. 7 and 8, (i.e. three levels and phase-shift of 120°). A resistive-inductive (R-L) load is used to verify the performance of the proposed inverter under loading conditions. Figs. 11 and 12 illustrate the obtained results when using a load with a lagging power factor of 0.7. Further, Figs. 11 and 12 show the five-level line voltage V_{AB} in the first trace while the phase voltage V_{AN} and load current I_{AN} are shown in the second and third traces, respectively.
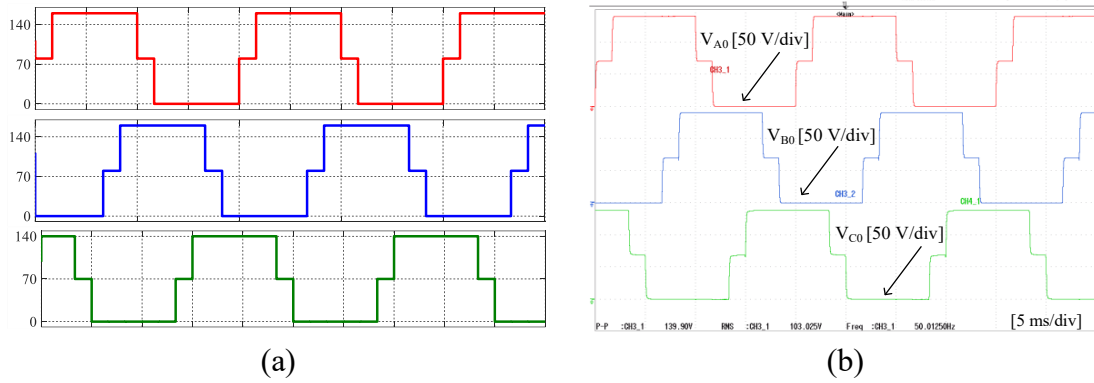

(a) (b)

Fig. 7. Pole voltages V_{A0}, V_{B0}, and V_{C0} for LFM. (a) Simulation. (b) Experimental.
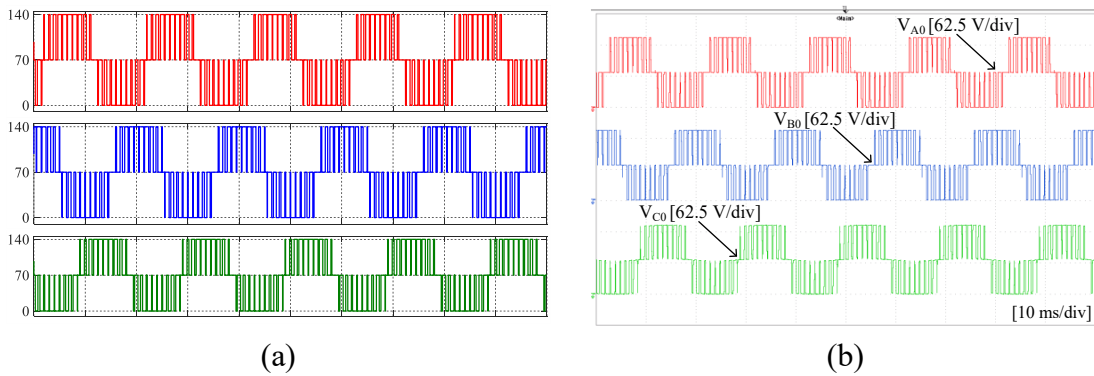

(a) (b)

Fig. 8. Pole voltages V_{A0}, V_{B0}, and V_{C0} for LS-PWM. (a) Simulation. (b) Experimental.

As observed from the second trace in Figs. 11 and 12, the phase-load voltage has seven levels of $-4/3E$, $-E$, $-2/3E$, 0, $2/3$ E, E, and $4/3E$ under LFM, while nine levels of $4/3E$, $-E$, $-2/3$ E, $-1/3E$, 0, $1/3E$, $2/3E$, E, and $4/3E$ are obtained under the LS-PWM control. The two extra levels come from the different pole voltage combinations for the two modulation schemes. Table IV shows a list of different combinations of voltage values across the poles of the proposed topology. In case of generating the switching pulses by using the LFM scheme, only seven voltage

combinations can be achieved (*A*1-*A*3), *A*5, and (*A*7-*A*9), while nine voltage combinations (*A*1-*A*9) are obtained by using the LS-PWM scheme.

Although the LFM scheme uses lower frequency signals for generating the switching pulses, the LS-PWM switching scheme has a higher degree of flexibility. In the LS-PWM, the output voltage frequency, RMS value, and the number of levels can be controlled online by changing the frequency and magnitude of the modulation signal. In the LFM scheme, the proposed modulator *H* is integrated into the switching algorithm to add a degree of freedom for changing the output level count and RMS value while the frequency of the output voltage is changed in the traditional way using the sinusoidal modulation signals.
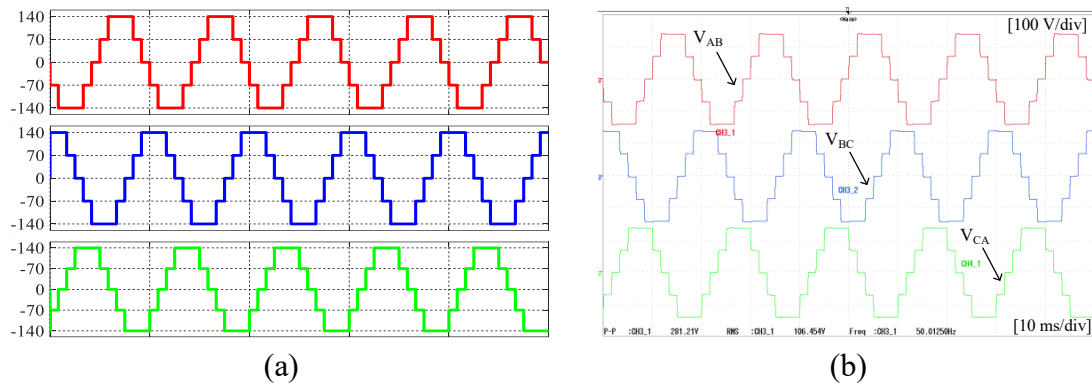

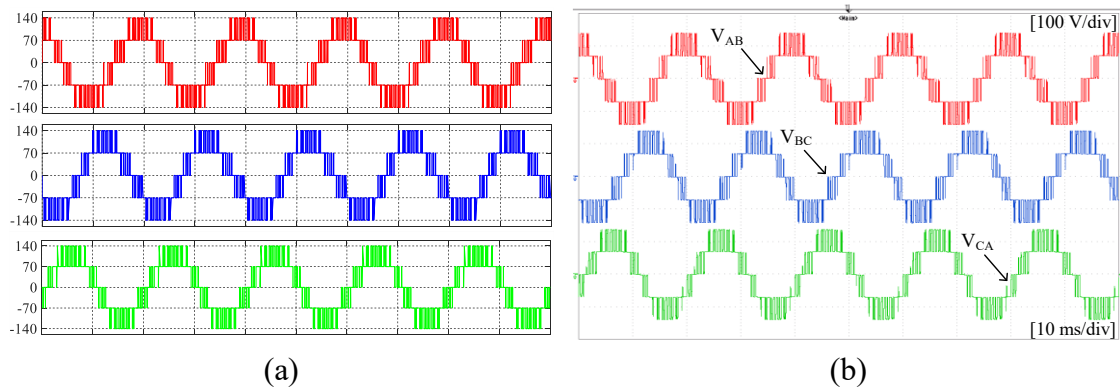Fig. 9. Line voltages V_{AB}, V_{BC}, and V_{CA} for LFM. (a) Simulation. (b) Experimental.

Fig. 10. Line voltages V_{AB}, V_{BC}, and V_{CA} for LS-PWM. (a) Simulation. (b) Experimental.
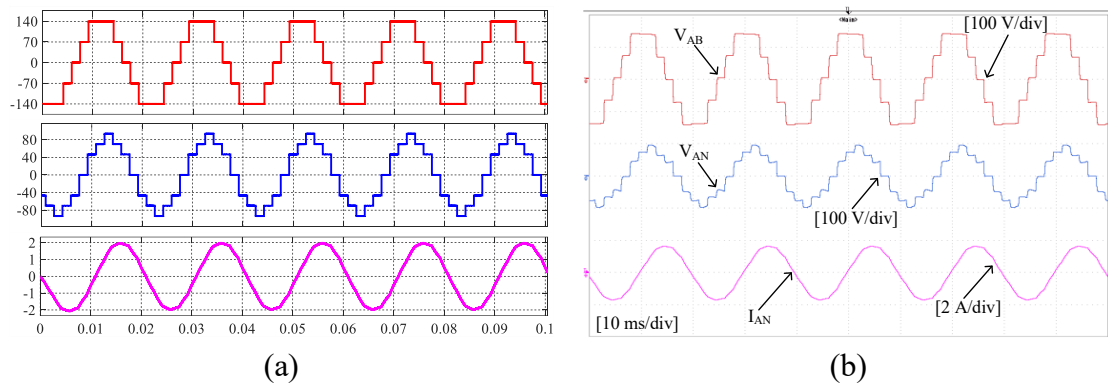

Fig. 11. Obtained V_{AB}, V_{AN}, and I_{AN} for LFM. (a) Simulation. (b) Experimental.

Figs. 13(a) and (b) show the simulation and experimental output line voltage waveforms at different values of the modulator H. By changing H from 1 to 0, the RMS value of the line voltage is varied from 0% to 81.6% of the DC-link voltage. Further, the line voltage has zero-, three-, and five levels when H is 1, 0.9, and 0.2, respectively. Therefore, the proposed topology can produce the output voltage with variable magnitudes, frequency, and level counts for both the LS-PWM and LFM.
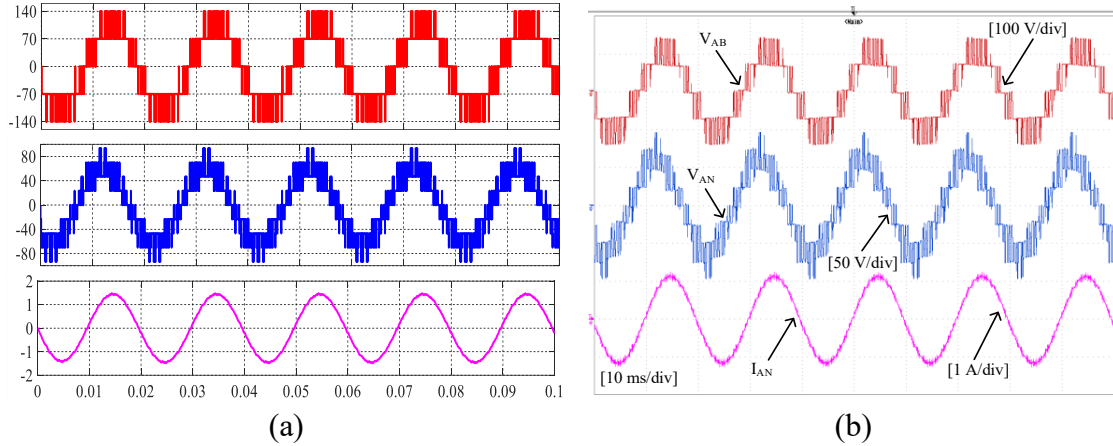

Fig. 12. Obtained V_{AB}, V_{AN}, and I_{AN} for LS-PWM. (a) Simulation. (b) Experimental.

TABLE IV
POLE VOLTAGE COMBINATIONS FOR THE USED SWITCHING SCHEMES

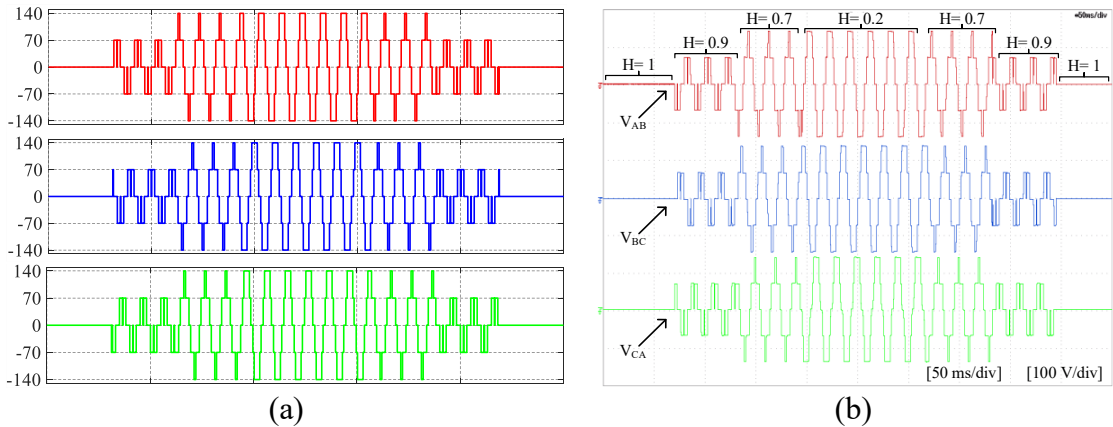|	LFM			LS-PWM			Phase voltage	
	V_{A0}	V_{B0}	V_{C0}	V_{A0}	V_{B0}	V_{C0}	LFM	LS-PWM
$A1$	$2E$	0	0	$2E$	0	0	$4/3E$	$4/3E$
$A2$	$2E$	E	0	$2E$	E	0	E	E
$A3$	$2E$	$2E$	0	$2E$	$2E$	0	$2/3E$	$2/3E$
$A4$	$-$	$-$	$-$	E	E	0	$-$	$1/3E$
$A5$	E	$2E$	0	E	$2E$	0	0	0
$A6$	$-$	$-$	$-$	E	$2E$	E	$-$	$-1/3E$
$A7$	0	$2E$	0	0	$2E$	0	$-2/3E$	$-2/3E$
$A8$	0	$2E$	E	0	$2E$	E	$-E$	$-E$
$A9$	0	$2E$	$2E$	0	$2E$	$2E$	$-4/3E$	$-4/3E$

Fig. 13. Line voltages V_{AB}, V_{BC}, and V_{CA} for different values of H. (a) Simulation. (b) Experimental.

Some selected results for the hybrid configuration of the proposed topology depicted in Fig. 3 are shown in Figs. 14, 15 and 16 when the fixed stage and one repeated module are used for feeding power to an R-L load (R=50 Ω, L=100 mH) under LFM and LS-PWM, respectively. By using one module cascaded with the fixed stage, seven levels of -2E, -E, 0, E, 2E, 3E, and 4E can be produced in the pole voltage V_{A0} while thirteen levels of -6E, -5E, -4E, -3E, -2E, -E, 0, E, 2E, 3E, 4E, 5E, and 6E are generated in the line voltage V_{AB}.
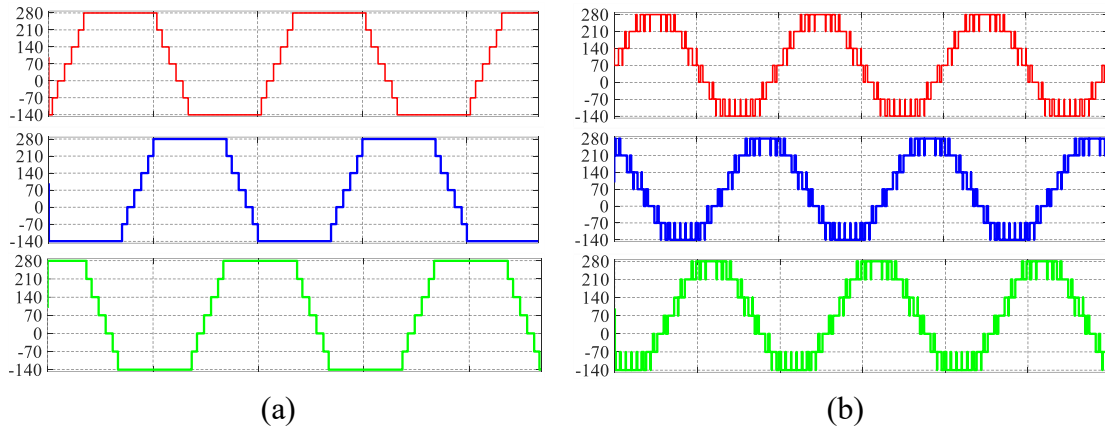

(a)	(b)

Fig. 14. Pole voltages V_{A0}, V_{B0}, and V_{C0}. (a) LFM. (b) LS-PWM.

(a)	(b)
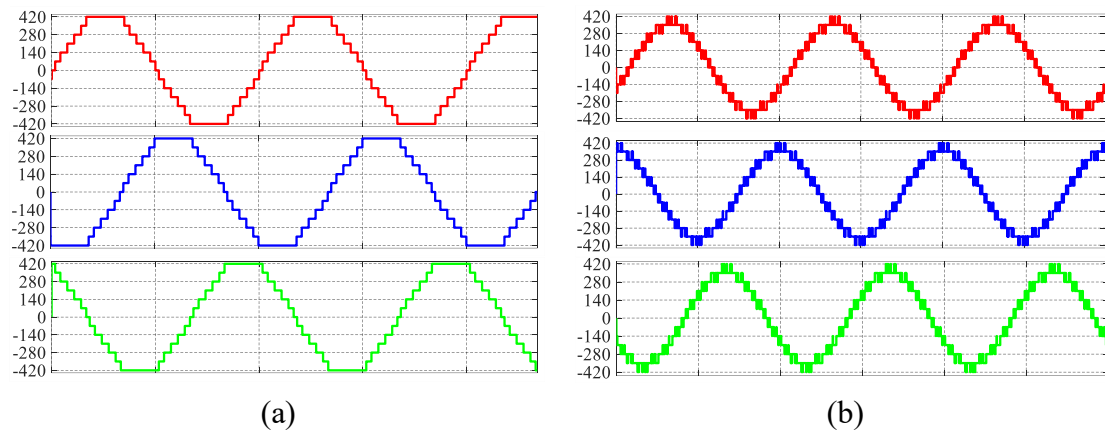
Fig. 15. Line voltages V_{AB}, V_{BC}, and V_{CA}. (a) LFM. (b) LS-PWM.

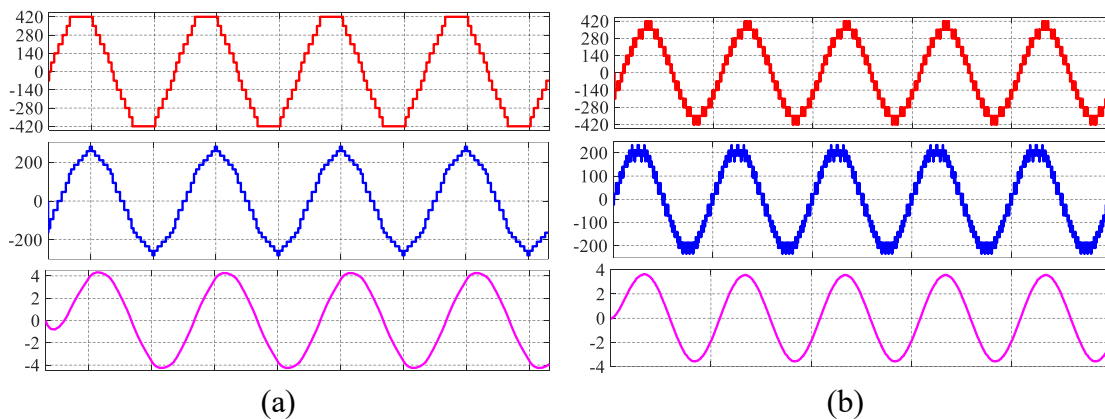|	
(a)	(b)

Fig. 16. Obtained waveforms of V_{AB}, V_{AN}, and I_A. (a) LFM. (b) LS-PWM.

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IV. POWER LOSSES AND EFFICIENCY ANALYSIS

The power losses in semiconductor devices are classified into three categories according to the operating state of the device: A) OFF-state losses, B) ON-state or conduction losses, and C) changing-state or switching losses [31-33]. Due to the nonideality characteristics of switches, a leakage current is following through switches during OFF-state, causing OFF-state power losses. The OFF-state losses can be neglected in most cases since leakage currents are insignificant during OFF-state [31]. During the ON-state, the switches have non-zero ON-state voltage (V_{on}) and ON-state resistance (R_{on}), causing power losses. The ON-state losses depend on V_{on}, R_{on}, load current and the switch duty cycle [33]. The transitions, from OFF- to ON states and vice versa, cannot occur instantaneously. In those transition periods, the flowing current and voltage across the device result in a large instantaneous loss or dissipated energies, which are termed as turn-on energy (E_{on}) and turn-off energy (E_{off}) for IGBTs, and reverse recovery energy (E_{rec}) for diodes. The switching losses are directly proportional to the switching frequency and blocking voltage of the devices [31, 32, 34]. More details on calculating the switching and conduction losses can be found in [31-34].

The efficiency of the proposed topology and the losses distribution in the switches are analysed based on a PSIM software model, considering the actual working condition of the IGBT modules. The required parameters of IGBTs are obtained from data sheets provided by component manufacturers. The IGBT modules are assumed to be working at a junction temperature of 150° C. Table V shows the system specifications and the parameters of used IGBT modules. The IGBT module has a part number of SKM300GA12E4, which is medium-fast trench IGBT in conjunction with a soft-switching controlled axial lifetime (CAL) freewheeling diode.

The loss distribution of different switches is shown in Fig. 17, where the losses are divided into conduction losses (P_{con}) and switching losses (P_{sw}). The conduction period and blocking voltage of the switch have the main effects on the conduction losses and switching losses when the switching frequency and load are kept constant ($Fs = 5$ kHz and $P_{out} = 4$ kW). For example, S_1, S_5, and S_9 have voltage stresses of $2E$, so their switching losses are higher than the other switches. On the other hand, S_2, S_6, and S_{10} have the highest conduction losses because their conduction durations are the longest among switches. Fig. 18 shows that the switching frequency significantly affects switching losses, but it has a small impact on the conduction losses.

The performance of the proposed topology is investigated by changing the switching frequency and load while keeping all other variables constant. Fig. 19 shows the efficiency variation when increasing the load from 10% to a full load of 4 kW in steps of 10% at the switching frequency of 5 kHz. The efficiency increases from 95.89% to 99.06% when the load is increased from 10% to 100% of the rated power. On the other hand, Fig. 19 also shows the effect of increasing the switching frequency from 1 kHz to 10 kHz on the converter efficiency at full load. The efficiency decreases from 99.35% at 1 kHz to 98.71% at 10 kHz.

TABLE V
SYSTEM SPECIFICATIONS FOR THE LOSS ANALYSIS

| Parameter/Specification	Value	Unit
Collector-emitter breakdown voltage (V_{CE})	1200	V
Collector-emitter on-state voltage ($V_{CE, on}$)	2.45	V
Collector-emitter voltage at zero current ($V_{CE, I=0}$)	0.8	V
IGBT on resistance ($R_{CE, on}$)	5.5	mΩ
Input capacitance (C_{ies})	17.6	nF
Output capacitance (C_{oes})	1.16	nF
Reverse transfer capacitance (C_{res})	0.94	nF
Turn-on delay time ($T_{d, on}$)	220	ns
Rise time (T_r)	51	ns
Turn-off delay time ($T_{d, off}$)	515	ns
Fall time (T_f)	105	ns
Turn-on switching energy (E_{on})	23.4	mJ
Turn-off switching energy (E_{off})	35	mJ
Reverse recovery energy (E_{rec})	22.2	mJ
Forward voltage (V_f)	2.42	V
Forward voltage at zero current (V_{f0})	1.1	V
Diode on-resistance (R_{on})	4.4	mΩ
Junction temperature (T_j)	150	°C
Switching frequency (F_s)	5	kHz
Modulation index (M_I)	0.9	-
Power factor (PF)	0.877	-
Input DC sources (E)	500	V
Rated output power (P_{out})	4	kW
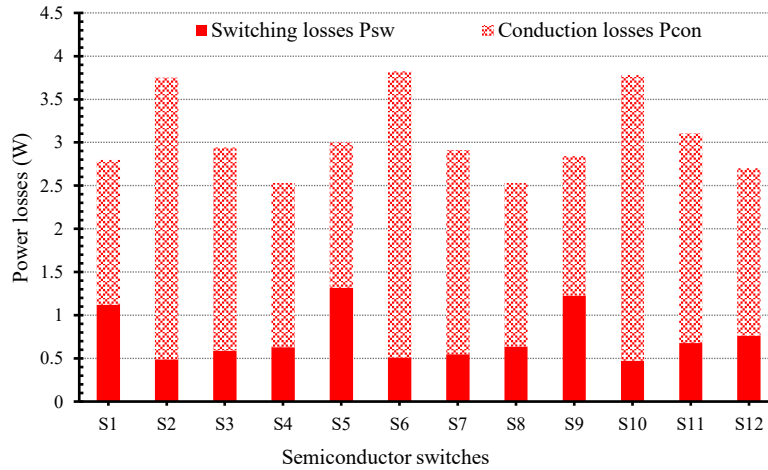
Fig. 17. Loss distribution in various switches at the rated power and switching frequency of 5 kHz.

V. THE COMPARATIVE STUDY

In this section, a comparison between the proposed topology and the recently reported multilevel topologies in [1-12] is carried out to highlight the key features of the proposed circuit. The compared topologies are labelled with T_A to T_S, which
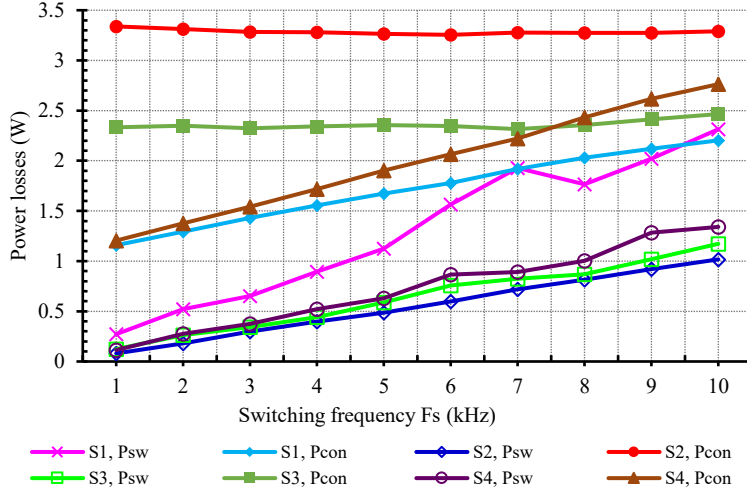
Fig. 18. Effects of switching frequency on the power losses of switches (phase A) at the rated power.
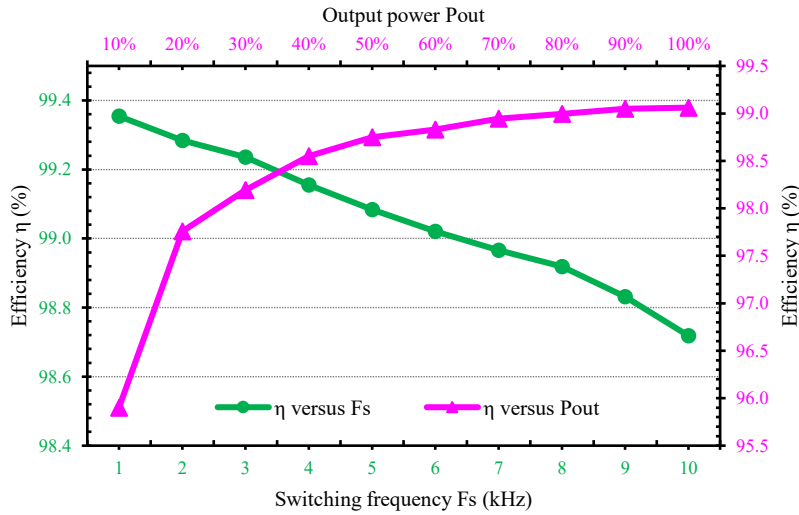

Fig. 19. Efficiency at different loads and switching frequencies.

are ordered in a descending manner in terms of the required number of components. Merits and demerits of each topology were discussed in Section I. Table VI lists the component counts for three-phase configuration of the addressed topologies, including DC source count N_{DC}, switch count N_{SW}, power diode count N_D, inductor count N_L, and capacitors count N_C. Further, 'component per level factor (CLF)' is used to calculate the required components for producing one voltage level [35].

Some assumptions are used in the comparison study: A) the number of levels N is equal to three for the pole voltage and five for the line voltage, B) all mentioned topologies are set to be in three-phase configurations, C) the unidirectional switch is the counting unit for switching devices, i.e. each bidirectional switch was disassembled into its primary parts, D) the built-in/freewheeling diodes are not included for calculating the diode count N_D, E) the coupled-inductor is counted as one inductor, F) the capacitor count N_C includes only the flying capacitors, while the DC-link capacitors for single-source MLIs are replaced by DC sources (i.e. the

DC-link structures are unified for all single-source MLI, in the form of two DC sources in series instead of one DC source divided by two capacitors into two equal parts).

TABLE VI

SUMMARY OF THE COMPARISON STUDY AMONG THE PROPOSED TOPOLOGY, THE MLIS IN [1-12] AND THE CONVENTIONAL MLIS IN TERMS OF COMPONENT COUNT AND DC-LINK VOLTAGE REQUIREMENTS

Topology	N_{DC}		N_{SW}				N_D		N_L	N_C	CLF
	E	**2E**	**0.5E**	**E**	**1.5E**	**2E**	**E**	**2E**		**E**	
T_A In [1]	0	3	0	3	0	6	12	0	0	6	10.0
T_B In [2]	1	1	4	1	3	6	12	0	0	0	9.3
T_C In [3]	3	0	0	18	0	0	3	0	0	0	8.0
T_D In [7]	2	0	0	3	0	6	12	0	0	0	7.7
T_E In [10]	1	1	0	6	0	3	3	6	3	0	7.7
T_F In [4]	3	0	0	18	0	0	0	0	0	0	7.0
T_G In [3]	3	0	0	18	0	0	0	0	0	0	7.0
T_H In [3]	3	0	0	15	0	0	3	0	0	0	7.0
T_I In [9]	2	0	0	18	0	0	0	0	0	0	6.7
T_J In [8]	2	0	0	12	0	6	0	0	0	0	6.7
T_K, NPC	2	0	0	12	0	0	6	0	0	0	6.7
T_L, CHHB	6	0	0	12	0	0	0	0	0	0	6.0
T_M In [5]	6	0	0	6	0	6	0	0	0	0	6.0
T_N, FCs	2	0	0	12	0	0	0	0	0	3	5.7
T_O In [6]	4	0	0	12	0	0	0	0	0	0	5.3
T_P, CHB	3	0	0	12	0	0	0	0	0	0	5.0
T_Q, T-type	2	0	0	6	0	6	0	0	0	0	4.7
T_R In [12]	2	0	0	9	0	3	0	0	0	0	4.7
T_S In [11]	1	1	0	6	0	6	0	0	0	0	4.7
The proposed topology	2	0	0	9	0	3	0	0	0	0	4.7

To make the comparison as fair as possible, the transferred power to the load must be equal in all compared topologies. This can be accomplished by generating the same voltage values across the connected load of each topology. The five voltage levels must have the same values for all circuits. For Example , -2E, E, 0, E, and 2E are selected to be the values of the five levels in the output voltage. Therefore, the values of the DC sources in the DC-link of some topologies are changed to generate the same output voltages.

According to Table VI, topologies T_Q-T_S are considered as the counterparts to the proposed topology in terms of component count. All of them require fourteen components to produce three voltage levels. However, the proposed topology has advantages of A) simpler DC-link requirements and lower high-voltage switches compared to topology T_S, B) higher count of low-voltage switches (9 instead of 6) and a 50% reduction of high voltage switches (3 instead of 6) compared to topology T_Q. Although the proposed topology and the topology T_R have the same advantages and disadvantages for three-level operations, the proposed topology is more advantageous for level counts more than three due to its merits of eliminating

flying capacitors, reaching to high voltages without output transformer, and simplifying control requirements (there is no need for voltage balancing algorithms or voltage sensors for controlling the voltages of the flying capacitors). From application point of view, the proposed topology is more advantageous in renewable energy systems, e.g. PV farms, or for low and high voltage applications, where several isolated DC sources are available. For example, when one module is used with the three-level fixed stage (i.e. six switches and DC sources more while saving three flying capacitors compared to T_R), the proposed topology generates seven, nine, eleven, and fifteen voltage levels for symmetrical and asymmetrical operation (DC voltage ratios are 1:1, 2:1, 1:2, and 1:3) while T_R generates five, seven, seven, and nine voltage levels with same DC voltage ratios.

VI. Conclusion

This paper presents and analyses a new three-phase multilevel topology, being applicable for both low-voltage and high-voltage applications. The key features of the proposed topology are numerically verified by simulation results and experimentally validated through an in-house laboratory prototype. The proposed topology is tested using a resistive-inductive load under low-frequency modulation and level-shifted pulse width modulation techniques. Further, the LFM is modified by integrating the proposed modulator H, enabling online control of the output voltage in terms of RMS value, frequency, and level count. Using similar building blocks in both configurations allows for reducing the time and cost of manufacturing, troubleshooting, voltage-level upgrading. A detailed comparison between the proposed topology and other recently developed MLIs in terms of component count and voltage ratings proves that the proposed topology avoids using of power diodes, inductors, and capacitors, resulting in a more compact design with a higher life-time, efficiency and simpler control algorithms.

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