Multilevel Inverters with Reduced Component Count for Energy Systems

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UiA University of Agder

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Summary

Multilevel inverters (MLIs) have gained increasing interest for advanced energy-conversion systems with a wide range of voltage levels, due to their attractive features of low harmonic contents, low dv/dt stress, low filtering requirements, low switching frequency, low electromagnetic interference (EMI), and employing low-rated semiconductor devices for producing high voltages. Further, some MLIs have a modularity feature, facilitating voltage and current scalability with high redundancy in switching states, allowing for fault-tolerant operations. The mentioned features are directly related to the number of generated voltage levels. However, enlarging level count renders challenges of requiring massive component counts, including DC sources, capacitors, power diodes, switches, inductors, and transformers. The high count of components negatively affects the size, cost, efficiency, lifespan, reliability, complexity of MLI-based energy conversion systems. Thus, proposing novel MLIs, which can enlarge the voltage level number with a low component count, is currently one of the most attractive topics in this research theme.

In this dissertation, four three-phase topologies are proposed to mitigate the aforementioned shortcomings. Two transformerless topologies are proposed for low- and medium voltage applications, while two transformer-based topologies are intended for medium- and high-voltage applications. The proposed topologies have the key features of being capacitor-, diode-free, and low counts of DC sources, switches, and transformers. Further, three of them have a high modularity degree, allowing for higher voltage operations without increasing the voltage stress across the switches. The working principle of the proposed topologies are theoretically demonstrated, numerically verified, and experimentally validated through an in-house experimental setup. The effectiveness of the proposed topologies is proven through detailed comparative studies regarding component counts and voltage ratings. The proposed topologies are briefly described in this dissertation, while detailed explanations and results can be found in the appended papers.

List of Publications

The following six papers have been published or submitted for publication in peer-reviewed journals and conference proceedings.

- A. Salem, H. V. Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Voltage source multilevel inverters with reduced device count: topological review and novel comparative factors," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2720-2747, 2021. doi: 10.1109/TPEL.2020.3011908.

- A. Salem, H. V. Khang, and K. G. Robbersmyr, "Four-level three-phase inverter with reduced component count for low and medium voltage applications," *IEEE Access,* vol. 9, pp. 35151-35163, 2021. doi: 10.1109/access.2021.3062110.

- A. Salem, H. V. Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Novel three-phase multi-level inverter with reduced components," in *Proc. 45th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2019, pp. 6501-6506. doi: 10.1109/IECON.2019.8927732.

- A. Salem, H. V. Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Novel three-phase multilevel inverter with reduced components for low- and high-voltage applications," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 7, pp. 5978-5989, 2021. doi: 10.1109/tie.2020.2998752.

- A. Salem, H. V. Khang, and K. G. Robbersmyr, "New multilevel inverter topology with reduced component count," in *Proc. 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1-P.8. doi: 10.23919/EPE.2019.8915400.

- A. Salem, H. V. Khang, I. N. Jiya, and K. G. Robbersmyr, "Hybrid three-phase transformer-based multilevel inverter with reduced component count," *Submitted to IEEE Journal of Emerging and Selected Topics in Power Electronics (Under review)*.

The following paper was written and submitted for publication during the time of the PhD project, but is not included in the dissertation.

- A. Salem, H. V. Khang, and K. G. Robbersmyr, “Novel transformer-based six-level inverter with low component count,” *accepted for publication in 23rd European Conference on Power Electronics and Applications (EPE '21 ECCE Europe)*, 2021, pp. xx-xx.

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List of Abbreviations and Symbols

2L-VSIs	two-level voltage source inverters
3L-HB	three-level H-bridge
3L-NPC	three-level NPC
3-PS	three-phase synthesizer stage
4L-ANPC	four-level active neutral point clamped
5L-CHB	five-level CHB
5L-HI	five-level hybrid inverter
APFs	active power filters
CEL	component for each level
CHB-MLI	cascaded H-bridge MLI
CLF	component per level factor
CMLI	cascaded MLI
CMV	common-mode voltage
CT-MLI	cascaded-transformer MLI
DT-type	dual T-type
EI	eighteen-step inverter
EMI	electromagnetic interference
FACTS	flexible AC transmission systems
FC-MLI	flying capacitor MLI
F_S	switching frequency
H	modulator signal
H9LI	hybrid nine-level inverter
HC-MLI	hybrid cascaded MLI
HVDC	high-voltage direct-current
IGBT	insulated-gate bipolar transistor
L	load inductor
LDUs	level doubling units
LFM	low-frequency modulation
LGS	level generator stage
LSPWM	level-shifted pulse width modulation
LSR	level-number per switch ratio
M	module count
MANPC	modified active-neutral point-clamped
MESs	modern energy systems
MI	modulation index
MLIs	multilevel inverters
MOSFET	metal-oxide-semiconductor field-effect transistor
MSC	multiple sources configuration

N	voltage level count
N_{Cap}	capacitor count
N_D	diode count
N_{DC}	DC source count
NE_C	equivalent number of capacitors
NE_{DC}	equivalent number of DC sources
NE_L	equivalent number of inductors
NE_{SEMI}	equivalent semiconductor count
NE_{Total}	total equivalent component count
NE_{Trf}	equivalent number of transformers
N_L	inductor count
NNPC	nested neutral-point-clamped
NPC-MLI	neutral point clamped MLI
NPPI	neutral-point-piloted inverter
N_{SE}	count of stored energy elements
N_{Trf}	transformer count
N_{Total}	total component count
NT-type	nested T-type
N_X	other component counts
P_{con}	conduction loss
PCS	polarity changer stage
PECs	power electronic converters
P_{out}	output power
PSPPs	pumped storage power plants
P_{sw}	switching loss
PV	photovoltaic
PWM	pulse width modulation
R	load resistor
RESs	renewable energy systems
R-L	resistive-inductive
RMS	root mean square
SE	stored energy
SEF	stored energy factor
SHE	selective harmonic elimination
SSC	single source configuration
STATCOMs	static synchronous compensators
T_A	proposed topology A
T_B	proposed topology B
T_C	proposed topology C
T_D	proposed topology D
TE	total stored energy
THD	total harmonic distortion

TSV	total standing voltage
TSV_{SEMI}	total standing voltage of semiconductor devices
T_x	exemplary topology
UPQCs	unified power quality conditioners
V_{BASE}	base value of the voltage
VFDs	variable frequency drives
VGS	voltage generator stage
VPK	peak voltage
SR_A	sinusoidal reference signal
VS-PSPPs	variable-speed pumped storage power plants
β	transformer turn ratio
η	efficiency

Chapter 1

Introduction

1.1 Background

Power electronic converters (PECs) allow for efficient power transfer in modern energy systems (MESs), for example, in renewable energy systems (RESs), adjustable speed drives, electric vehicles, and traction applications [1-3]. An essential stage in MESs is the inverter stage, converting the DC voltage to AC with a customized magnitude, frequency, and phase angle. For a long time, the conversion process has been managed by traditional two-level voltage source inverters (2L-VSIs) due to their merits in low-power applications. The key features of the 2L-VSIs include simple structure, low control requirements, low component count, and maturity. However adopting the 2L-VSIs in medium- and high-power applications renders challenges [2-4], which can be mainly summarized as follows: A) high harmonic contents, causing a poor power quality and requiring massive and expensive filters to meet the utility grid or customer standards, B) high power rating of the semiconductor switches, resulting in connecting strings of series and/or parallel devices to fulfil the required voltage and current capacities, limiting the maximum power to the available technologies, increasing power losses, and decreasing the system reliability. To overcome these challenges, multilevel inverters (MLIs) are considered as a favourite solution for medium- and high-power conversions [2-4].

1.2 Multilevel inverters

MLIs have been developed for more than five decades and gained popularity in energy systems and industrial applications as one of the most attractive solutions for implementing medium- and high-voltage DC-AC converters. The MLIs are configured by distinct arrangements of single or several DC sources, semiconductor switching devices, capacitors, inductors, and transformers, in a way

to produce a near sinusoid output voltage with low distortion as an example in Figure 1.1. In MLIs, combining low-voltage DC sources with passive and/or active component networks can efficiently generate high-voltage stepped waveforms at outputs. The rating of the components is defined by the linked DC sources rating, so their voltage rating is much lower than the output voltage [1-10].

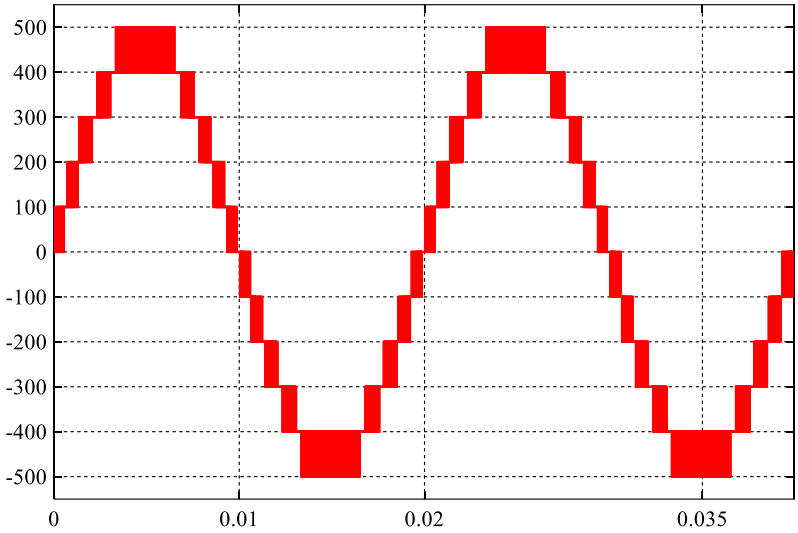
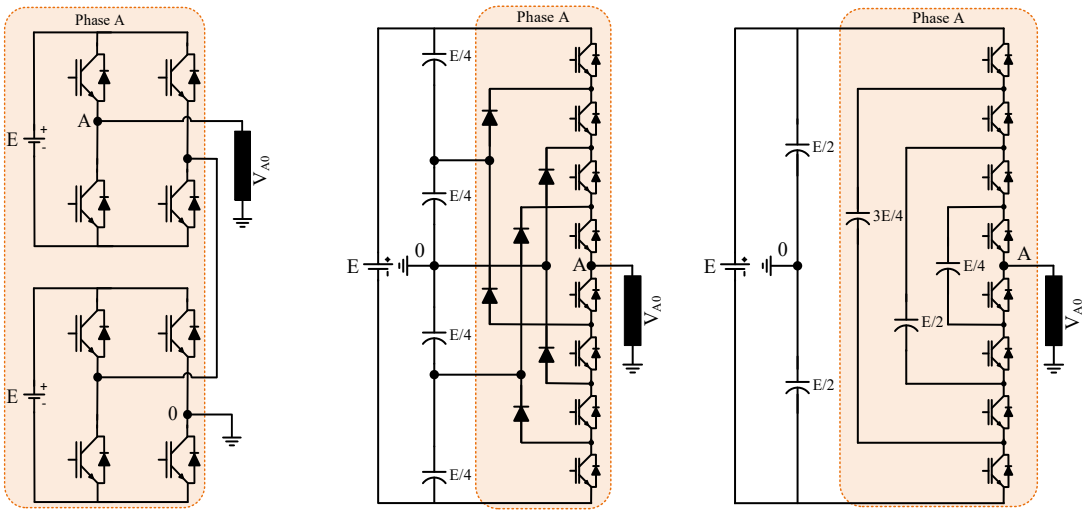


Figure 1.1: Typical eleven-level voltage waveform.

From the 1970s, Baker and Bannister in [11] have invented the first MLI topology, which is widely known as a cascaded H-bridge MLI (CHB-MLI), using several DC sources. Each source was linked to a single-phase inverter to form one cell. By connecting more cells in cascade, as shown in Figure 1.2 (a), a multilevel output can be achieved. A few years later, in the 1980s, a single source MLI topology called diode clamped or neutral point clamped MLI (NPC-MLI) has been proposed by Baker in [12]. Despite using one DC source, it requires several diodes connected to a neutral point, as shown in Figure 1.2 (b). In 1981, Nabae et al. in [13] presented the NPC-MLI implementation using the pulse width modulation (PWM) scheme. Figure 1.2 (c) shows the capacitor-clamped or flying capacitor MLI (FC-MLI), being introduced during the 1990s in [14] and [15] by Meynard et al. and Lavieville et al., respectively. Although it needs only one DC source, using several flying capacitors results in increasing both the size and control complexity. These three topologies, namely CHB-MLI, NPC-MLI, and FC-MLI, are considered as the basic MLI topologies in literature.

The MLI-based conversion systems have several attractive merits, as reported in [1-10], being favourite in medium- and high-power DC-AC conversions. Their key merits include:



(a) (b) (c)

Figure 1.2: Five-level configuration of the basic MLI topologies (phase A). (a) CHB-MLI. (b) NPC-MLI. (c) FC-MLI.

A) producing staircase waveforms with low harmonic contents and low dv/dt stress, significantly reducing the total harmonic distortion (THD), filter dimensions, and electromagnetic interference (EMI).

B) using low-rated semiconductor devices for producing high voltages without connecting them in a series/parallel manner as in two-level medium-power inverters.

C) switching at low frequency, reducing switching losses, being beneficial for efficiency and cooling requirements, especially in high-power applications.

D) having low common-mode voltage (CMV), being favourite in many applications. For example, in motor drives, the stress in the bearings can be reduced when motors are connected to MLI-based drive systems.

Moreover, the modularity feature of several MLIs allows for voltage and current scalability with high redundancy in switching states that make fault-tolerant operation more efficient. Due to these beneficial features, the MLIs are widely used in power systems, transportation, and RESs, for example, in flexible AC transmission systems (FACTS) [16, 17], high-voltage direct-current (HVDC) power transfer [18-20], active power filters (APFs) [21, 22], variable frequency drives (VFDs) [23-26], pumped storage power plants (PSPPs) [27-29] and grid-connected or standalone photovoltaic (PV) systems [30-32]. On the other hand, the MLI merits come with the cost of high numbers of passive and active components, such as DC sources, flying capacitors, inductors, transformers, diodes, and switches. Consequently, the converter volume, cost, complexity, losses, and failure

rate are increased. Thus, proposing new MLIs, that can enlarge the level number along with a low component count, is currently one of the most important topics in this research theme [1-10].

1.3 Motivation and research problem

More advanced power converters are significantly important for modernizing power generation, transmission, and distribution to achieve better operations, controls and power managements, for example, in large-scale PV power plants, adjustable-speed wind turbines, variable-speed PSPPs (VS-PSPPs), HVDC power transfer, static synchronous compensators (STATCOMs), unified power quality conditioners (UPQCs), and electric propulsion systems for electric trains and ships [1, 2, 4, 9, 19, 22, 25, 27, 30]. MLIs have been introduced as promising alternatives in the mentioned applications and more because of their unique features as mentioned above [2, 3]. However, MLIs have two correlated drawbacks: high component count and control complexity. The component nature and count are the core problem in MLIs, while the control complexity and other demerits are the consequences. These drawbacks motivate researchers in academia and industry to propose reduced component circuits to overcome the MLI drawbacks.

To further improve the existing MLIs, this work aims to mitigate the aforementioned limitations by proposing novel MLI topologies with reduced component count and enhanced features. From application point of view, the proposed topologies are mainly recommended for low- and medium-voltage applications, while some of them are more suitable for medium- and high-voltage power conversions, covering a wider range of operation voltage. In terms of structure point of view, both transformer-based and transformerless topologies are studied to fulfil the galvanic isolation and/or high-power density requirements. Further, the proposed topologies usually utilize a single DC-link for industrial applications, but some of them employ several DC-link ports, being suitable for renewable energy. The proposed topologies do not need any clamping diode or flying capacitor.

1.4 Scientific contributions of the dissertation

The scientific contributions of this dissertation are highlighted based on three published IEEE journal papers, two published conference papers, and one under-review journal paper.

Paper I: Voltage source multilevel inverters with reduced device count: topological review and novel comparative factors

Summary: This paper updates and summarizes the recently developed MLI topologies with a reduced component count, based on their advantages, disadvantages, construction, and specific applications. Within the framework, both single-phase and three-phase topologies with symmetrical and asymmetrical operations are considered via a detailed comparison in terms of component count and type. Unlike the existing reviews focusing on a specific application, this work reviews diverse MLI topologies in a wide range of applications. Further, a comparative method with novel factors to take component ratings into account is proposed in this paper. Selected topologies are compared using both the existing and proposed comparative factors, verifying the effectiveness of the proposed method.

Contributions: A comprehensive review study for the most promising MLI topologies in terms of construction, salient features and limitations is presented to give guidelines to further improve the current topologies more efficiently. Moreover, novel comparative factors, namely component for each level (*CEL*) and stored energy factor (*SEF*), are introduced to evaluate different topologies more effectively.

This paper has been published as:

A. Salem, H. V. Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Voltage source multilevel inverters with reduced device count: topological review and novel comparative factors," *IEEE Transactions on Power Electronics,* vol. 36, no. 3, pp. 2720-2747, 2021. doi: 10.1109/TPEL.2020.3011908.

Paper II: Four-level three-phase inverter with reduced component count for low and medium voltage applications

Summary: Paper II proposes a novel four-level inverter topology with a reduced component count for low- and medium-voltage energy systems. It requires three bidirectional switches and twelve unidirectional switches without using flying capacitors, transformers, inductors, or clamping diodes, reducing the size, cost, and losses. Removing flying capacitors, inductors, and clamping diodes allows it to simplify control algorithms and increase the inverter reliability, efficiency, and lifetime. Depending on the availability of the DC sources or applications, the DC-

link of the proposed topology has two configurations: (A) multiple sources configuration (MSC), recommended for energy systems, (B) single source configuration (SSC), recommended for industrial applications. A modified LFM scheme is developed and implemented on the proposed topology to produce a staircase voltage with four steps. Further, a LSPWM scheme is used to reduce the filter size and increase the output voltage controllability. Moreover, a voltage balancing control algorithm is executed to balance the DC-link capacitor voltages. The performance of the proposed topology is numerically demonstrated and experimentally validated on an in-house test setup. Within the framework, the power loss distribution in switches and conversion efficiency of the proposed circuit are studied, and its main features against counterparts are highlighted.

Contributions: A novel four-level inverter topology with a reduced component count, being attractive in low- and medium-voltage applications, is proposed and experimentally validated. Its superior features are highlighted through a detailed analysis.

This paper has been published as:

A. Salem, H. V. Khang, and K. G. Robbersmyr, "Four-level three-phase inverter with reduced component count for low and medium voltage applications," *IEEE Access,* vol. 9, pp. 35151-35163, 2021. doi: 10.1109/access.2021.3062110.

Paper III: Novel three-phase multi-level inverter with reduced components

Summary: In paper III, preliminary analysis and results of a new MLI topology are provided, while the full analysis is presented in paper IV. The proposed topology does not require transformers or electrolytic capacitors in its operation, making it compact and suitable in portable converters with a reduced size. It is a capacitor-, inductor-, and diode-free configuration, reducing the converter footprint, increasing the lifetime, and simplifying the control strategy. Further, low power losses are expected in the proposed circuit due to using low switching devices, operating at low frequencies instead of using hybrid designs based on switches and diodes. Some preliminary simulation results for the low-voltage configuration of the proposed topology are provided for different modulation strategies to verify its working principle. The introduced configuration in paper III is suitable for low-voltage applications, while the high-voltage version is proposed in paper IV.

Contributions: A new three-phase transformerless MLI is proposed and numerically verified through simulation results. It is recommended for low-voltage applications, where the low component count and compact design are more important than isolation between source and load.

This paper has been published as:

A. Salem, H. V. Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Novel three-phase multi-level inverter with reduced components," in *Proc. 45th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2019, pp. 6501-6506. doi: 10.1109/IECON.2019.8927732.

Paper IV: Novel three-phase multilevel inverter with reduced components for low- and high-voltage applications

Summary: Paper IV details the low-voltage configuration of the introduced topology in paper III and presents a new *N*-level hybrid configuration for high-voltage applications. It comprises a three-level fixed stage connected to several repeated cells, enlarging the output voltage level count, and enabling medium-, and high-voltage operations without increasing the voltage stress. Within the study, the switching algorithm for the LFM scheme is modified to control the RMS value, level count, and frequency of the output voltage online. Further, the overall efficiency of the topology and loss distribution in switches are studied. Within this framework, additional simulation results are presented for both configurations, and the low-voltage configuration is experimentally validated through an in-house test setup.

Contributions: A novel hybrid three-phase *N*-level inverter topology is presented for both medium- and high-voltage applications. Further, the LFM in paper III is improved by integrating the proposed modulator *H*, enabling online control of the output voltage in terms of RMS value, frequency, and voltage level count. The proposed circuit is numerically verified and experimentally validated through a scaled setup.

This paper has been published as:

A. Salem, H. V. Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Novel three-phase multilevel inverter with reduced components for low- and high-voltage applications," *IEEE Transactions on Industrial Electronics,* vol. 68, no. 7, pp. 5978-5989, 2021. doi: 10.1109/tie.2020.2998752.

Paper V: New multilevel inverter topology with reduced component count

Summary: Paper V introduces a new transformer-based MLI topology with a reduced component count. It can operate with symmetrical or asymmetrical DC voltage sources, and can be extended to produce higher voltage levels without increasing the switches blocking voltage, allowing it to fit well in medium- and high-voltage applications. The key features of the proposed topology include reduced component counts, structure simplicity, isolation feature, and modularity. The proposed topology is recommended to be used in PV-based energy systems, where the galvanic isolation feature is appreciated, and the availability of DC voltage sources is guaranteed. Two switching schemes control the output voltage of the proposed topology: low-frequency modulation (LFM) and level-shifted pulse width modulation (LSPWM). Selected simulation and experimental results were provided to validate the effectiveness of the proposed circuit under different modulation schemes and load conditions.

Contributions: A new reduced-component transformer-based MLI topology for PV-based energy systems and other medium- and high-voltage applications is proposed and validated in the in-house experimental setup.

This paper has been published as:

A. Salem, H. V. Khang, and K. G. Robbersmyr, "New multilevel inverter topology with reduced component count," in *Proc. 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1-P.8. doi: 10.23919/EPE.2019.8915400.

Paper VI: Hybrid three-phase transformer-based multilevel inverter with reduced component count

Summary: This paper proposes a novel three-phase transformer-based topology to maximize the output voltage levels while reducing component counts as compared to counterparts. The proposed hybrid topology is formed by connecting a T-type module with several three-level H-bridge (3L-HB) cells through single-phase transformers. The T-type module is fixed, while the 3L-HB cell can be repeated for enlarging the output voltage levels. The proposed topology features include low part count, capacitor-free, diode-free, voltage boosting, simple control, and modularity. Further, the proposed circuit allows for increasing the voltage level count without increasing the voltage stress across the switches, being a

promising candidate for high-voltage applications. The working principle of the proposed topology was theoretically demonstrated, numerically verified, and experimentally validated through the in-house setup.

Contributions: A novel three-phase transformer-based MLI topology is proposed and experimentally validated. The proposed circuit can reduce the total part count while preserving the key features of being capacitor-, diode-free, and low counts of DC sources, switches, and transformers.

This paper has been submitted as:

A. Salem, H. V. Khang, I. N. Jiya, and K. G. Robbersmyr, "Hybrid three-phase transformer-based multilevel inverter with reduced component count," *Submitted to IEEE Journal of Emerging and Selected Topics in Power Electronics (Under review)*.

1.5 Dissertation structure

The dissertation consists of five chapters and outlined as follows:

Chapter 1: Introduction

This chapter provides a brief introduction about MLIs, motivation and research problem, dissertation contributions, and dissertation structure.

Chapter 2: State-of-the-art

This chapter presents a review study for the recently developed three-phase MLI topologies in terms of construction, salient features, and limitations, highlighting the current challenges and research gaps in the MLI-based converters. The comprehensive review of MLIs in paper I is considered as a base for this chapter.

Chapter 3: Novel multilevel inverter topologies

This chapter introduces and discusses the circuit configurations, working principles, and switching strategies of the proposed topologies in papers II-VI.

Chapter 4: Results and discussions

This chapter presents brief results and findings withdrawn from papers II-VI, in which the operability and performance of the proposed topologies are numerically verified and experimentally validated through in-house

laboratory prototypes. Further, their key features are highlighted by comparative studies.

Chapter 5: Concluding remarks

This chapter summarizes the work conclusions, limitations, and future possibilities for improvements.

Chapter 2

State-of-the-art

This chapter reviews some of the recently developed MLI topologies with a reduced component count based on their construction, salient features, and limitations. The reported topologies represent diverse families of MLIs, such as single source, multiple sources, transformer-based, and inductor-based MLIs. Further, a comparative method with novel factors is proposed to take component ratings into account when comparing different MLI topologies.

2.1 Multilevel inverter overview

Over the past few years, proposing new MLIs with a lower component count has been one of the most attractive power electronics topics [4, 33]. Within the theme, improving efficiency, power density, control simplicity, reliability, cost, and broadening MLIs applications have attracted a large number of publications every year. Accordingly, reviewing the recent advanced knowledge in this research field periodically is always of importance to update the research baselines or the newest reflections, resulting in many review studies presented in [3-10, 20, 23, 33-35]. Most of those studies give a detailed review of MLIs based on a specific application or inverter family, e.g. transportation [9], medium-voltage drive systems [23], modular MLIs [3, 8-10, 34], HVDC applications [20], and renewable energy integration [4]. Moreover, in the literature, there are two comparative factors for assessing the developed topologies in terms of component counts [36, 37], namely the level-number per switch ratio (*LSR*) and component per level factor (*CLF*). However, *LSR* and *CLF* are not able to take component ratings or cost into consideration. Accordingly, a more comprehensive review of diverse MLI topologies in a wide range of applications is necessary to give readers a full picture of MLIs in different areas, not just focusing on a narrow application or inverter family.

Paper I can overcome these limitations by reviewing the promising MLI topologies with higher structure and application diversity than other existing review studies. Further, two novel comparative factors, namely component for each level (*CEL*) and stored energy factor (*SEF*) are introduced to consider component ratings. Figures 2.1 and 2.2 show selected topologies to represent some of the inverter families in paper I. More details can be found in paper I regarding the advantages, disadvantages, and construction of these topologies and other circuits.

For single-phase applications, Figures 2.1 (a)-(f) show inductor-based MLI [38, 39], unipolar MLI with a polarity changer [40], transformer-based MLI [41], QZS-based MLI [42], FC-based MLI [43], and cross-switched MLI [44], each subfigure shows one representative of each family. Further, Figures 2.2 (a)-(d) show

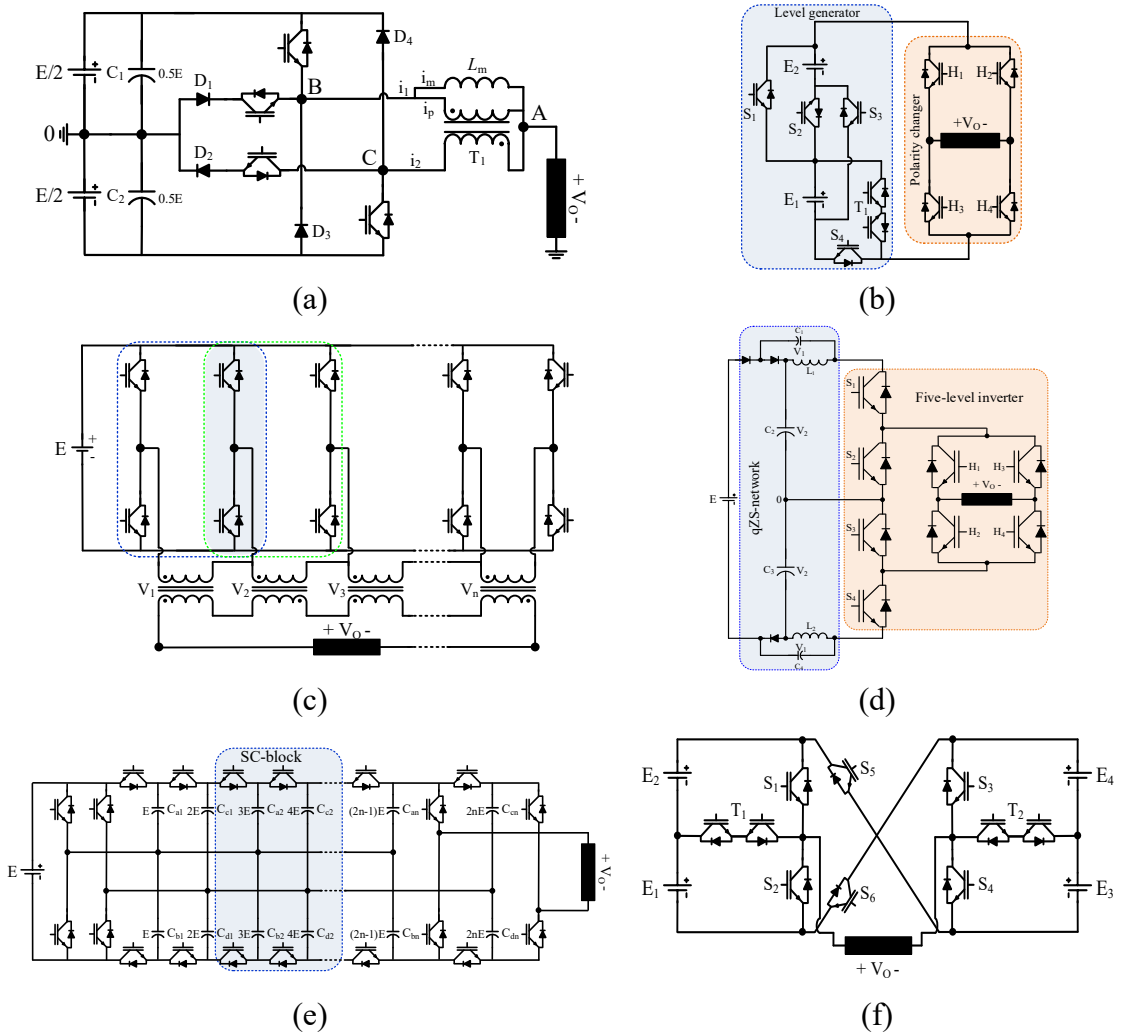


Figure 2.1: Single-phase MLIs belong to different MLI families. (a) Inductor-based MLI [38, 39]. (b) Unipolar MLI with a polarity changer [40]. (c) Transformer-based MLI [41]. (d) QZS-based MLI [42]. (e) Flying-capacitor-clamped MLI [43]. (f) Cross-switched MLI [44].

different three-phase circuits that include voltage-boosting single-stage MLI [45], nested neutral-point-clamped (NNPC) MLI for medium-voltage applications [46], hybrid MLI for high-speed drives [47], and transformer-based MLI used in STATCOMs for improving power quality [48].

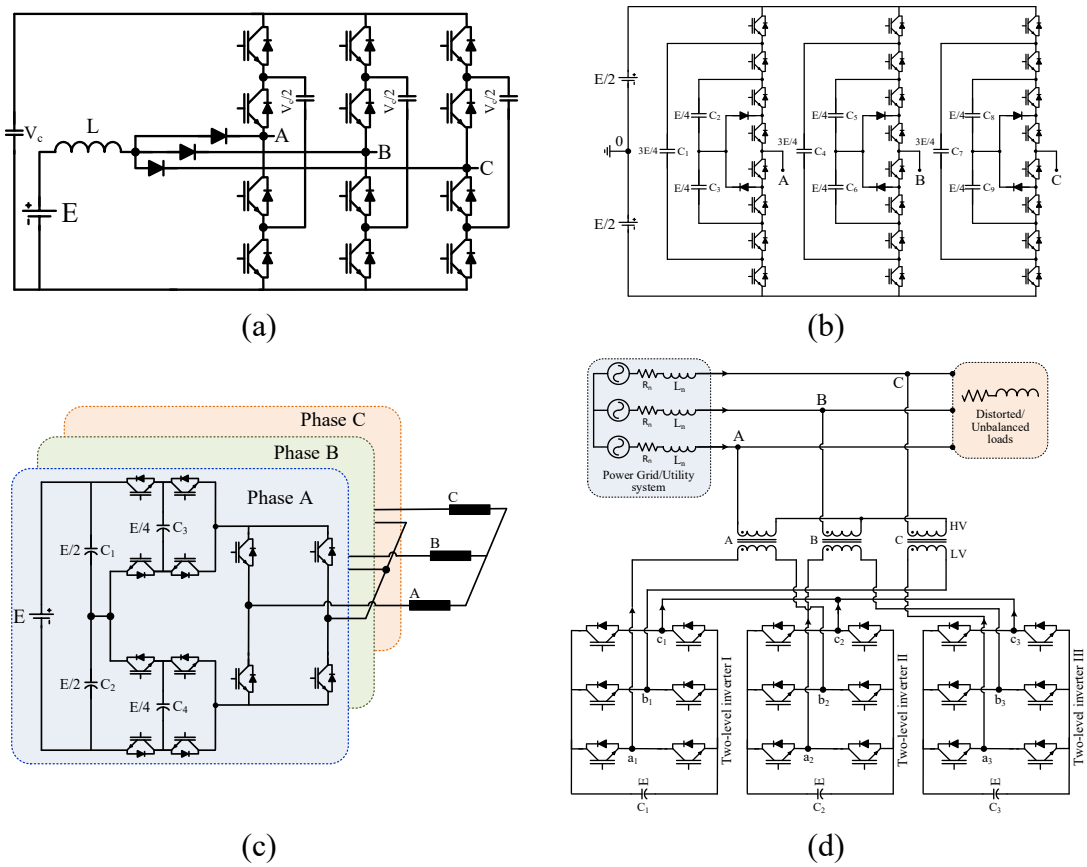


Figure 2.2: Three-phase MLIs belong to different MLI families. (a) Single-stage MLI with boosting capability [45]. (b) Nested neutral point-clamped MLI for medium-voltage applications [46]. (c) Hybrid MLI for high-speed motor drives [47]. (d) Transformer-based MLI used in STATCOM [28].

The topologies in Figures 2.1 and 2.2 show the diversity of the recently developed MLIs in structure and features, providing end-users with more varieties to fulfil their needs. However, selecting the best one is always a challenge since different aspects are considered, for example, low semiconductor count, low passive elements, isolation feature, boosting ability, modularity, etc. To make the comparative process easier and more efficient for both industry and academia, two strategies have been presented in [36, 37]. The strategy in [36] is based on *LSR* for comparing different MLIs. As described in (2.1), the *LSR* is calculated by the number of levels N over the switch count N_{SW}, indicating number of levels generated by each switch. Accordingly, topologies with higher *LSR* are better than those with a lower one from the switch count point of view.

$$LSR = \frac{N}{N_{SW}} \tag{2.1}$$

LSR cannot figure out other component counts, e.g., capacitors N_{Cap}, inductors N_L, diodes N_D, transformers N_{Trf}, DC sources N_{DC}, and other components N_X. To overcome this drawback, the *CLF* was proposed in [37] as a comparative factor. Instead of counting only switches, *CLF* is to count all the used components for producing one level, as calculated in (2.2). Therefore, it can be used to compare MLI topologies by the total component count. A reduced component circuit has a lower *CLF*.

$$CLF = \frac{N_{Cap} + N_D + N_L + N_{SW} + N_{DC} + N_{Trf} + N_X}{N} \tag{2.2}$$

According to (2.2), the drawbacks of using *LSR* for comparing MLIs have been solved by *CLF*. However, component ratings have been ignored when computing *CLF* values since the *CLF* alone cannot consider the component ratings. One device with a voltage rating of E has been equally counted as a device with a voltage rating of $0.5E$. Therefore, paper I proposes new factors to take component ratings into consideration. In the proposed method, the components are subdivided into two groups: semiconductor and passive elements. The semiconductor group includes switches and diodes, while capacitors, inductors, and transformers are classified as passive elements. Second, for simplicity, the peak current passing through each component is assumed to equal the load current, so the peak voltage *VPK* is considered as an indicator for the rating of a component. The rating of each component is merged with its count to produce one number, reflecting both count and rating of a similar component group. For example, the DC sources count N_D is merged with their ratings to be "equivalent number of DC sources NE_{DC}".

For calculating the equivalent semiconductor count NE_{SEMI}, the total standing voltage TSV_{SEMI} for NE_{SEMI} elements is calculated as in (2.3). Afterwards, NE_{SEMI} is defined by TSV_{SEMI} and the base value of the voltage V_{BASE} in (2.4). The equivalent numbers of capacitors NE_C, inductors NE_L, transformers NE_{Trf}, and DC sources NE_{DC} are calculated by (2.5)-(2.8), respectively. For example, if an exemplary topology T_X requires two DC sources of E and $2E$ volt, the number of DC sources N_{DC} is 2, while the equivalent number NE_{DC} is equal to three or $(E+2E)/E$. The same rule can be applied to the rest of the used components. The total equivalent component count NE_{Total} and *CEL* are defined by (2.9) and (2.10), respectively.

$$TSV_{\text{SEMI}} = \sum_{i=1}^{N_{\text{SW}}+N_{\text{D}}} VPK_{\text{i}} \tag{2.3}$$

$$NE_{\text{SEMI}} = \frac{TSV_{\text{SEMI}}}{V_{\text{BASE}}} \tag{2.4}$$

$$NE_{\text{C}} = \frac{\sum_{i=1}^{N_{\text{Cap}}} VPK_{\text{i}}}{V_{\text{BASE}}} \tag{2.5}$$

$$NE_{\text{L}} = \frac{\sum_{i=1}^{N_{\text{L}}} VPK_{\text{i}}}{V_{\text{BASE}}} \tag{2.6}$$

$$NE_{\text{Trf}} = \frac{\sum_{i=1}^{N_{\text{Trf}}} VPK_{\text{i}}}{V_{\text{BASE}}} \tag{2.7}$$

$$NE_{\text{DC}} = \frac{\sum_{i=1}^{N_{\text{DC}}} VPK_{\text{i}}}{V_{\text{BASE}}} \tag{2.8}$$

$$NE_{\text{Total}} = NE_{\text{SEMI}} + NE_{\text{C}} + NE_{\text{L}} + NE_{\text{Trf}} + NE_{\text{DC}} \tag{2.9}$$

$$CEL = \frac{NE_{\text{Total}}}{N} \tag{2.10}$$

To verify the effectiveness of the proposed factor *CEL* over the existing factor in ranking MLIs, a five-level hybrid inverter (5L-HI) in [49] is compared to the traditional five-level CHB (5L-CHB). A fair comparison can be achieved because both number and value of the output voltage levels are the same (i.e., five levels of -0.25*E*, -0.5*E*, 0, 0.25*E*, and 0.5*E*). Figure 2.3 shows the 5L-HI circuit, which is selected as an example to clarify the *CEL* calculation. It requires eight switches with a voltage rating of 0.25*E* and twelve switches with 0.5*E*, in addition to six diodes with a rating of 0.5*E* and two 0.25*E* capacitors. For calculating the equivalent semiconductor count, NE_{SEMI}, first (2.3) is used for obtaining the TSV_{SEMI} value, and then (2.4) is used to define NE_{SEMI}. TSV_{SEMI} is 11*E* or 8(*E*/4)+12(*E*/2)+6(*E*/2), so the value of NE_{SEMI} is 11. Using (2.5) and (2.8), NE_{C} and NE_{DC} can be calculated as ((0.25*E*+025*E*)/*E*) and ((0.5*E*+05*E*)/*E*), respectively. Using (2.9) and the obtained values of NE_{SEMI}, NE_{DC} and NE_{C}, results

in the total component count of 12.5. Finally, *CEL* of 2.5 is calculated by using (2.10). For the 5L-CHB, the same procedure can be repeated. In Table 2.1, the differences between the existing method and the proposed one can be well observed. For example, in 5L-HI, the *CLF* factor results in the total component count (N_{Total}) of 30 regardless of their voltage rating, while NE_{Total} is only 12.5 when using *CEL* factor. Without considering the component voltage rating or based on *CLF* values alone, both 5L-CHB and 5L-HI require the same component count. However, when considering the voltage rating by the proposed indicator *CEL*, the total equivalent component count of the 5L-CHB is lower than that of 5L-HI since the *CEL* of 5L-CHB is smaller than that of 5L-HI.

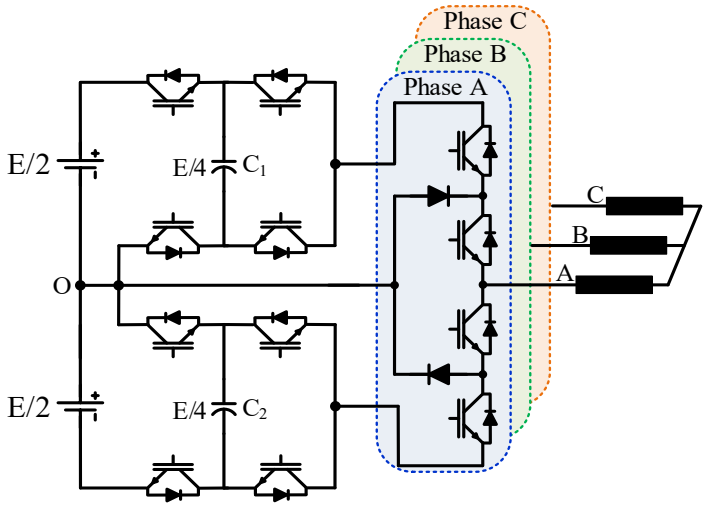


Figure 2.3: Circuit configuration of the five-level hybrid inverter [49].

Table 2.1: Using *CLF* and *CEL* for comparing 5L-HI [49] and 5L-CHB.

Topology	**DC sources**		**Switches**		**Diodes**	**Capacitors**	**Existing method**		**Proposed method**	
	***E*/4**	***E*/2**	***E*/4**	***E*/2**	***E*/2**	***E*/4**	N_{Total}	***CLF***	NE_{Total}	***CEL***
5L-HI, [49]	0	2	8	12	6	2	30	6	12.5	2.5
5L-CHB	6	0	24	0	0	0	30	6	7.5	1.5

The passive elements in the MLI topologies, such as capacitors and inductors, have distinctive natures as compared to other components since they store energy either in magnetic or electric fields. An additional comparative factor, namely *SEF*, is proposed to take their stored energy *SE* into consideration when comparing topologies besides their equivalent numbers. The total stored energy *TE* of stored energy elements N_{SE} is calculated in (2.11) and used to obtain the proposed *SEF* in (2.12).

$$TE = \sum_{i=1}^{N_{SE}} SE_i \tag{2.11}$$

$$SEF = \frac{TE}{TE_{BASE}} \tag{2.12}$$

where SE_i is the stored energy in a passive element i in a topology. TE_{BASE} is the total stored energy base value. The value of the TE_{BASE} can be the total stored energy of an interested or proposed topology. The *SEF* can be calculated for different stored energy elements in a compared topology *T*x, indicating the stored energy in percentage. For example, two MLI topologies T_1 and T_2 use capacitors. T_1 has two capacitors of 1 mF with the voltage rating of 100 V, while T_2 has three capacitors (two of 0.25 mF and one of 0.5 mF), and all the capacitors have the voltage rating of 75 V. The equivalent count of the capacitors is defined by (2.5), and their *SEFs* are calculated by (2.11) and (2.12). The equivalent capacitor counts of T_1 and T_2 are 2 and 2.25, respectively (V_{BASE} is selected at 100 V). The *SEFs*[1] of T_1 and T_2 are 1 and 0.28, respectively. Although the topology T_2 requires a higher equivalent capacitor count than T_1, the capacitors in T_2 store 28.1% of the stored energy in T_1, affecting the cost and size of the capacitors. It is worth mentioning that the same procedure can be applied to inductors as well.

Each topology should be evaluated by some of the proposed factors, i.e., NE_{SEMI}, NE_{DC}, NE_C, NE_L, NE_{Trf}, *SEF*, and *CEL*, to highlight its merits, allowing for finding the most suitable application. For example, in PV farms, NE_{DC} is less important than that in motor drives, while NE_C, NE_L, NE_{Trf}, and *SEF* should be reduced for more compact designs. For control simplicity, NE_{SEMI} and NE_C have salient effects as compared to other factors. Finally, the *CEL* factor indicates the advantage of having low-rated components in a topology regardless of other features. It is worth mentioning that the proposed factors do not reflect the required component count, but it produces numbers based on the count and rating of the components.

2.2 Three-phase MLIs

This section summarizes some of the promising three-phase MLI topologies for energy systems and motor drives. They are classified according to their recommended operating voltage or structure into three groups: A) low- and

[1] The total stored energy *TE* of T_1 is ($2 \times 0.5 \times 1e^{-3} \times 100^2$) and it is ($2 \times 0.5 \times 0.25e^{-3} \times 75^2$) + ($0.5 \times 0.5e^{-3} \times 75^2$) for T_2. TE_{BASE} is selected to be the stored energy of T_1.

medium-voltage MLIs, B) high-voltage MLIs, and C) transformer-based MLIs. This classification is made according to their merits, demerits, or recommended by the view of authors.

2.2.1 Low- and medium-voltage MLIs

T-type inverter or neutral-point-piloted inverter (NPPI) is considered as one of the most popular three-level topologies in low- and medium-voltage applications [50-52]. A single-phase T-type inverter was patented by Conergy in [53], and the authors in [54] presented the three-phase T-type configuration. Figure 2.4 (a) shows the three-phase T-type inverter, consisting of a conventional 2L-VSI combined with three branches of bidirectional switches, being assumed as a common-emitter configuration. Each branch connects the midpoint of the DC-link to one leg of the 2L-VSI, forming a T-type shape. The six switches of the 2L-VSI (S_1-S_6) are rated at the input voltage E, while the remaining switches have the voltage rating of $0.5E$. One counterpart to the T-type MLI is NPC-MLI, which is shown in Figure 2.4 (b). It requires six clamping diodes, while the T-type uses six switches instead. Both of them use a single DC source, two capacitors, and twelve switches to produce three voltage levels. Due to the lower count of power electronics components in the current paths, the T-type MLI has a lower conduction loss than NPC-MLI. For example, any positive or negative voltage level in the T-type inverter needs only one switch in the current path, while two switches are required in NPC-MLI regardless of the voltage level. However, the switching loss in NPC-MLI is lower than that in T-type inverter because of having lower voltage stresses than those in the unidirectional switches of T-type MLI. Accordingly, the T-type MLI is more advantageous in applications that require low switching frequencies [51].

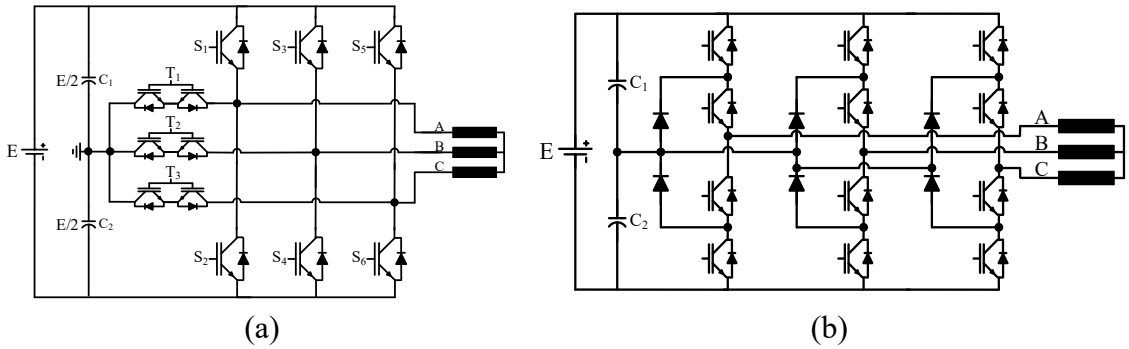


Figure 2.4: Three-phase circuits in [52, 55] (a) T-type MLI [52]. (b) Three-level NPC inverter [55].

Due to their maturity, low component counts, and market availability, many new topologies use either T-type or NPC-MLI as a stage in their structures [56-59]. Figure 2.5 shows some of them, being detailed in paper I. On the other hand, 50% of employed switches in the T-type inverter must withstand the full DC-link voltage, and many clamped diodes in the NPC-MLI inverter are the main drawbacks. These drawbacks are transferred to the new MLIs based on either T-type or NPC-MLI.

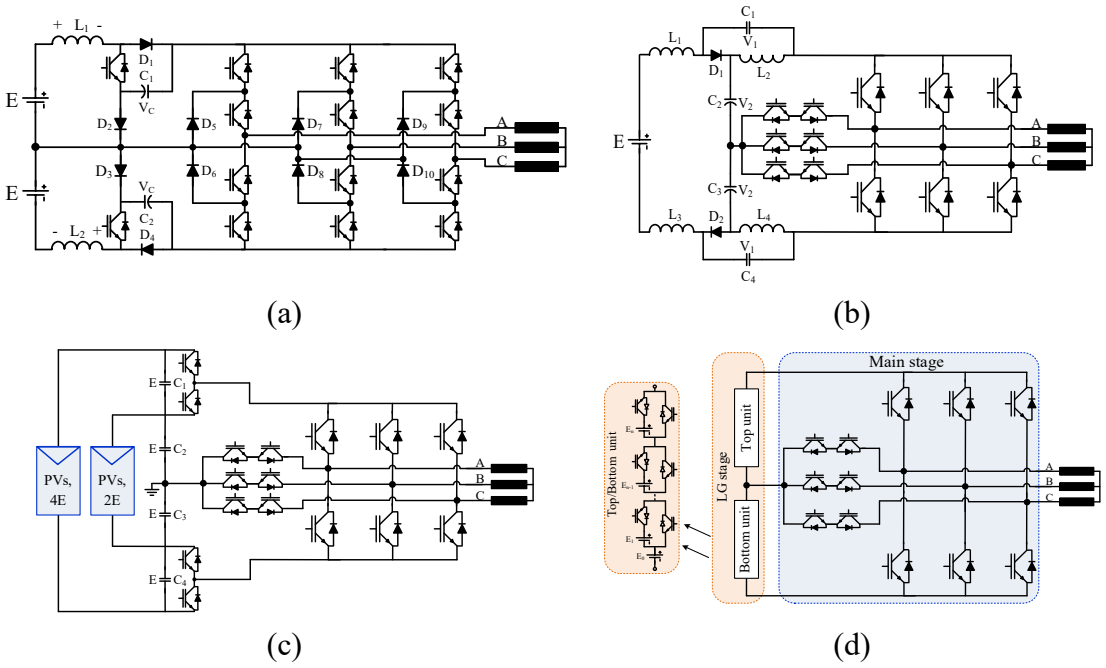


Figure 2.5: Three-phase MLIs based on either T-type or NPC-MLI. (a) Three-level LC-switching-based voltage boost NPC-MLI [56]. (b) Quasi-Z-source inverter with a T-type MLI [57]. (c) Modified T-type three-level inverter [58]. (d) Hybrid MLI with separate level and phase-sequence parts [59].

The performance and power quality of the MLIs are enhanced by increasing the output voltage level number [60]. Therefore, many topologies are developed to enlarge the level count above three levels. Figures 2.6 and 2.7 show a group of four-level topologies for low- and medium-voltage applications [61-69]. Figure 2.6 (a) shows the eighteen-step inverter (EI) topology in [61], which generates four voltage levels by using twelve switches, twenty-four diodes, three DC-link capacitors, and one DC source. As compared to many existing four-level topologies, the EI topology requires fewer active switches and does not need any flying capacitor. However, it suffers from using a high count of clamping diodes and high-voltage ratings of the semiconductor devices. For example, six switches block 3*E*, six switches block 2*E*, twelve diodes withstand for 2*E* and twelve diodes subject to *E* when applying a DC-link voltage of 3*E*. To mitigate the drawbacks of

EI topology, a four-level NNPC (4L-NNPC) was presented in [62], combining the FC-MLI and NPC-MLI. It consists of eighteen switches, six clamping diodes, six flying capacitors, two DC-link capacitors and one DC source, as depicted in Figure 2.6 (b). It reduces the clamping diode count to only six instead of twenty-four diodes in the EI, but the numbers of the flying capacitors and switches are increased to six capacitors and eighteen switches, respectively. Although the 4L-NNPC has a lower count of diodes and DC-link capacitors than the EI circuit, it must use higher flying capacitor and switch counts, increasing the size, cost, and control requirements. Its salient features include low total standing voltage of the switches and using switches of equal rating, attracting more investigations to mitigate its shortcomings [70, 71].

Figure 2.6 (c) shows the hybrid π-type topology reported in [63]. It eliminates the clamping diodes in both EI and 4L-NNPC, but it requires an addition of twelve switches and three flying capacitors as compared to the EI circuit or needs six additional switches while saving three flying capacitors as compared to the 4L-NNPC. Despite removing clamping diodes, the hybrid π-type topology still has a high count of switches besides using three flying capacitors, increasing its cost and size. Alternatively, a four-level active neutral point clamped (4L-ANPC) topology was reported in [64] to eliminate flying capacitors in the hybrid π-type inverter while using the same switch count. As shown in Figure 2.6 (d), the 4L-ANPC consists of twenty-four switches, three DC-link capacitors, and a single DC source. It is worth mentioning that the switch count can be reduced to eighteen instead of twenty-four by replacing twelve switches with only six switches at the double voltage rating.

The authors in [65-67] presented a nested T-type (NT-type) MLI, consisting of six switches and two flying capacitors per inverter leg, as shown in Figure 2.7 (a). The three inverter legs share the same DC-link, which is formed by a single DC source without using DC-link capacitors. The NT-type MLI can be used to deal with the high switch count of the hybrid π-type topology in [63] while keeping the diode-free feature of the hybrid π-type against EI and 4L-NNPC circuits. The switch count is reduced to eighteen instead of twenty-four while the DC-link capacitors are eliminated. These benefits came with the cost of using six flying capacitors instead of three in the hybrid π-type circuit, increasing the control complexity and decreasing the lifetime.

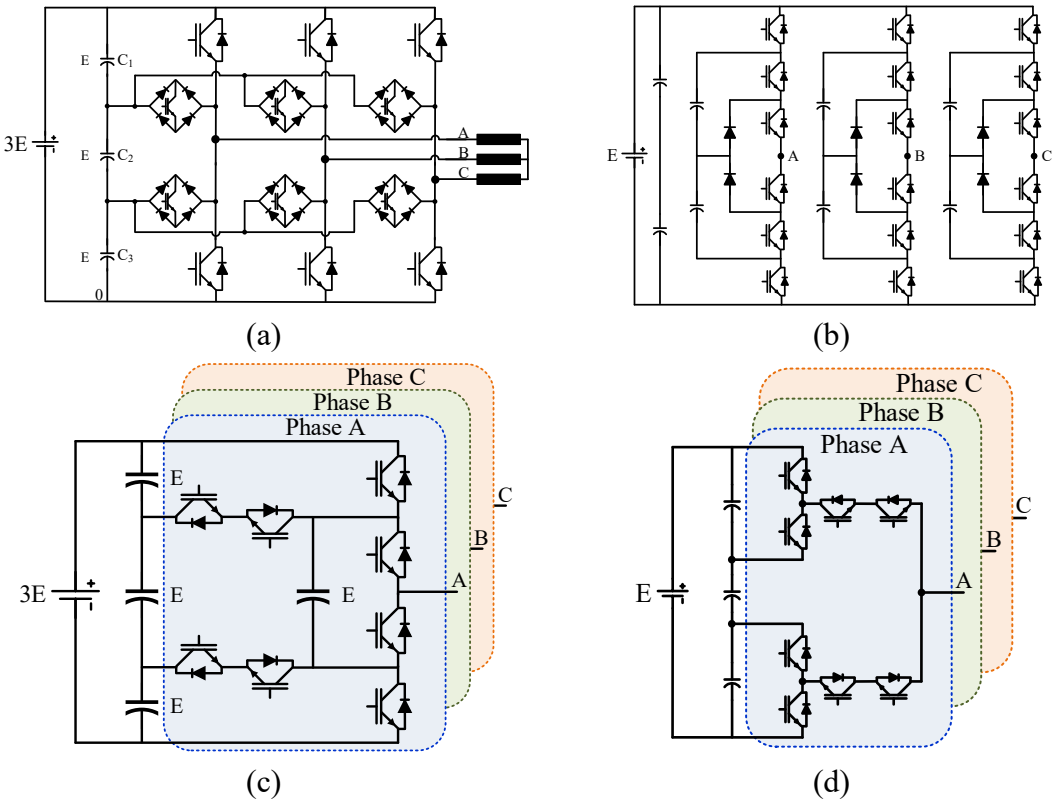


Figure 2.6: Three-phase four-level topologies in [61-64]. (a) Eighteen-step inverter [61]. (b) Four-level nested neutral point-clamped [62]. (c) Hybrid π-type topology [63]. (d) Active neutral-point clamped [64].

To solve the drawbacks of using flying capacitors in the NT-type inverter while preserving the reduced switch count and removing clamping diodes, the authors in [68, 69] presented the dual T-type (DT-type) and π-type MLIs. Figures 2.7 (b) and (c) show the circuits of DT-type and π-type inverters, respectively. The DT-type topology in [68] uses eighteen switches, three DC-link capacitors and one DC source. The eighteen switches are configured in a way to build six T-type legs, being connected back-to-back through three bidirectional switches. Similarly, the π-type inverter in [69] uses the same counts of switches, DC sources, and DC-link capacitors. Both two circuits can eliminate flying capacitors and clamping diodes, being considered as their main merits. However, they still suffer from a high-voltage stress of the full DC-link voltage applied on six switches out of eighteen switches.

The drawbacks of the above topologies include high counts of DC sources in [56, 58, 59], power diodes in [55, 56, 61, 62], flying capacitors in [62, 63, 65-67], and switches in [63, 64], increasing the inverter footprint, cost, failure rate, and control complexity. Further, a high percentage of the employed semiconductor

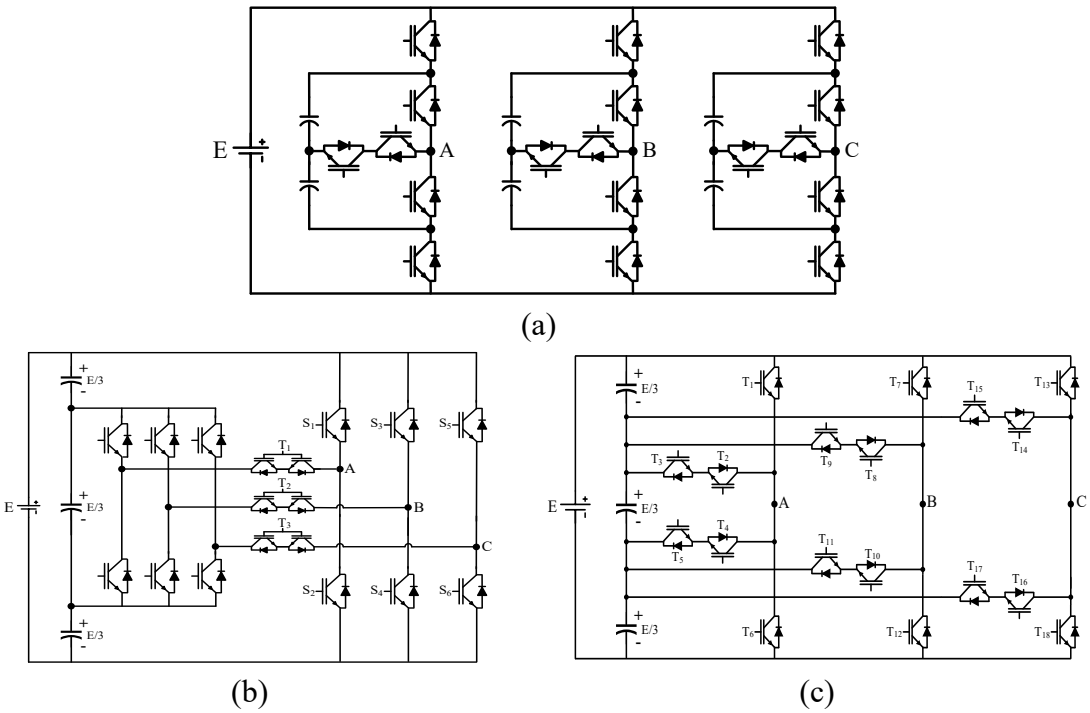


Figure 2.7: Three-phase four-level topologies in [65-69]. (a) Nested T-type [65-67]. (b) Dual T-type [68]. (c) π-type [69].

switches in those topologies must withstand the full input voltage, for example, 50% in [52, 57, 61] and 33% in [68, 69], restricting the reachable output voltage and increasing the switching losses. As mentioned above, the T-type MLI is considered as an attractive three-level solution in many advanced topologies [57-59]. However, its six switches of twelve must withstand the full voltage of the DC-link, having negative implications on cost, loss, and reachable voltage. Therefore, proposing novel three-level circuits, with reduced voltage stresses to compete with T-type is an important topic in developing MLIs. Further, the features of MLIs are improved by increasing the number of levels as discussed before. One recently developed four-level inverter is the π-type MLI [69]. Despite eliminating flying capacitors and clamping diodes, it needs one-third of its switches to be rated at the full DC-link voltage. To overcome this drawback, it is necessary to develop novel inverters, that can preserve the features of π-type and reduce high-voltage switches.

2.2.2 High-voltage MLIs

One unique merit of some MLIs is their ability to reach higher voltage values while utilizing low-voltage components, broadening MLI applications. Common approaches in developing high-voltage MLIs include: A) stacking low-voltage single-phase modules in cascade, namely as multicell or cascaded configuration,

B) hybridizing one three-phase low-voltage stage with several repeated cells in a granular configuration [72]. Some promising topologies are introduced in [73-76] and [72, 77] for the first and second approaches, respectively. Figure 2.8 (a) shows the asymmetrical inverter topology in [73], which is formed by connecting *m* main cells in cascade. Each cell generates fifteen voltage levels and requires twelve switches and three asymmetrical DC sources (E_1=*5E*, E_2= *2E*, and E_3=*E*). It can be extended to enlarge the output level count by either adding more sub-units to the main cell or/and cascading several main cells, as detailed in [73]. Its features include low component count along with eliminating both flying capacitors and clamping diodes. On the other hand, its major drawbacks are the high DC source count and high-voltage stresses of switches. For example, in each main cell, S_1 and S_2 must block *2E*, S_3-S_6 block *5E*, S_7 and S_8 subject to *7E*, and S_9 blocks *E*. The hybrid cascaded MLI (HC-MLI) in [74] can reduce the DC sources and almost double the voltage levels of the topology in [73], but must use a high flying capacitor count. The HC-MLI topology employs level doubling units (LDUs), in which each one is a half H-bridge fed by a capacitor. The LDU is connected to a three-level H-bridge (3L-HB) to form one primary module. Due to the asymmetrical binary ratio between the DC source in the H-bridge and the LDU capacitor, five voltage levels can be generated as detailed in [74]. Producing higher voltage levels requires cascading several modules with different asymmetrical

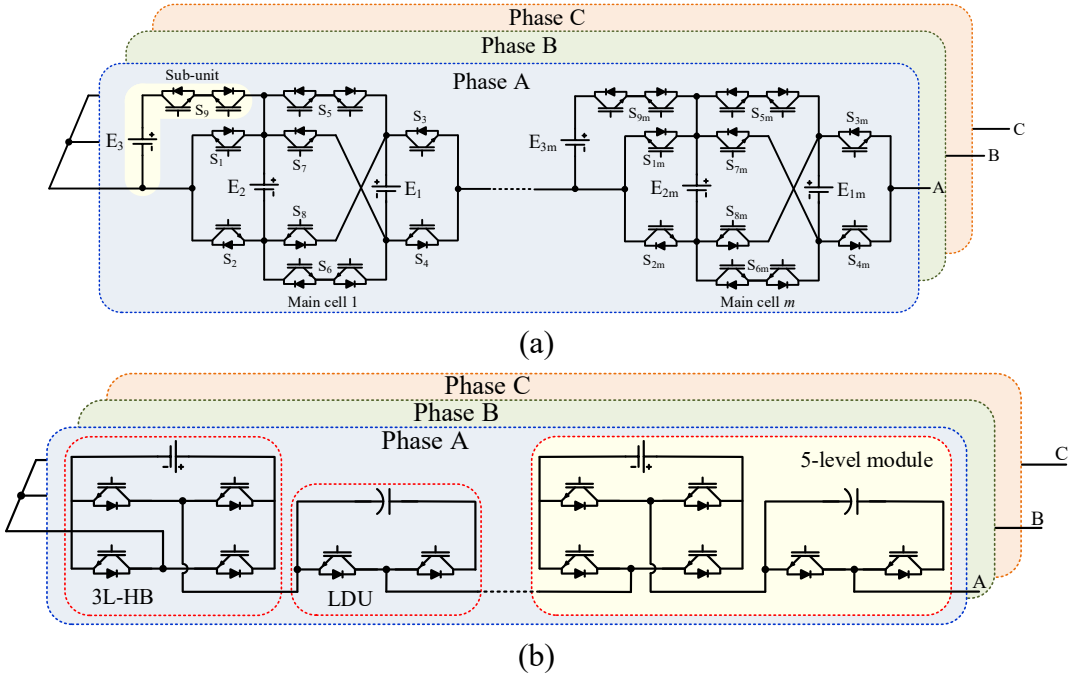


Figure 2.8: Three-phase configuration of multicell topologies in [73, 74]. (a) Asymmetrical MLI topology [73]. (b) Hybrid cascaded MLI [74].

ratios, as shown in Figure 2.8 (b). For example, two primary modules with 1:7 asymmetry can produce 33 voltage levels, requiring 36 switches, six flying capacitors, and six asymmetrical DC sources. Producing high-resolution waveforms with low component count is considered as the main feature of the HC-MLI. However, it suffers from using a high count of flying capacitors and high-voltage stress of switches due to the high asymmetry ratios.

Two new structures are introduced in [75, 76], acting as building blocks in multicell topologies for high-voltage applications. They can be configured with symmetric or asymmetric DC sources for producing a high-resolution output voltage. The structure unit in [75] consists of one bidirectional switch, six unidirectional switches and a voltage divider network formed by connecting two capacitors in series. It generates nine, seven, and eleven levels by using two DC voltage sources with ratios of 1:1, 2:1, and 2:3, respectively. Detailed extension options are provided in [75]. Figure 2.9 (a) shows the *N*-level configuration, which is formed by connecting several structure units in cascade. Using high counts of switches and capacitors is its main limitation. Alternatively, the cross-switched structure in [76] does not require any capacitors, and uses two switches lower than [75]. However, it produces lower voltage levels than the basic structure in [75]. For example, for symmetrical operations, the cross-switched structure in [76] generates five voltage levels instead of nine levels in [75]. The level number can be extended by using several configurations as detailed in [76]. Figure 2.9 (b) shows the recommended configuration by the authors in [76], being constructed by using two basic structures connected in cascade for constructing each phase leg. It requires twelve switches and four DC sources to produce 9 and 49 levels for symmetrical and asymmetrical operations, respectively. Features of being capacitor- and inductor-free are considered as its main merit, but it still suffers from using many isolated DC sources.

In addition to the aforementioned multicell topologies, a hybrid topology belonging to the granular configurations is presented in [77]. Figure 2.10 shows the schematic diagram of its three-phase arrangement, in which a three-level T-type inverter works as the main stage, and a new four-level cell is connected in cascade for producing more levels. The new four-level cell is a modified full H-bridge and constructed from two capacitors, four switches and two DC sources. The reduced switch count and operating in symmetrical or asymmetrical modes are the main features of this MLI. However, it uses many DC sources and capacitors, increasing the inverter size and complexity. By using only one cell per

phase in addition to the main stage, nine voltage levels can be achieved with twenty-four switches, eight capacitors, and seven symmetrical DC sources. By increasing the cell numbers, the output voltage and level count can be increased as well. Consequently, more capacitors and DC sources must be used.

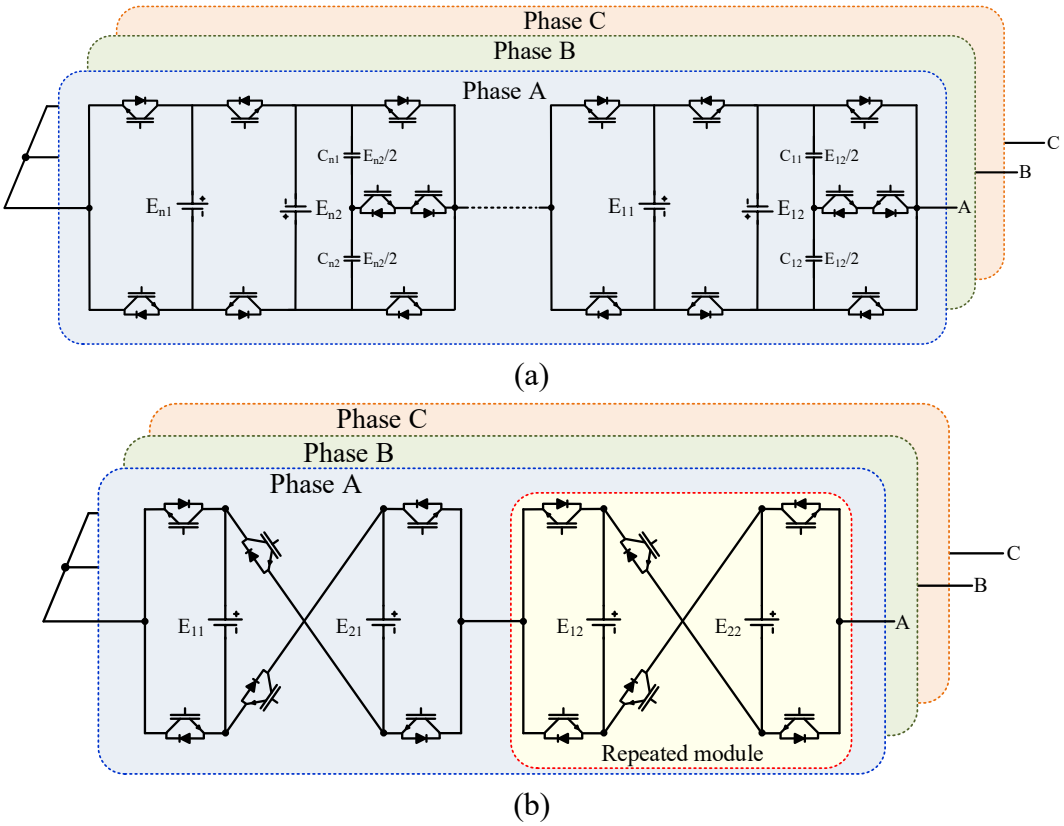


Figure 2.9: Three-phase configuration of multicell topologies in [75, 76]. (a) High-voltage configuration of the MLI in [75]. (b) Cascaded cross-switched topology [76].

It is worth mentioning that the extension technique in granular configurations in [72, 77] can be applied to all low- and medium-voltage MLIs, making them applicable to high-voltage applications. According to the above-discussed topologies, many primary cells should be cascaded to increase the output voltage values, requiring high counts of switches, capacitors, and isolated DC sources. All high-voltage topologies suffer from common drawbacks of huge DC source count, making them most applicable for PV farms where realising DC sources is easy. Further, by using high asymmetry ratios between the DC sources to increase the level count, the voltage ratings of switches and other components are increased dramatically. To tackle these drawbacks, the transformer-based MLIs can be used as alternatives.

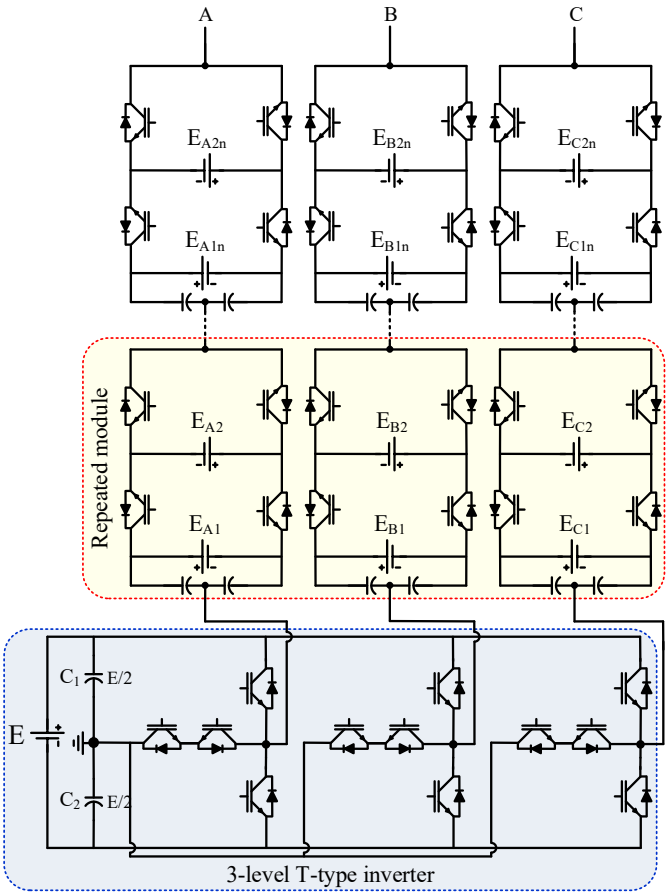


Figure 2.10: Three-phase hybrid MLI for renewable energy [77].

2.2.3 Transformer-based MLIs

Transformer-based MLIs have received a significant attention due to features of reducing DC source count, providing galvanic isolation, and maximizing the output voltage [78, 79]. In the transformer-based MLIs, the roles of the transformers are typically either synthesizing three-phase voltages with multiple DC sources [78, 80-83] or creating several isolated voltages with low DC source count [79, 84-86]. Selected topologies for each group are briefly discussed hereafter regarding their structure, merits, and demerits.

Figure 2.11 (a) shows the transformer-based cascaded MLI (CMLI) in [78]. It comprises two stages: voltage generator stage (VGS) and polarity changer stage (PCS). Half-bridge modules are the building block in the VGS, thus adding more half-bridge modules enlarges the voltage level count. The PCS employs full H-bridges to bipolarize the generated unipolar multilevel voltages from the VGS. Producing three-phase voltages requires three single-phase transformers to couple the PCS outputs with the load. This CMLI requires three power transformers, $3N$+9 switches, and 0.5(N-1) DC voltage sources for generating N voltage levels. It can eliminate flying capacitors, clamping diodes and reduce the DC source count as

compared to FC-MLI, NPC-MLI, and CHB-MLI, respectively. However, using three H-bridge cells to produce bipolar voltages is a conspicuous drawback because of linking the switch blocking voltage to the output voltage level count. For example, the total standing voltage of PCS switches is $6(N\text{-}1)V_{DC}$, where V_{DC} is the voltage rating of each DC source in the DC-link, limiting the modularity of this CMLI and other associated features such as THD and dv/dt.

To tackle the drawbacks of the CMLI in [78], a hybrid nine-level inverter (H9LI) is proposed in [80], which can produce bipolar voltages without a polarity changer. Figure 2.11 (b) illustrates its three-phase configuration. It employs twenty-four switches, nine capacitors, six power diodes, one DC source, and three single-phase transformers. It saves twelve switches and three DC sources as compared to the CMLI when producing nine-level voltages. However, reducing DC sources and switches requires higher numbers of power diodes and capacitors, decreasing the inverter efficiency, reliability, and life span. Further, during startup, the H9LI requires pre-charging circuits for three capacitors, as suggested by the authors in [80]. Figure 2.11 (c) shows the modified active-neutral point-clamped (MANPC) topology in [81], which reduces the capacitors and eliminates the clamping diodes in H9LI, decreasing the total component count as compared to H9LI in [80]. It requires thirty switches, five capacitors, three single-phase transformers, and one DC source to produce nine voltage levels. Both MANPC and H9LI use the same count of transformers and DC sources, but the MANPC topology eliminates the six power diodes in H9LI and uses only five capacitors instead of nine in H9LI, reducing component counts, simplifying control algorithms, and improving inverter reliability. However, using additional six switches is a disadvantage of the MANPC as compared to the H9LI.

A cascaded-transformer MLI (CT-MLI) based on three-level NPC (3L-NPC) legs is presented in [86]. It employs T single-phase transformers with asymmetrical turn ratios and T+1 legs for each phase. The transformer secondary windings are connected in series to synthesize output voltages with N levels. On the other hand, the positive terminals of primary windings are connected to the midpoints of the T inverter legs, while the midpoint of the shared leg T+1 is used as a connection point for all negative terminals, as shown in Figure 2.12 (a). The three phases of CT-MLI share a single DC-link formed by two capacitors and one DC source. Producing $(2\cdot3^{T}\text{-}1)$ levels needs $3T$ transformers, $12(T+1)$ switches, and $6(T+1)$ clamping diodes. For example, one DC source, two capacitors, six transformers, 36 switches, and eighteen diodes are required to generate seventeen voltage levels.

The other two configurations of the CT-MLI and turn ratios selection are detailed in [86]. Using a single DC source, low voltage rating of switches, and modularity are considered as its main features. However, requiring many switches, transformers, and power diodes is its limitation, along with voltage stresses across the diodes equal to 50% of the full DC-link voltage.

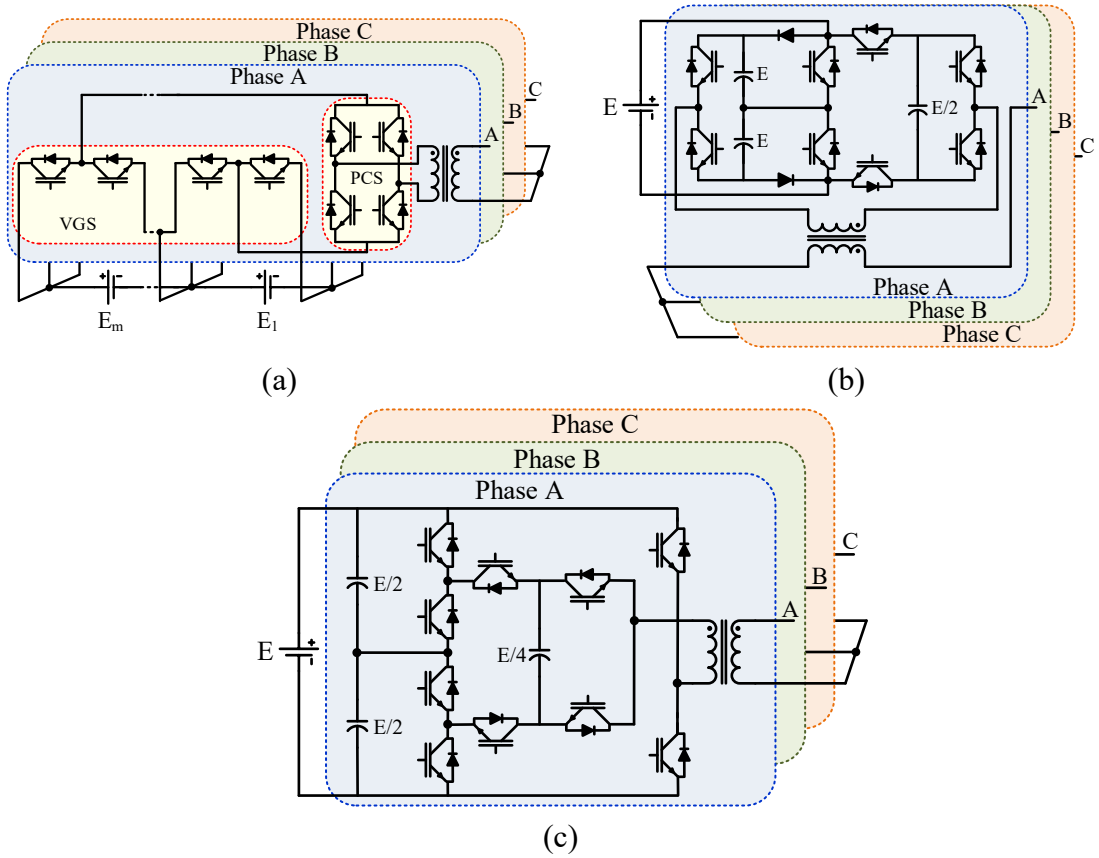
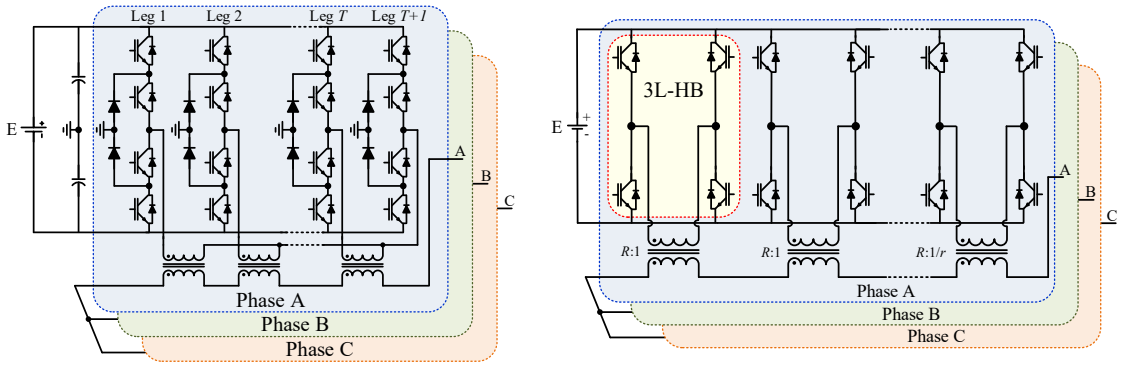


Figure 2.11: Transformer-based MLIs in [78, 80, 81]. (a) Transformer-based cascaded MLI [78]. (b) Hybrid nine-level inverter [80]. (c) Modified active-neutral point-clamped [81].

The transformer-based topology in [79] is based on the 3L-HB inverter, so it can eliminate both clamping diodes and capacitors of the CT-MLI in [86]. Figure 2.12 (b) shows its three-phase arrangement, consisting of 3(K-1) transformers with turn ratios of R:1 and three transformers with R:1/r, where K is the H-bridge cell count. Using K cells produces (2r(K-1) +3) voltage levels, and it requires 12K switches. The value of r should be either 2 or 3 for producing multilevel voltages with equal steps as recommended in [79]. One DC source, 48 switches, and twelve transformers are needed when using four cells per phase, producing fifteen and twenty-one voltage levels at r of 2 and 3, respectively. Modularity, being capacitor-, diode-free, and reduced switch count are its key merits. However, demanding many transformers increases the size and cost of the inverter.



(a) (b)

Figure 2.12: Cascaded-transformer MLIs in [79, 86]. (a) CT-MLI based on 3-L NPC [86]. (b) CT-MLI based on 3L-HB [79].

The transformer-based MLIs have several beneficial features as mentioned before, but they suffer from requiring high counts of DC sources in CMLI [78], power diodes and capacitors in H9LI and CT-MLI [80, 86], switches in MANPC [81], or transformers in CT-MLI and TB-CHB [79, 86]. The common disadvantage in the transformer-based MLIs is their big size because of employing low-frequency transformers. It can be noted that the transformer sizes in the first group in Figure 2.11 are larger than the second group in Figure 2.12 due to contributing to the transferred power with higher portions. In some topologies, the transformer size can be reduced by increasing the switching frequency and using high-frequency transformers, but this results in increasing the power losses and switch control requirements. Therefore, proposing novel topologies with reduced DC sources, transformers, and component count is important to advance the transformer-based MLIs.

Chapter 3

Novel multilevel inverter topologies

This chapter presents the proposed MLI topologies in this dissertation, detailing the circuit configuration, operating concept, and switching strategy for each topology. The proposed topologies are labelled by Topology A (T_A) to Topology D (T_D) and discussed in Sections 3.1 to 3.4, respectively. This chapter is based on papers II to VI.

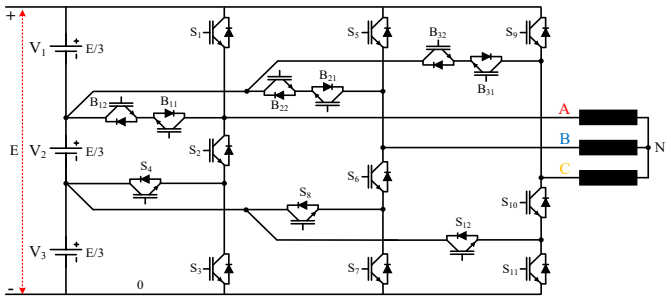
3.1 Proposed topology T_A

3.1.1 Circuit configuration

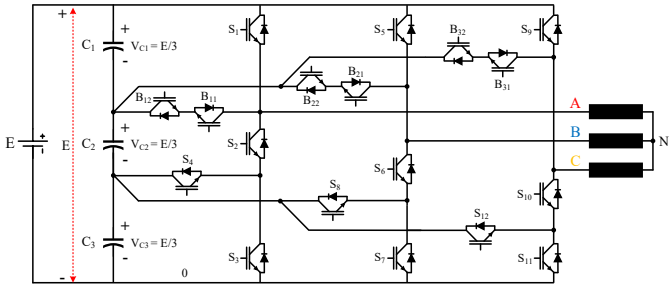
Figure 3.1 shows the circuit configuration of the proposed topology T_A, consisting of twelve unidirectional switches (S_1-S_{12}) and three bidirectional switches (B_1-B_3). It does not use any power diode or flying capacitor, reducing control algorithms complexity, power loss, and increasing the inverter lifetime. To simplify the gate-drive circuits, the common-emitter structure is adopted to configure the bidirectional switches. Further, the three-phase legs share the same DC-link, reducing the counts of DC sources and DC-link capacitors.

Depending on the availability of the DC sources or applications, the DC-link of the proposed topology can be configured in two ways: either using three low-voltage DC sources or single medium-voltage DC source linked to three DC-link capacitors as shown in Figures 3.1 (a) and (b), respectively. Renewable energy systems based on PVs and fuel cells have multiple DC sources, thus the first configuration is recommended to be used in those energy systems. Accordingly, DC-link capacitors and their associated control algorithms can be eliminated. However, power electronic conditioner circuits are needed to control/maximize the raw generated power from those renewable energy sources. On the other hand, the second configuration or single source configuration (SSC) in Figure 3.1 (b) is

recommended for industrial applications, where a single medium-voltage bus is available.



(a)



(b)

Figure 3.1: The proposed topology T_A. (a) Multiple sources configuration (MSC), recommended for energy systems. (b) Single source configuration (SSC), recommended for industrial applications.

3.1.2 Operating concept

The inverter switches are controlled to produce four unipolar voltage levels of 0, $E/3$, $2E/3$, and E in the pole voltages V_{A0}, V_{B0}, and V_{C0}. The three waveforms of the pole voltages are shifted in phase by 120°, so subtracting any two of them produces seven-level bipolar voltages. For example, V_{AB} is synthesized by subtracting V_{B0} from V_{A0}, producing a seven-level voltage of 0, $\pm E/3$, $\pm 2E/3$, and $\pm E$.

The operating modes of the proposed topology are illustrated in Figure 3.2, showing the switching states for producing seven voltage levels in V_{AB}. Each state is accompanied by its corresponding paths for the positive and negative currents. For example, in Figure 3.2 (a), the state I shows that the switches S_1, S_6, and S_7 must be in ON-states to obtain the maximum positive voltage of E in the line voltage V_{AB} while switches (S_2-S_4), (S_5, S_8) and (B_1, B_2) are in OFF-states. The positive and negative currents are highlighted in blue and red dash lines, respectively. Similarly, switching states from II to VIII in Figures 3.2 (b) to (h) explain the different switching modes of the proposed topology for producing the remaining voltage levels. It should be noted that some switching states are

removed when forming these switching paths, preventing the short-circuit faults in the inverter. For example, in leg A, the switching combinations of (S_1, S_2, S_3), (S_1, S_2, S_4), (S_3, S_4), (S_1, B_1), and (B_1, S_2, S_4) are marked as unused states in both switching algorithms.

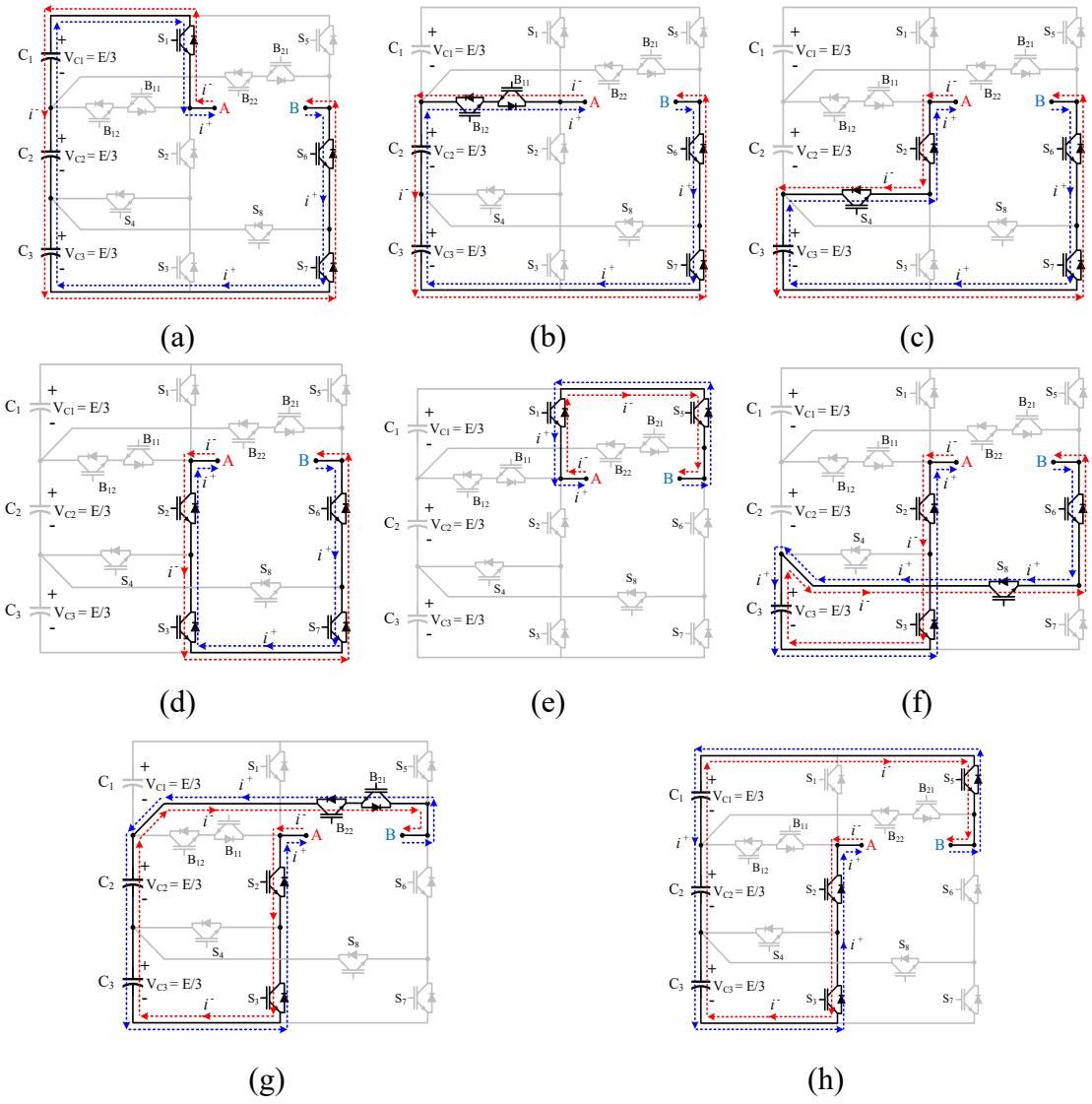


Figure 3.2: Switching states of T_A. (a) State I: V_{AB}= E. (b) State II: V_{AB}= 2E/3. (c) State III: V_{AB}= E/3. (d) State IV: V_{AB}= 0. (e) State V: V_{AB}= 0. (f) State VI: V_{AB}= -E/3. (g) State VII: V_{AB}= -2E/3. (h) State VIII: V_{AB}= -E.

3.1.3 Modulation strategies

Two modulation strategies are utilized in this section to control the output voltage of T_A. The low-frequency modulation (LFM) is adopted to reduce the switching loss, while the level-shifted pulse width modulation (LSPWM) is implemented to increase the controllability of the output voltage. Both switching strategies follow the provided switching states in Table 3.1 to create the switching pulses for the

proposed inverter. Table 3.1 shows the switching pattern of switches (S_1-S_4) and B_1 for producing four levels in the pole voltage V_{A0}.

Table 3.1: Switching states for producing four levels in the pole voltage V_{A0}.

State	V_{A0}	S_1	S_2	S_3	S_4	B_1
A	**E**	ON	OFF	OFF	OFF	OFF
B	**2E/3**	OFF	OFF	OFF	OFF	ON
C	**E/3**	OFF	ON	OFF	ON	OFF
D	**0**	OFF	ON	ON	OFF	OFF

Figure 3.3 (a) shows the LFM switching pattern accompanied by the pole voltage V_{A0}. In the LFM scheme, three sinusoidal reference signals (only SR_A is shown) and two modulator signals H^+ and H^- are used for generating three controlling signals, M_1-M_3. For instance, M_1 and M_2 are produced by comparing the SR_A signal with H^+ and H^-, respectively, while comparing the SR_A signal with zero produces the M_3 controlling signal. Simple logical operators summarized in (3.1)-(3.5) are applied on M_1-M_3 for producing five switching signals of switches S_1-S_4 and B_1 in leg A. Similarly, switching signals for the switches in legs B and C can be generated. Both sinusoidal and modulator signals can be varied in their magnitude from 0 to 1, providing extra flexibility for producing voltages at different RMS, level counts, and THDs. For example, selecting a magnitude value of 1 for the three sinusoidal signals and ±0.35 for H modulators can produce seven-level line voltages with THD of 11.81%. Nevertheless, five-level line voltages with the THD of 34.88% are produced when H modulators are equal to ±0.9.

$$S_1 = M_1 \tag{3.1}$$

$$S_2 = \overline{M_3} \tag{3.2}$$

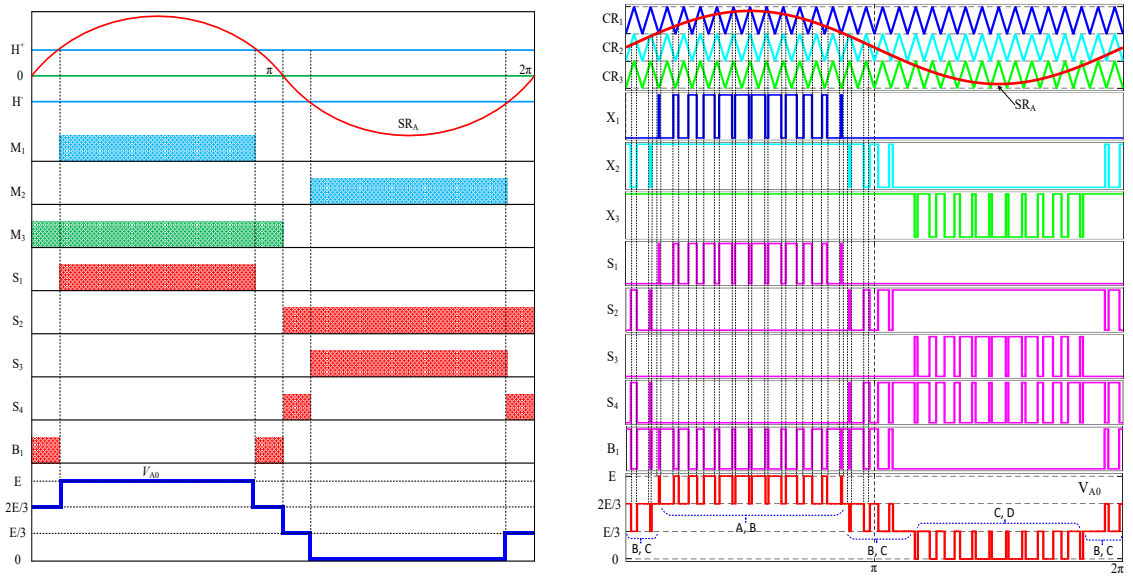
$$S_3 = M_2 \tag{3.3}$$

$$S_4 = \overline{M_2} \times \overline{M_3} \tag{3.4}$$

$$B_1 = \overline{M_1} \times M_3 \tag{3.5}$$

Although the controllability of the applied LFM is better than the conventional LFM, it is still not as smooth as the other switching schemes based on sinusoidal pulse width modulation. Therefore, the LSPWM scheme is also utilized for producing the switching signals of the proposed topology. The LSPWM requires three carrier signals and three sinusoidal modulation signals to produce the

required switching pulses. The carrier signals have a fixed amplitude of V_{cr} and are shifted in level by $V_{cr,}$ while the three sinusoidal signals are shifted in phase by 120°, and their magnitude can be varied from 0 to $1.5V_{cr}$. Figure 3.3 (b) shows the generation process of switching pulses for leg A switches, S_1-S_4 and B_1, in which three carrier signals CR_1, CR_2 and CR_3 are compared with one sinusoidal reference signal SR_A, producing three controlling signals X_1, X_2 and X_3. Equations (3.6)-(3.10) describe the logical operation applied on X_1-X_3 signals to generate the switching pulses. The last trace in Figure 3.3 (b) shows the pole voltage V_{A0} with four voltage levels of 0, E/3, 2E/3, and E, being marked by the switching states in Table 3.1.



(a) (b)

Figure 3.3: Switching pattern and the pole voltage V_{A0}. (a) LFM. (b) LSPWM.

$$S_1 = X_1 \tag{3.6}$$

$$S_2 = \overline{X_2} \tag{3.7}$$

$$S_3 = \overline{X_3} \tag{3.8}$$

$$S_4 = \overline{X_2} \times X_3 \tag{3.9}$$

$$B_1 = \overline{X_1} \times X_2 \tag{3.10}$$

The pre-described operators in (6)-(10) can be applied on X_4-X_9 signals to generate the switching pulses for switches in legs B and C. The X_4-X_9 are the controlling signals, resulting from the comparison process between three carrier

signals and the other two phase-shifted sinusoidal signals SR_B and SR_C. It is worth mentioning that the above-explained LSPWM scheme should be modified to balance the three capacitor voltages in SSC of the proposed topology as detailed in paper II.

3.2 Proposed topology T_B

3.2.1 Circuit configuration

The low-voltage configuration of the proposed topology B (T_B) is shown in Figure 3.4 (a), which is a transformerless MLI and does not require any flying capacitor, power diode or coupled inductor in its operation, allowing for a high-efficiency and compact design. Each phase consists of only four switches, being distinctively connected for constructing a three-level unit. Further, to reduce the DC source count, the three-phase legs share the same DC-link. The DC-link is formed by connecting two symmetrical DC sources of E in series. However, these DC sources can be replaced by batteries or AC voltage sources followed by rectifiers or different RESs, e.g., PV strings and fuel cells.

In addition to the low-voltage configuration of the proposed inverter, the N-level hybrid configuration for high-voltage applications is proposed as shown in Figure 3.4 (b), using the three-level configuration as a fixed stage and a new three-phase module as a repeated stage. Each module has three basic cells or one cell for each phase. Each basic cell requires eight switches and two DC sources. It can produce five voltage and seven voltage levels for symmetrical and asymmetrical DC sources, respectively. As shown in Figure 3.4 (b), the basic cell is formed by using the DC-link and either (leg A + leg B) or (leg B + leg C) or (leg C + leg A), which is the two-phase version of the fixed stage in Figure 3.4 (a). The basic cell is formed in a way to allow it to be used in the two proposed configurations, reducing complexity, maintenance and voltage upgrading costs.

In the hybrid configuration of the proposed topology, the voltage levels can be enlarged to N levels without increasing the voltage stress across the switches due to its modularity feature. The counts of the three-phase modules M, switches N_{SW}, and DC sources N_{DC} in terms of voltage levels N, are presented in (3.11)-(3.13). Only one module is needed to produce seven levels in the pole voltage as calculated in (3.11). Consequently, eight symmetrical DC sources and thirty-six switches are required according to (3.12) and (3.13), respectively.

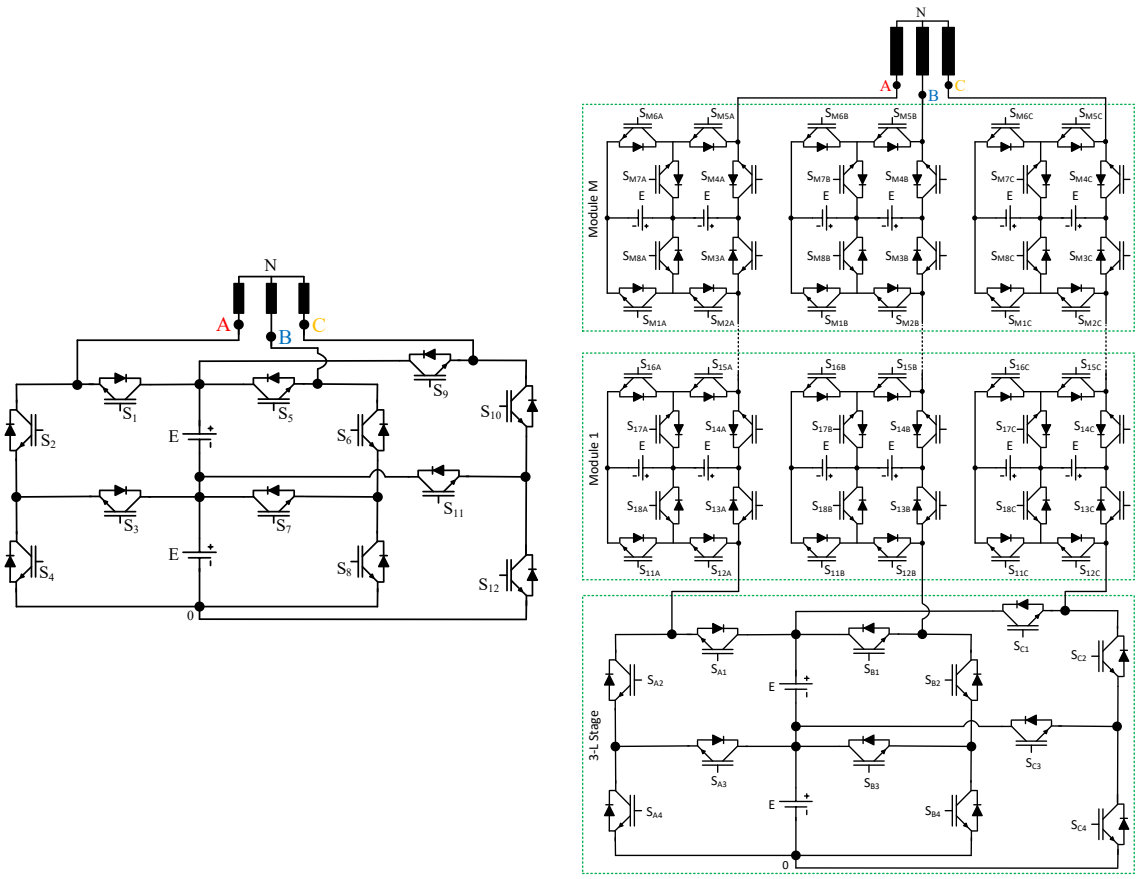


Figure 3.4: Circuit configuration of T_B. (a) 3-level low-voltage configuration. (b) N-level high-voltage hybrid configuration.

$$M = 0.25N - 0.75 \tag{3.11}$$

$$N_{DC} = 1.5N - 2.5 \tag{3.12}$$

$$N_{SW} = 6N - 6 \tag{3.13}$$

It is worth mentioning that the switch count for each module can be reduced to eighteen instead of twenty-four switches. This can be obtained by merging the three switches S_{M5A}, S_{M6A}, and S_{M7A} in each basic cell to be one switch and changing the switching algorithm a little bit. For example, in the first module (i.e., $M = 1$), S_{15A}, S_{16A}, and S_{17A} can be merged to be one switching device with a higher blocking voltage ($2E$ instead of E). Accordingly, the total number of required switches could be reduced, as calculated in (3.14) for the symmetrical operation.

$$N_{SW} = 4.5N - 1.5 \tag{3.14}$$

3.2.2 Operating concept

Twelve power switches S_1 to S_{12} are used to create different paths from the two DC sources to the load. Therefore, the DC sources can be arranged in different ways for producing five levels 0, $\pm E$, and $\pm 2E$ in the line voltage. For example, when S_1, S_6, S_8, and S_9 are in ON-states, and the remaining switches are in OFF-states, the line voltages V_{AB}, V_{BC}, and V_{CA} are equal to $2E$, $-2E$ and 0, respectively.

Figure 3.5 shows the switching modes for the proposed circuit when producing five voltage levels in the line voltage V_{AB}, along with the conduction paths for the forward and reverse currents in red and blue lines, respectively. These switching modes have been selected to prevent any appearance of a positive voltage across built-in diodes of the switches. As a result, the DC sources are protected from short-circuit faults. Further, for the same reason, some selected switching states are removed from the control algorithms of the inverter. For example, in phase A, (S_1-S_3), (S_1, S_2, S_4) and (S_3, S_4) cannot be in ON-states at the same instance.

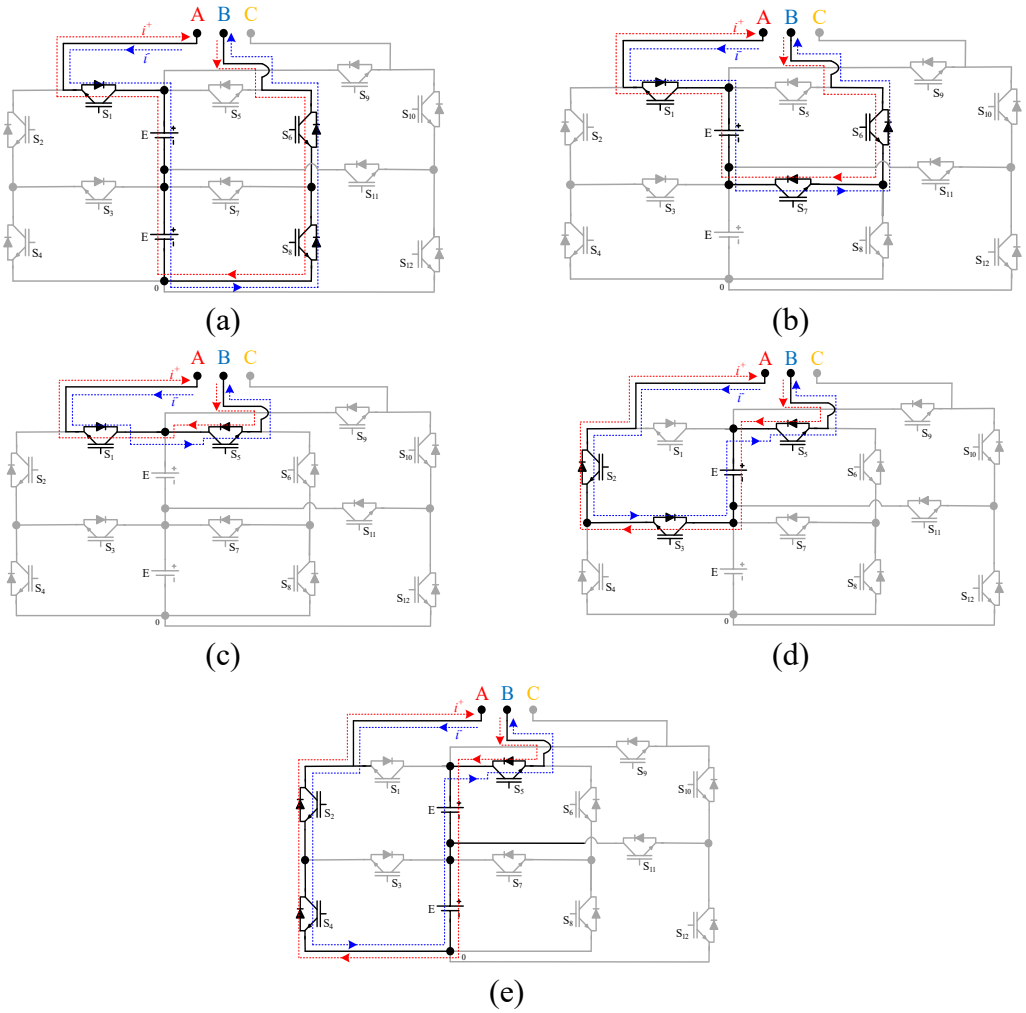


Figure 3.5: The switching modes for the low-voltage configuration. (a) $V_{AB} = 2E$. (b) $V_{AB} = E$. (c) $V_{AB} = 0$. (d) $V_{AB} = -E$. (e) $V_{AB} = -2E$.

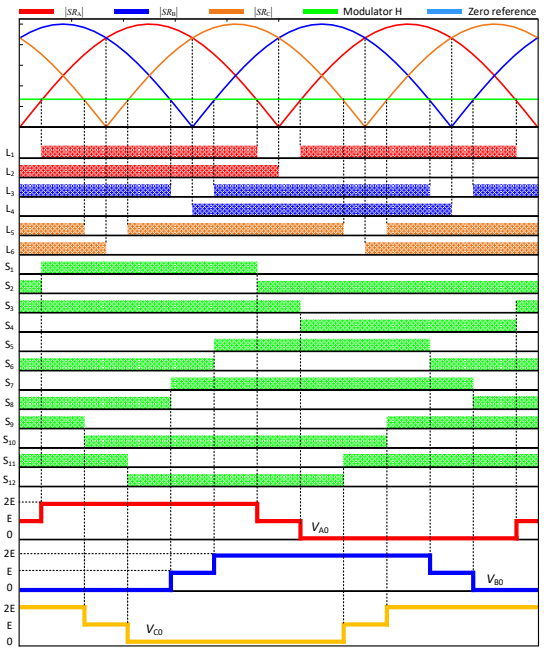
3.2.3 Modulation strategies

The low-voltage configuration in Figure 3.4 (a) has twenty-seven switching states, but only twelve states are required and summarized in Table 3.2, being used in the switching algorithms for the two modulation techniques. To reduce the power losses, reducing the count of ON-switches in the conducting path and switching cycles were taken into consideration when selecting these switching states. Table 3.2 shows that the switching states of S_3 and S_4 are labelled with 'X' letter for producing $2E$ in pole A. The 'X' state can be either in ON or OFF. However, to minimise switching cycles, the switching algorithms were designed to keep the same previous states of S_3 and S_4 to be their new switching states, i.e., X-state is ON if the previous state was ON, and vice versa. For example, in S_4, the previous switching state was OFF, so the new state is selected to be OFF.

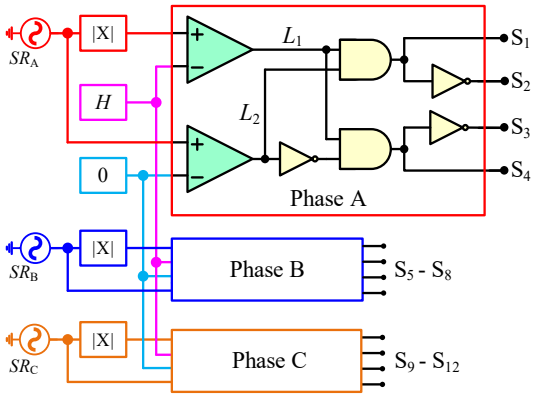
Figure 3.6 shows the switching patterns for the LFM and highlights the three-pole voltage waveforms V_{A0}, V_{B0}, and V_{C0}. The LFM uses three rectified sinusoidal waveforms with amplitudes of 1. These waveforms are compared to two signals, 'zero-reference' and a proposed modulator signal H, to generate L_1-L_6. The value of the modulator signal H can be varied from 0 to 1 for obtaining different numbers of voltage levels. Therefore, the proposed modulator H adds more flexibility for the online control of both level number and RMS value of the output voltages. Implementing Boolean operations on L_1 and L_2, as described in (3.15) and (3.16), results in the switching signals for phase A. For phases B and C, the procedures are similar except a phase-shift of 120°.

Table 3.2: Switching states and the corresponding pole voltages (X: ON or OFF).

V_{A0}	V_{B0}	V_{C0}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
			Pole A				**Pole B**				**Pole C**			
E	**0**	**2E**	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	OFF	X	X
2E	**0**	**2E**	ON	OFF	X	X	OFF	ON	OFF	ON	ON	OFF	X	X
2E	**0**	**E**	ON	OFF	X	X	OFF	ON	OFF	ON	OFF	ON	ON	OFF
2E	**0**	**0**	ON	OFF	X	X	OFF	ON	OFF	ON	OFF	ON	OFF	ON
2E	**E**	**0**	ON	OFF	X	X	OFF	ON	ON	OFF	OFF	ON	OFF	ON
2E	**2E**	**0**	ON	OFF	X	X	ON	OFF	X	X	OFF	ON	OFF	ON
E	**2E**	**0**	OFF	ON	ON	OFF	ON	OFF	X	X	OFF	ON	OFF	ON
0	**2E**	**0**	OFF	ON	OFF	ON	ON	OFF	X	X	OFF	ON	OFF	ON
0	**2E**	**E**	OFF	ON	OFF	ON	ON	OFF	X	X	OFF	ON	ON	OFF
0	**2E**	**2E**	OFF	ON	OFF	ON	ON	OFF	X	X	ON	OFF	X	X
0	**E**	**2E**	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	X	X
0	**0**	**2E**	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	X	X



(a)



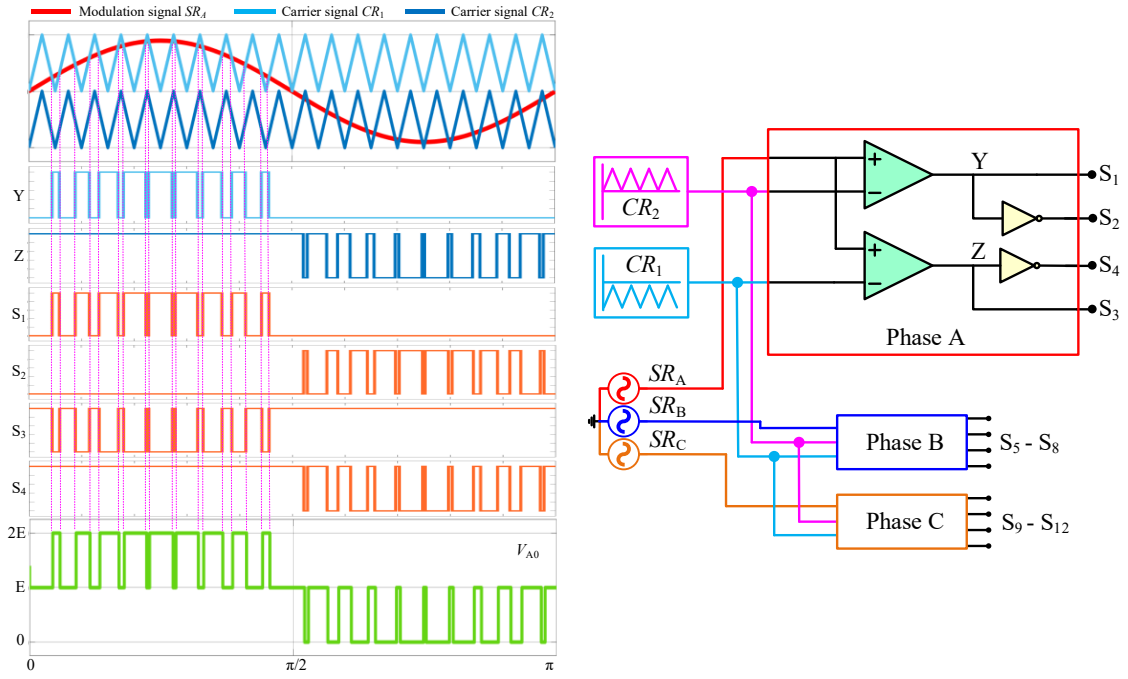
(b)

Figure 3.6: LFM switching scheme. (a) Key waveforms. (b) Switching logic.

$$\overline{S_1},\ S_2=\overline{L_1\times L_2} \tag{3.15}$$

$$\overline{S_3},\ S_4=L_1\times\overline{L_2} \tag{3.16}$$

For the LSPWM scheme, two carrier signals CR_1 and CR_2 and three sinusoidal waveforms SR_A, SR_B, and SR_C are required to generate the switching pulses. Figure 3.7 (a) shows the generation process of switching pulses for the four switches in phase A. The Y and Z signals are generated by comparing SR_A with the two carrier signals. Afterwards, different Boolean operators are used for extracting the correct switching signals from Y and Z, as seen in Figure 3.7 (b). Similarly, the switching pulses of the high-voltage configuration can be generated for LFM and LSPWM schemes, as detailed in paper IV.



(a) (b)

Figure 3.7: LSPWM switching scheme. (a) Key waveforms. (b) Switching logic.

3.3 Proposed topology T_C

3.3.1 Circuit configuration

Figure 3.8 shows the circuit configuration of the proposed topology C (T_C), consisting of three stages, a five-level stage (5-LS), a level generator stage (LGS), and a three-phase synthesizer stage (3-PS). The 5-LS and 3-PS are fixed regardless of the output voltage levels, while the LGS has repeated basic cells for enlarging the level count. Three T-type legs, three two-level legs, and two DC sources are used to construct the 5-LS, which acts as a base for the proposed topology. It has six output terminals, three of them (A, B, and C) are connected to the basic-cell strings in the LGS, while the other three terminals (i.e., A`, B`, and C`) are directly connected to the 3-PS. Although the basic cell can be any lower multilevel structures such as 3-L H-bridge, 3-L T-type leg, or other newer structures, the proposed configuration employs the same five-level cell in the 5-LS stage to reduce the demands of manufacturing, maintenance, and voltage upgrading. The last stage in topology T_C is the 3-PS, which couples the six output terminals of the proposed topology to a three-phase load. It consists of three single-phase transformers (T_{FA}, T_{FB}, and T_{FC}) that provide galvanic isolation and stepping-up features, being attractive in PV-based energy systems. It is worth mentioning that

the 3-PS can be eliminated in some applications like open-end winding motor drives.

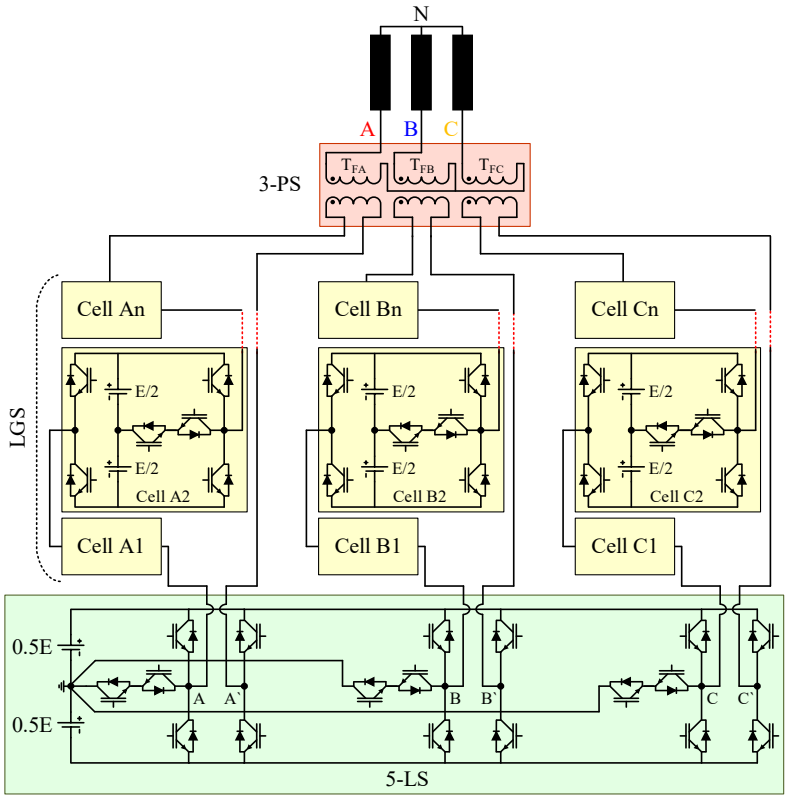


Figure 3.8: The circuit configuration of the proposed topology T_C.

The relationship between the output voltage level number N and the utilized components can be defined using (3.17)-(3.19).

$$N_{\text{Total}} = 6N - 7 \tag{3.17}$$

$$N_{\text{DC}} = 1.5N - 5.5 \tag{3.18}$$

$$N_{\text{SW}} = 4.5N - 4.5 \tag{3.19}$$

where N_{Total}, N_{DC}, and N_{SW} are the total component count, DC source count and switch count, respectively. For example, if three-phase voltages with five levels are required, the total number of the components will be twenty-three: two DC sources, eighteen switches, and three single-phase transformers.

3.3.2 Operating concept

The working principle of the topology T_C can be illustrated by considering it as three single-phase inverters connected in parallel to a single DC-link. Each one has six switches and produces five voltage levels across its output terminals. For example, phase A comprises two legs, I and II, as shown in Figure 3.9 (a). The

voltage difference between the midpoints of the two legs and the reference point R are labelled as V_{AR} and $V_{A`R}$. The $V_{AR}$ has three levels of -0.5$E$, 0, and 0.5$E$, while $V_{A`R}$ has two levels of -0.5E and 0.5E. By subtracting $V_{A`R}$ from $V_{AR}$, five voltage levels of 0, ± 0.5$E$, and ± E are generated. The two voltages are subtracted by using the transformer $T_{FA}$. Figures 3.9 (b)-(f) show the different operating modes of phase A to produce five levels in $V_{AA`}$. For example, Mode I in Figure 3.9 (b) shows that producing -E voltage requires switches S_2 and S_3 to be ON and S_1, S_4, and T_1 to be OFF. Figures 3.9 (c) to (f) highlight the generation of the remaining four levels.

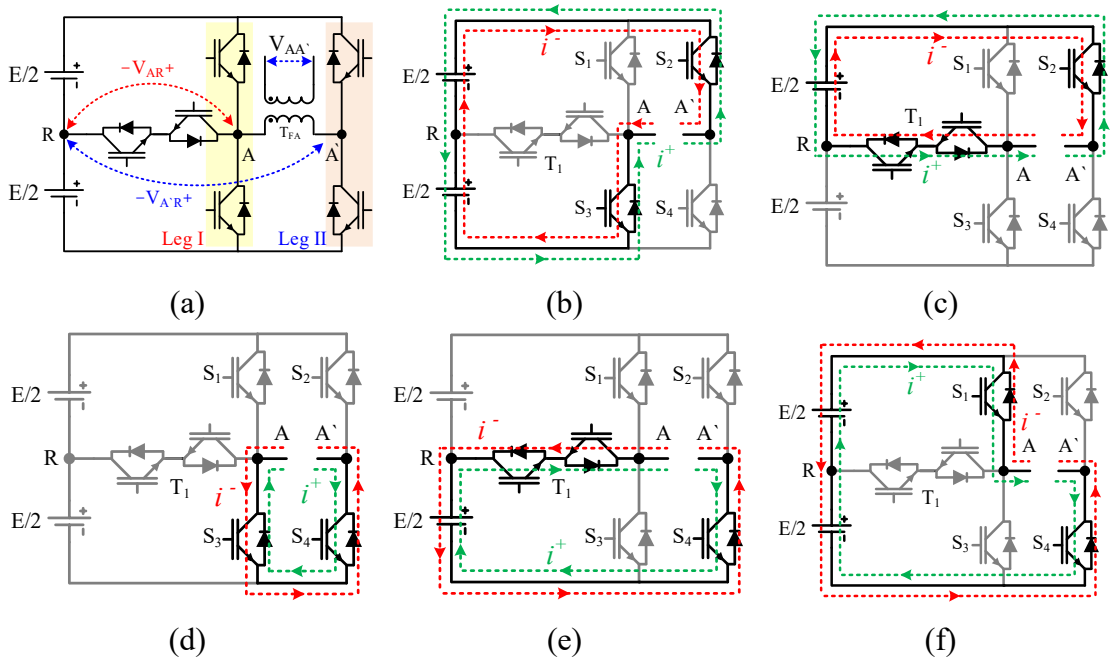


Figure 3.9: Operating concept of T_C. (a) Synthesising of $V_{AA`}$. (b) Mode I: $V_{AA`}$= -E. (c) Mode II: $V_{AA`}$= -0.5$E$. (d) Mode III: $V_{AA`}$= 0. (e) Mode IV: $V_{AA`}$= 0.5$E$. (f) Mode V: $V_{AA`}$= E.

3.3.3 Modulation strategies

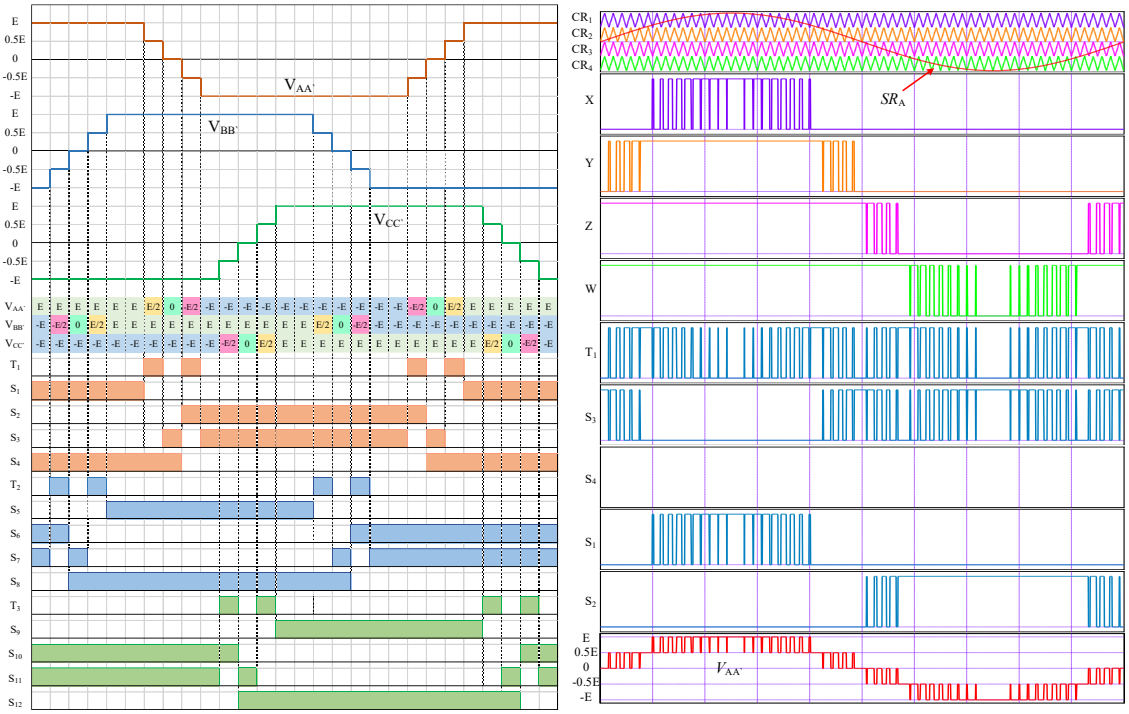
Table 3.3 lists the switching states of S_1-S_4 and T_1 in phase A of the proposed topology. Further, it shows the voltage $V_{AA`}$ and its two components $V_{AR}$ and $V_{A`R}$. Based on Table 3.3, the LFM and LSPWM are designed for the topology T_C.

Figure 3.10 (a) shows the LFM switching pattern accompanied by the three voltages $V_{AA`}$, $V_{BB`}$, and $V_{CC`}$. On the other hand, the LSPWM and key waveforms of phase A are shown in Figure 3.10 (b). To produce five levels, four carrier signals CR_1-CR_4 with level shift are required. These four level-shifted carrier signals are equal in their magnitude, frequency, and phase angle. They are compared with three modulation signals SR_A-SR_C, which are sinusoidal and have a phase shift of

120°, producing four controlling signals, *X*, *Y*, *Z*, and *W*. The switching pulses are generated by applying the logical operations in (3.20)-(3.23) on the *X*, *Y*, *Z*, and *W* signals, generating switched multilevel sinusoidal voltages at the output terminals.

Table 3.3: Switching states and the corresponding pole voltages (Phase A).

S_1	S_2	S_3	S_4	T_1	V_{AR}	$V_{A`R}$	$V_{A\,A`}$
ON	OFF	OFF	ON	OFF	**0.5E**	**-0.5E**	**E**
OFF	OFF	OFF	ON	ON	**0**	**-0.5E**	**0.5E**
OFF	OFF	ON	ON	OFF	**-0.5E**	**-0.5E**	**0**
ON	ON	OFF	OFF	OFF	**0.5E**	**0.5E**	**0**
OFF	ON	OFF	OFF	ON	**0**	**0.5E**	**-0.5E**
OFF	ON	ON	OFF	OFF	**-0.5E**	**0.5E**	**-E**



(a) (b)

Figure 3.10: Switching pattern and key waveforms of T_C. (a) LFM. (b) LSPWM.

$$S_1 = X \tag{3.20}$$

$$S_2, \overline{S_4} = \overline{Z} \tag{3.21}$$

$$S_3 = \left(\overline{Y} \cdot Z\right) + \overline{W} \tag{3.22}$$

$$T_1 = \left(\left(\overline{X} \cdot Y\right) + \overline{Z}\right) \cdot W \tag{3.23}$$

3.4 Proposed topology T_D

3.4.1 Circuit configuration

The circuit configuration of the proposed transformer-based inverter T_D is shown in Figure 3.11. It is a hybrid three-phase topology, being formed by connecting three T-type legs to three H-bridge inverters through three single-phase transformers. The proposed topology consists of two DC sources (V_1 and V_2), three transformers (T_{FA}, T_{FB}, and T_{FC}), and twenty-four switches (S_1-S_{24}). The twenty-four switches are used to implement eighteen unidirectional switches and three bidirectional switches. The proposed topology does not require any clamping diodes or flying capacitors in its operation. It can produce different voltage level count according to the selected transformer turns ratio β. For example, it produces seven voltage levels and nine voltage levels when selecting β to be 1 and 1.5, respectively. The proposed topology configuration keeps the maximum blocking voltage of the switches either below or equal to E, where E is the input DC-link voltage. The switches S_3, S_4, S_{11}, S_{12}, S_{19}, and S_{20} have a voltage stress of $0.5E$. Alternatively, the switches S_1, S_2, S_5-S_{10}, S_{13}-S_{18}, and S_{21}-S_{24} withstand a voltage stress of E.

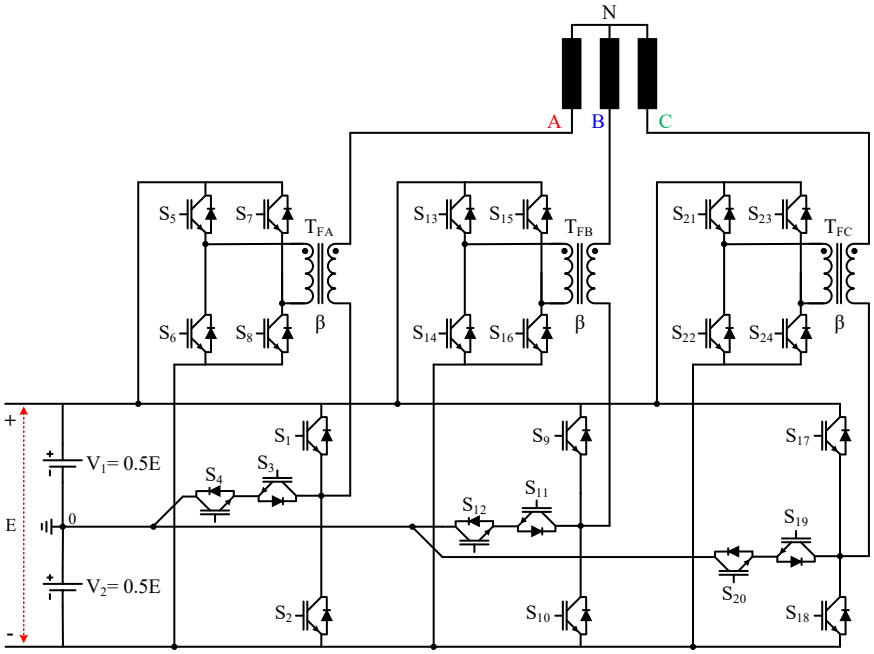


Figure 3.11: The circuit configuration of the proposed topology T_D.

The proposed topology can be extended to produce N voltage levels by adding more H-bridge cells in each phase leg, being connected through transformers, as shown in Figure 3.12. The blocking voltage of the switches is not a function of the

voltage levels count, so increasing the voltage level count does not increase the voltage stress across the switches. All H-bridge cells contribute to the pole voltage. For example, the pole voltage V_{A0} is synthesised by adding the cell voltages V_1, V_2, …, and V_n to the base voltage V_0 as expressed in (3.24).

$$V_{A0} = V_0 + \sum_{i=1}^{n} V_i \tag{3.24}$$

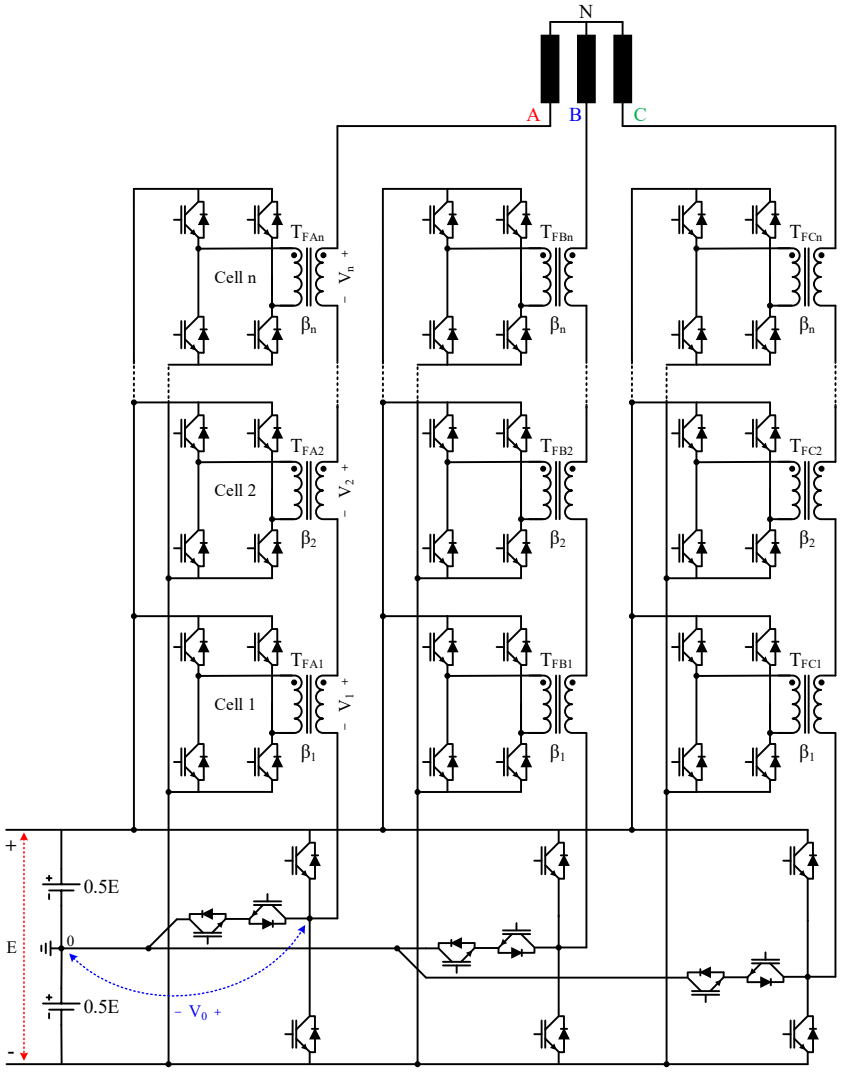


Figure 3.12: The *N*-level configuration of the proposed topology T_D.

The *N*-level configuration of the proposed inverter generates different voltage level counts according to the transformer turn ratio β while keeping the same component count. The generalized configuration has three cases, depending on β: A) symmetrical turns ratio (where $\beta_1 = \beta_2 = \ldots = \beta_n = 1$), B) asymmetrical binary turns ratio (where $\beta_1, \beta_2, \beta_3, \ldots$ are 1, 2, 4,…), C) asymmetrical ternary turns ratio (where $\beta_1, \beta_2, \beta_3, \ldots$ are 1.5, 4.5, 13.5,…). The relationships between the transformer count N_{Trf}, switch count N_{SW}, and the voltage level count N are presented in (3.25)-

(3.27), (3.28)-(3.30), and (3.31)-(3.33), for symmetrical, binary asymmetrical, and ternary asymmetrical turn ratios, respectively. For example, using six transformers (two per each phase leg) produces eleven, fifteen, twenty-seven voltage levels in the pole voltage for symmetrical, binary asymmetrical, ternary asymmetrical turn ratios, respectively. The component counts in (3.25)-(3.33) represent the total count in the three legs.

A) Symmetrical ratios: $\beta_1 = \beta_2 = \ldots = \beta_n = 1$

$$N = \frac{4N_{\text{Trf}}}{3} + 3, \quad N_{\text{Trf}} = 0, 3, 6, 9, 12, \ldots \tag{3.25}$$

$$N_{\text{SW}} = 3N + 3, \quad N = 3, 7, 11, 15, 19, 23, \ldots \tag{3.26}$$

$$N_{\text{Trf}} = \frac{3N - 9}{4}, \quad N = 3, 7, 11, 15, 19, 23, \ldots \tag{3.27}$$

B) Asymmetrical binary ratios: $\beta_1, \beta_2, \beta_3, \ldots$ are 1, 2, 4, …

$$N = 2^{\frac{N_{\text{Trf}}}{3}+2} - 1, \quad N_{\text{Trf}} = 0, 3, 6, 9, 12, \ldots \tag{3.28}$$

$$N_{\text{SW}} = 12\left(\frac{\ln(N+1)}{\ln(2)} - 1\right), \quad N = 3, 7, 15, 31, 63, 127, \ldots \tag{3.29}$$

$$N_{\text{Trf}} = 3\left(\frac{\ln(N+1)}{\ln(2)} - 2\right), \quad N = 3, 7, 15, 31, 63, 127, \ldots \tag{3.30}$$

C) Asymmetrical ternary ratios: $\beta_1, \beta_2, \beta_3, \ldots$ are 1.5, 4.5, 13.5, …

$$N = 3\,(3^{\frac{N_{\text{Trf}}}{3}}), \quad N_{\text{Trf}} = 0, 3, 6, 9, 12, \ldots. \tag{3.31}$$

$$N_{\text{SW}} = 12\left(\frac{\ln(\frac{N}{3})}{\ln(3)} + 1\right), \quad N = 3, 9, 27, 81, 243, 729, \ldots \tag{3.32}$$

$$N_{\text{Trf}} = 3\left(\frac{\ln(\frac{N}{3})}{\ln(3)}\right), \quad N = 3, 9, 27, 81, 243, 729, \ldots \tag{3.33}$$

3.4.2 Operating concept

The operating concept can be explained based on the generation of the pole voltages V_{A0}, V_{B0}, and V_{C0}. Considering V_{A0} as an example, it is synthesized by adding two voltage components: V_0 and V_1, as shown in (3.34) and Figure 3.13 (a). V_0 is the voltage between the midpoint of the T-type leg and the reference point 0, and V_1 is the secondary voltage of transformer T_{FA}. Both two voltage components can have three different voltage levels: V_0 has 0.5E, 0, and -0.5E voltages, while V_1 has three levels of βE, 0, and -βE.

$$V_{A0} = V_0 + V_1 \tag{3.34}$$

The transformer turns ratio β can have different values: A) Case A, β =1, producing three voltage levels of E, 0, and -E in the voltage component V_1; B) Case B, β =1.5, producing three voltage levels of 1.5E, 0, and -1.5 E in V_1. Although both cases keep producing the same number of voltage levels, the maximum reachable voltage in case B is higher than that in case A. Accordingly, the pole voltage can have different voltage level counts: seven levels in the case A (0, ±0.5E, ±E, and ±1.5E) and nine levels for case B (0, ±0.5E, ±E, ±1.5E, and ±2E).

Figures 3.13 (b)-(h) show seven different operating modes of the proposed topology to produce seven voltage levels in the pole voltage V_{A0} when β is equal to 1. For instance, in Figure 3.13 (b), Mode I describes the required ON/OFF switches for producing 1.5E, in which the switches S_1, S_4, S_5, and S_8 must be ON while S_2, S_3, S_6, and S_7 are OFF. The remaining six voltage levels can be achieved by following the operating modes II to VII, as shown in Figures 3.13 (c) to (h), respectively. It is worth noting that the mentioned operating modes are selected to produce the targeted voltage level without causing a short-circuit across the input DC sources. Therefore, some combinations of switches cannot be set ON. For example, in phase leg A, the following combinations are not used in the modulation control of the proposed topology: (S_1, S_2), (S_1, S_3, S_4), (S_2, S_3, S_4), (S_5, S_6), and (S_7, S_8).

3.4.3 Modulation strategy

The LFM scheme is selected to control the proposed topology output voltage due to its simplicity. However, other modulation schemes can be used as well. The LFM scheme is based on Table 3.4, showing the switching states of leg-A switches

(S_1-S_8) and the corresponding output voltages V_0, V_1, and V_{A0}. Table 3.4 lists the switching states when β is 1, generating seven voltage levels in the pole voltage V_{A0}. Alternatively, nine voltage levels are generated when β is 1.5 as detailed in paper VI.

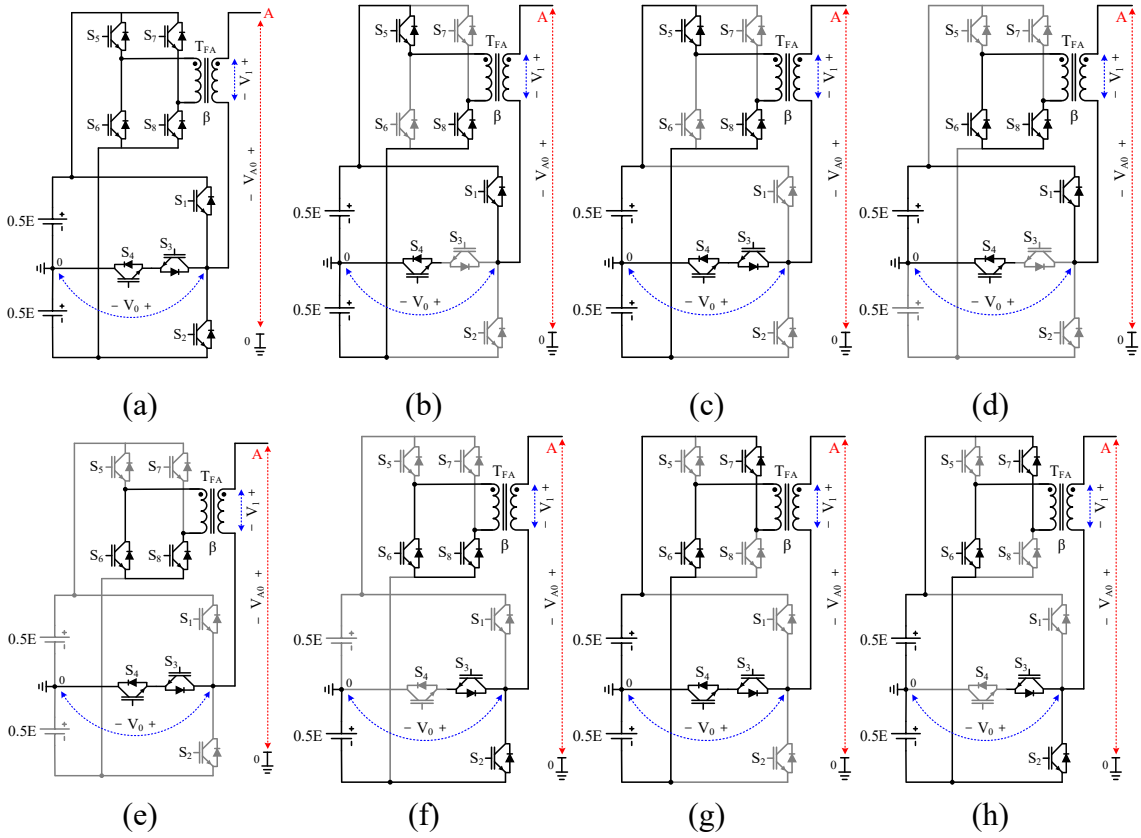


Figure 3.13: Operating concept of T_D when β is 1. (a) Synthesising of the pole voltage V_{A0}. (b) Mode I: V_{A0}= 1.5E. (c) Mode II: V_{A0}= E. (d) Mode III: V_{A0}= 0.5E. (e) Mode IV: V_{A0}= 0. (f) Mode V: V_{A0}= -0.5E. (g) Mode VI: V_{A0}= -E. (h) Mode VII: V_{A0}= -1.5E.

Table 3.4: Output voltages and the corresponding switching states when β is 1.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_0	V_1	V_{A0}
ON	OFF	OFF	ON	ON	OFF	OFF	ON	**0.5E**	**E**	**1.5E**
OFF	OFF	ON	ON	ON	OFF	OFF	ON	**0**	**E**	**E**
ON	OFF	OFF	ON	OFF	ON	OFF	ON	**0.5E**	**0**	**0.5E**
ON	OFF	OFF	ON	ON	OFF	ON	OFF	**0.5E**	**0**	**0.5E**
OFF	ON	ON	OFF	ON	OFF	OFF	ON	**-0.5E**	**E**	**0.5E**
OFF	OFF	ON	ON	ON	OFF	ON	OFF	**0**	**0**	**0**
OFF	OFF	ON	ON	OFF	ON	OFF	ON	**0**	**0**	**0**
OFF	ON	ON	OFF	OFF	ON	OFF	ON	**-0.5E**	**0**	**-0.5E**
OFF	ON	ON	OFF	ON	OFF	ON	OFF	**-0.5E**	**0**	**-0.5E**
ON	OFF	OFF	ON	OFF	ON	ON	OFF	**0.5E**	**-E**	**-0.5E**
OFF	OFF	ON	ON	OFF	ON	ON	OFF	**0**	**-E**	**- E**
OFF	ON	ON	OFF	OFF	ON	ON	OFF	**-0.5E**	**-E**	**-1.5E**

Figure 3.14 shows the generation of the switching signals for the leg-A switches when β is 1. To produce the seven-level pole voltage as shown in the last trace of Figure 3.14, a sinusoidal reference signal SR_A and six offset signals ($\pm R_1$, $\pm R_2$, and $\pm R_3$) are required. The reference signal can be varied from 0 to the maximum of V_P, while the offset signals can be expressed as in (3.35)-(3.37) [87].

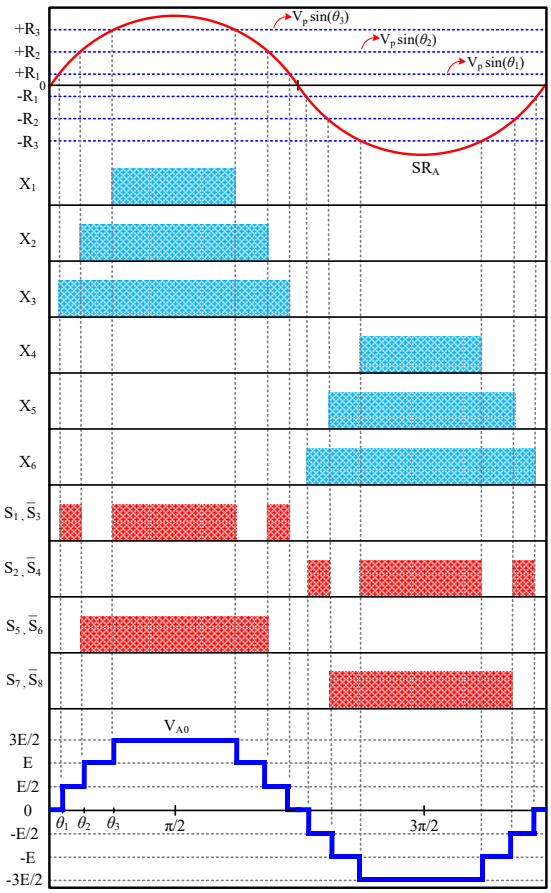


Figure 3.14: Switching signals generation and the pole voltage V_{A0} at β of 1.

$$\pm R_1 = V_p \sin(\theta_1) \tag{3.35}$$

$$\pm R_2 = V_p \sin(\theta_2) \tag{3.36}$$

$$\pm R_3 = V_p \sin(\theta_3) \tag{3.37}$$

where θ_1-θ_3 are the transition angles between voltage levels as marked in the pole voltage waveform in Figure 3.14. These transition angles can be calculated using (3.38) [87]. Further, (3.38) can be used for computing the transition angles of any number of voltage level produced by the N-level configuration in Figure 3.12. In the other words, Figure 3.14 can be extended for producing the required switching

pulses for N voltage levels by using (3.38) to determine N-1 offset signals ($\pm R_1$, $\pm R_2$, $\pm R_3$, ….and $\pm R_{(N-1)/2}$).

$$\theta_m = \sin^{-1}\left(\frac{2m-1}{N}\right),\ m = 1,\ 2,\ldots,\frac{N-1}{2},\quad 0 \le \theta_m \le \frac{\pi}{2} \tag{3.38}$$

Six primary signals X_1-X_6 are derived when comparing the reference signal SR_A with six offset signals. These six primary signals are the inputs for the Boolean operators, being used to achieve the switching states in Table 3.4, as expressed in (3.39)-(3.42). The symbols "+" and "×" in (3.39)-(3.42) correspond to the logical operators "OR" and "AND", respectively.

$$S_1,\ \overline{S_3} = X_1 + (\overline{X_2} \times X_3) \tag{3.39}$$

$$S_2,\ \overline{S_4} = X_4 + (\overline{X_5} \times X_6) \tag{3.40}$$

$$S_5,\ \overline{S_6} = X_2 \tag{3.41}$$

$$S_7,\ \overline{S_8} = X_5 \tag{3.42}$$

Chapter 4

Results and discussions

In this chapter, the operability and performance of the proposed topologies are numerically verified in MATLAB/Simulink, and then experimentally validated through an in-house test setup. Selected results are presented and discussed in the following sections, while the full results are detailed in papers II to VI. Further, a summary of the comparative studies in the mentioned papers between the proposed topologies and recently developed MLIs are provided to prove their key features.

4.1 In-house test setup

Figure 4.1 shows the experimental setup for validating the proposed topologies. It consists of three programmable DC voltage sources (Chroma, 62024P-100-50), one low-power DC source for control circuits (Rohde & Schwarz, HMP4040), three single-phase transformers (Triad Magnetics, VPM240-20800), dSPACE MicroLabBox controller, current and voltage probes, digital oscilloscope

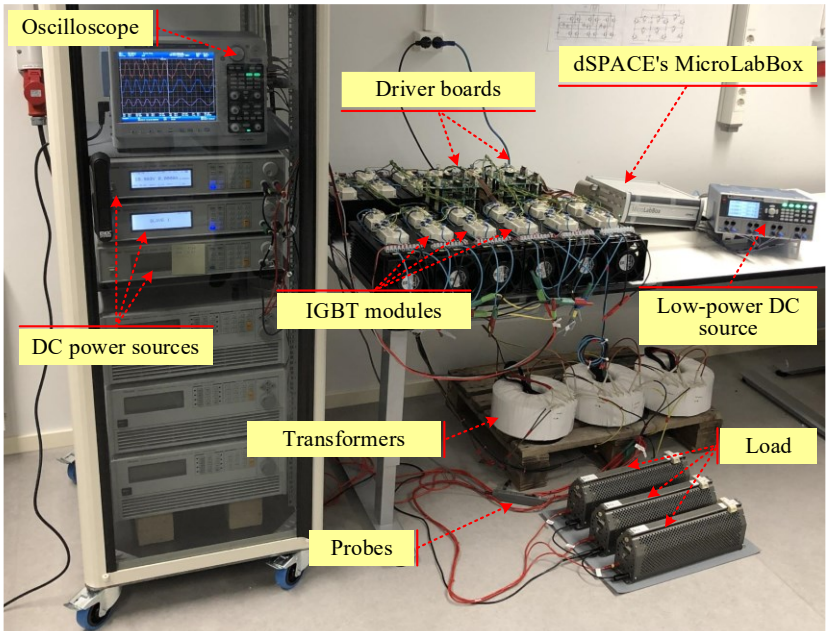


Figure 4.1: The in-house experimental setup.

(Yokogawa, DL850EV), resistive-inductive (R-L) loads, and the inverter prototype. The inverter prototype is constructed using twenty-four IGBT modules (SEMIKRON, SKM300GA12E4) associated with gate-driver boards (SEMIKRON, SKHI 10/12 R). The captured components in Figure 4.1 are not used at the same time to validate the proposed topologies: transformers used only in topologies C and D, three DC sources used in topology A, two DC sources used in topologies B-D, and eighteen, twelve, and twenty-four switches utilized in topologies (A and C), B, and D, respectively. The low-power DC source, dSPACE controller, loads, and measurement devices are commonly used in all topologies.

4.2 Key results of topology T_A

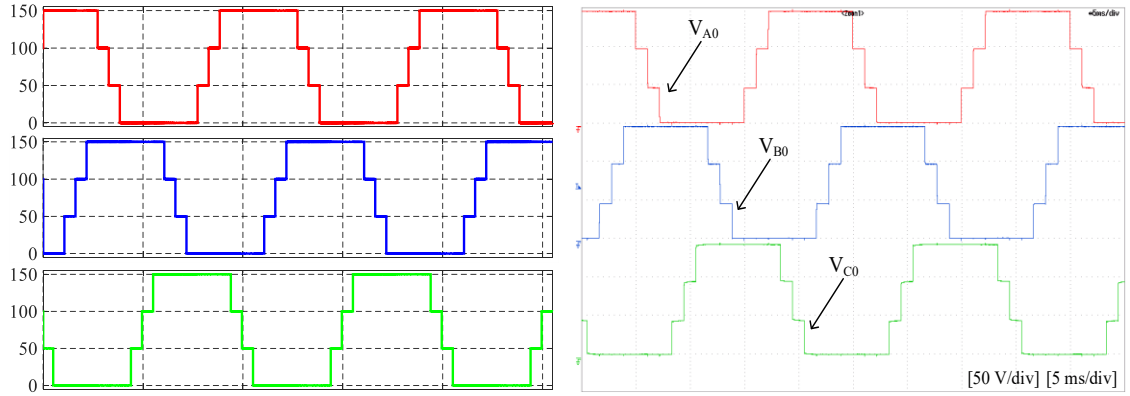
Several simulations and experimental tests were carried out and presented in this section to verify the operating concept of the proposed topology T_A. It is worth to clarify that the included results in this section are for both configurations in Figure 3.1, MSC and SSC. The MSC is first numerically verified and then experimentally validated through the in-house test setup shown in Figure 4.1. The SSC results are obtained by using the OPAL-RT real-time simulator OP5707. Table 4.1 lists the system specifications of the simulation and experimental validations.

Table 4.1: System specifications for simulation and experimental validations.

Description	Value	Unit
DC-link voltage	150	V
DC-link capacitors, for SSC	1000	µF
Load resistor	40	Ω
Load inductor	100	mH
Switching frequency	2	kHz
Modulation frequency	50	Hz
Modulation index, LSPWM	0.9	–
Modulator signals H, LFM	±0.35	–
Sampling time	15	µs

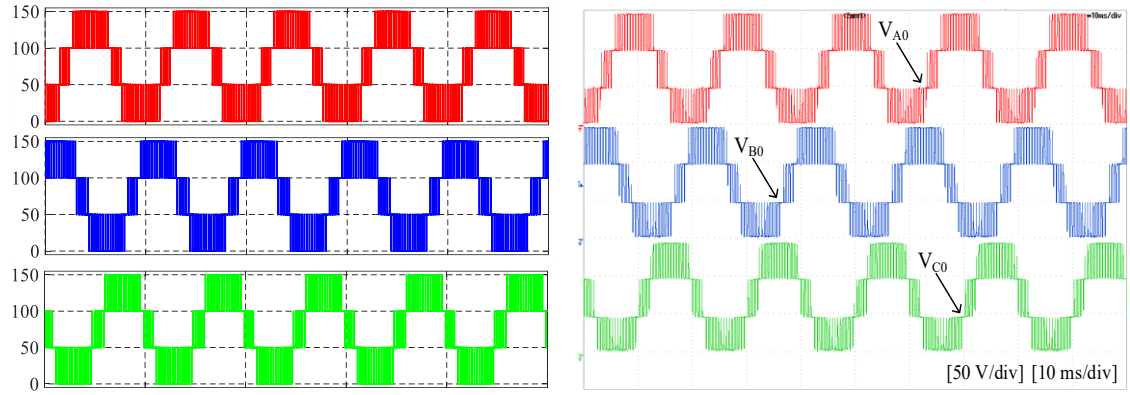
The LFM and LSPWM switching schemes are executed using the digital controller, producing the required switching pulses for the different switches in the T_A. These switching pulses control the corresponding switches to produce pole voltages with specific phase angles and level counts, as shown in Figures 4.2 and 4.3. Figures 4.2 (a) and (b) depict the simulation and experimental results for the pole voltages V_{A0}, V_{B0}, and V_{C0} when using the LFM scheme. Each pole voltage has three voltage levels of 50 V and a phase shift of 120° to the adjacent pole voltages. Further, the consistent pole voltage waveforms are shown in Figures 4.3

(a) and (b) when using LSPWM switching scheme. These pole voltages are the key waveforms for synthesising both line and phase voltages, as detailed in paper II.



(a) (b)

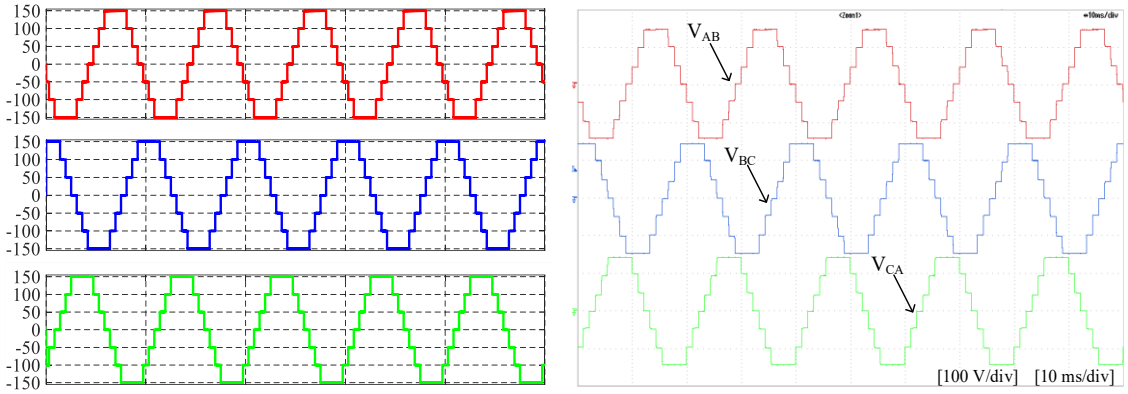
Figure 4.2: Pole voltages V_{A0}, V_{B0}, and V_{C0} using LFM. (a) Simulation. (b) Experimental.



(a) (b)

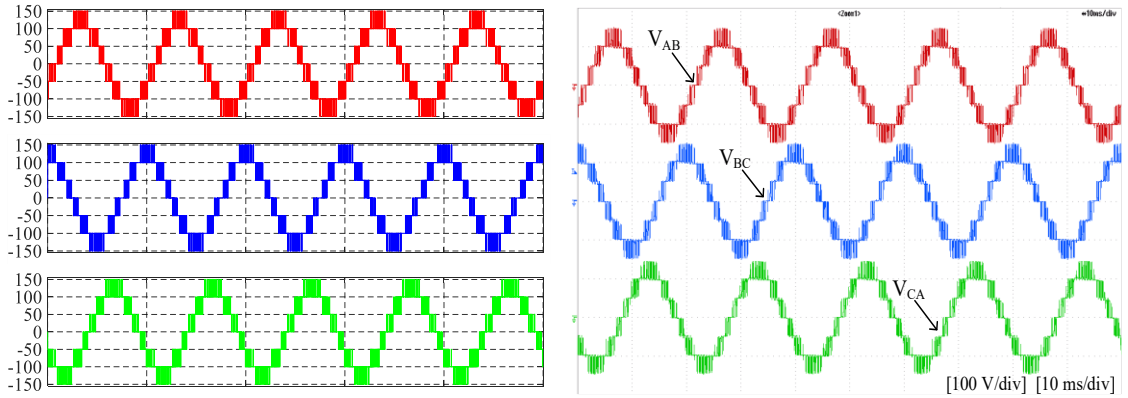
Figure 4.3: Pole voltages V_{A0}, V_{B0}, and V_{C0} using LSPWM. (a) Simulation. (b) Experimental.

Figures 4.4 and 4.5 show the line voltages V_{AB}, V_{BC}, and V_{CA} when using LFM and LSPWM schemes, respectively. As seen in Figure 4.4 and 4.5, the proposed topology generates seven-level waveforms: three positive levels of 150 V, 100 V, and 50 V, zero-voltage level, and three negative levels of -50 V, -100 V, and -150 V. These line voltages are balanced and identical in both simulation and experimental tests. The proposed topology is further tested on an R-L load of $50.86\angle 42.3°$ Ω (R= 40 Ω and L= 100 mH). Figures 4.6 and 4.7 illustrate the obtained waveforms of the line voltage V_{AB}, phase voltage V_{AN} and load current I_{AN} for LFM and LSPWM schemes, respectively.



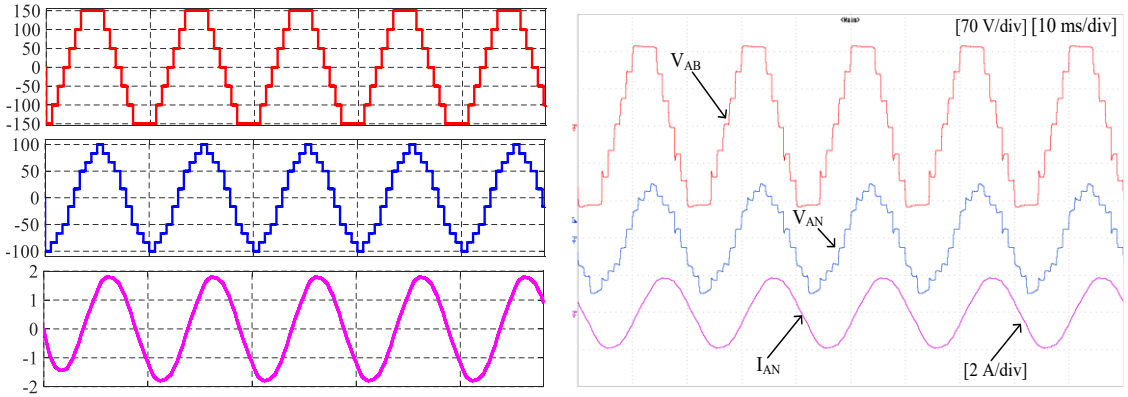
(a) (b)

Figure 4.4: Line voltages V_{AB}, V_{BC}, and V_{CA} using LFM. (a) Simulation. (b) Experimental.



(a) (b)

Figure 4.5: Line voltages V_{AB}, V_{BC}, and V_{CA} using LSPWM. (a) Simulation. (b) Experimental.

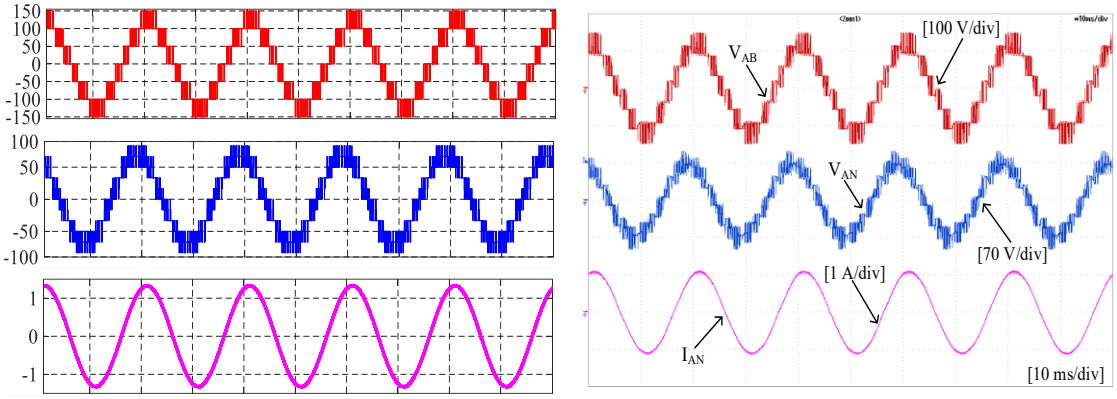


(a) (b)

Figure 4.6: Obtained V_{AB}, V_{AN}, and I_{AN} for R-L load using LFM. (a) Simulation. (b) Experimental.

Figures 4.8 and 4.9 show the key results of the SSC configuration of the T_A. Figure 4.8 shows the line voltage V_{AB}, phase voltage V_{AN} and the load current I_{AN} when an R-L load is connected to the proposed topology. Further, Figure 4.9 illustrates the effectiveness of the applied voltage-balance control of the DC-link capacitors C_1, C_2, and C_3. The three capacitor voltages V_{C1}, V_{C2}, and V_{C3} are

balanced for a wide range of modulation indices (*MIs*) as shown in Figure 4.9 (a), in which the *MI* changes from 0.9 to 0.3, keeping an acceptable tolerance of the capacitor voltages (V_{C1}= 51.21 V, V_{C2}= 50.20 V, and V_{C3}= 49.03 V). Further, Figure 4.9 (b) shows that the voltage-balance control can balance the capacitor voltages nearby 50 V (V_{C1}= 50.58 V, V_{C2}= 50.48 V, and V_{C3}= 49.37 V) while changing the load value by 100%.



(a) (b)

Figure 4.7: Obtained V_{AB}, V_{AN}, and I_{AN} for R-L load using LSPWM. (a) Simulation. (b) Experimental.

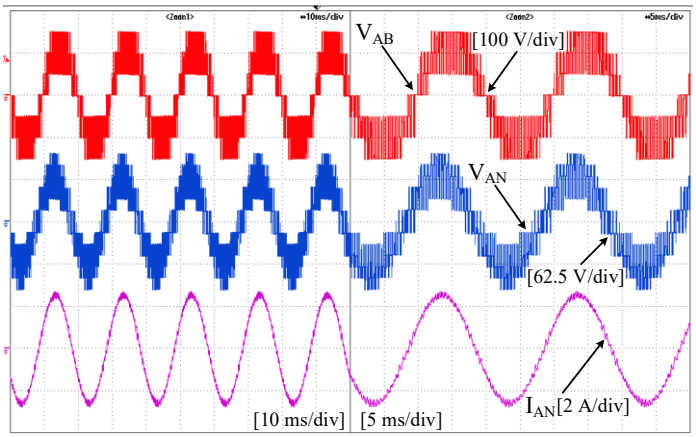
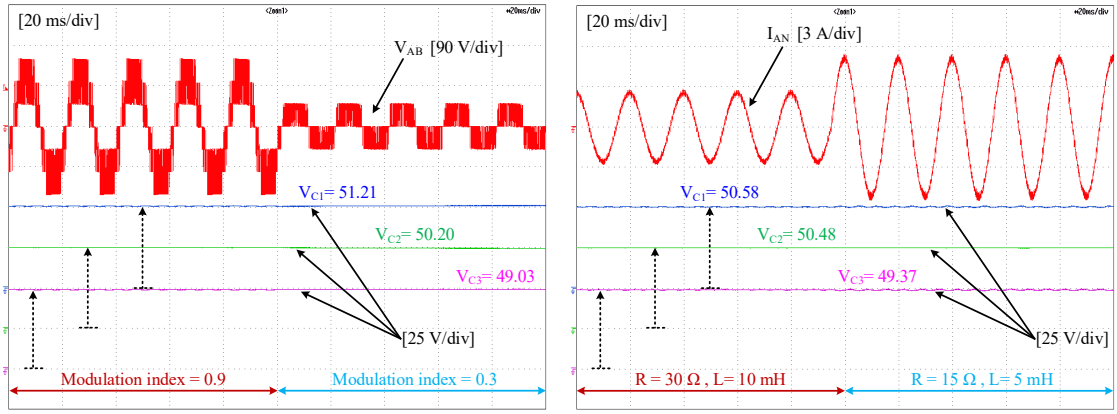


Figure 4.8: Obtained V_{AB}, V_{AN}, and I_{AN} for the SSC when feeding R-L load (using OP5707).

The loss analysis of the proposed topology is detailed in paper II, while key figures are provided hereafter. The switching frequency (F_S) and output power (P_{out}) are varied to study their effects on the conversion efficiency. F_S is changed from 2 kHz to 8 kHz in steps of 3 kHz, while P_{out} is changed from 0.5 kW to 5 kW in steps of 0.5 kW. The efficiency increases when raising the load, and decreases when F_S rises as shown in Figure 4.10. For example, at F_S of 5 kHz, the efficiency is increased from 96.65% to 99.15% when increasing the load from 0.5 kW to 5 kW. Contrarily, it is decreased from 99.19% to 98.41% when increasing F_S from

2 kHz to 8 kHz at 2.5 kW load, matching well power-loss calculations in literature [88-91]. It is emphasized that all switching device parameters and the other system specifications such as input voltage, power factor, and modulation index are kept constant while studying the effects of the switching frequency or load on the total efficiency.



(a) (b)

Figure 4.9: Dynamic results of the SSC (using OP5707). (a) Changing the *MI* from 0.9 to 0.3: V_{AB}, V_{C1}, V_{C2}, and V_{C3}. (b) Changing the load value by 100%: I_{AN}, V_{C1}, V_{C2}, and V_{C3}.

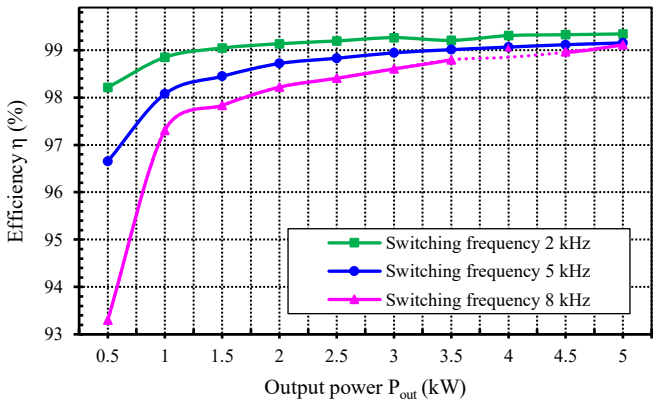


Figure 4.10: Conversion efficiency at different output powers and switching frequencies.

As explained in paper II, both switching loss (P_{sw}) and conduction loss (P_{con}) are considered as the dominant losses in semiconductor devices. Therefore, the power loss distribution of individual switches is studied and subdivided into switching and conduction losses. Figure 4.11 shows the power loss distribution among different switches at F_S of 5 kHz and P_{out} of 2.5 kW. Since the load and switching frequency are constant, the conduction and switching losses are directly proportional to the conduction period and switching voltage, respectively. For example, the switching losses in switches S_1, S_5, S_9 are higher than those of the remaining switches because they block higher voltages. The switches S_4, S_8, and

S_{12} have the lowest conduction loss since their conduction periods are shorter than those of other switches.

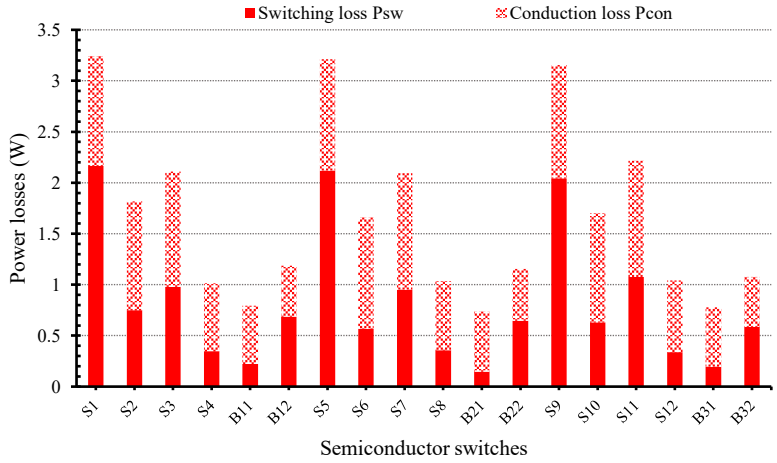


Figure 4.11:Power loss distribution in the switches at F_S of 5 kHz and P_{out} of 2.5 kW.

4.3 Key results of topology T_B

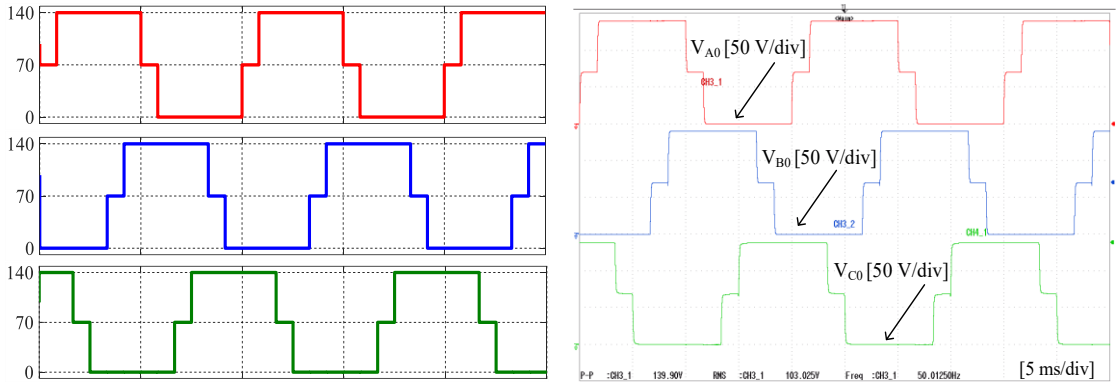
The low-voltage configuration of the proposed topology T_B shown in Figure 3.4 (a) is used to verify its performance under LFM and LSPWM schemes. Selected simulation and experimental results are provided in this section. Further, the key results of its efficiency and loss distribution among switches are presented. More details can be found in paper IV. Table 4.2 lists system specifications for simulations and experimental tests.

Table 4.2: System specifications for simulations and experimental tests.

Description	**Value**	**Unit**
DC-link voltage	140	V
Load resistor	30	Ω
Load inductor	100	mH
Switching frequency	1000	Hz
Modulation frequency	50	Hz
Modulation index, LSPWM	0.9	–
Modulator signal H, LFM	0.27	–
Sampling time	15	µs

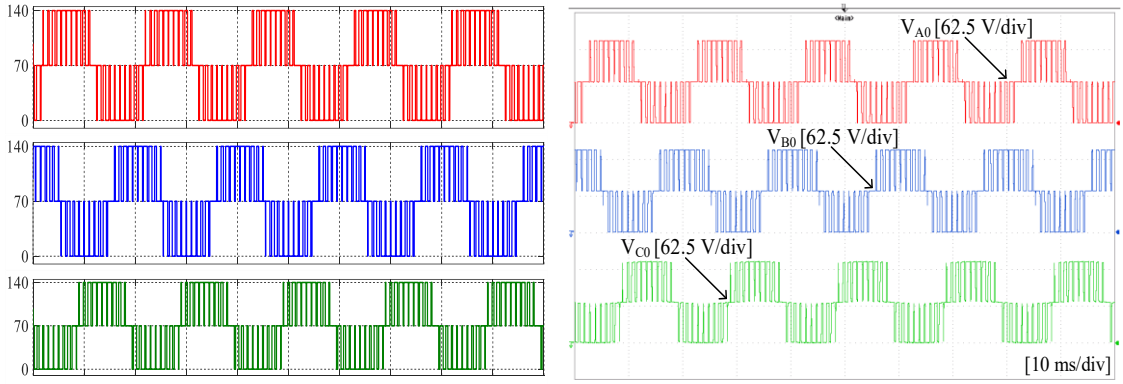
Figures 4.12 (a) and 4.13 (a) show the simulation waveforms of the pole voltages V_{A0}, V_{B0}, and V_{C0} for LFM and LSPWM, respectively. Each waveform has three voltage levels of 0, E, and $2E$, in addition to a phase shift of 120° for the two other pole voltages. The waveforms of experimental tests are presented in Figures 4.12 (b) and 4.13 (b), matching well the obtained simulation results. Figures 4.14 and

4.15 depict the balanced three-phase line voltages V_{AB}, V_{BC}, and V_{CA}, where five voltage levels of $2E$, E, 0, $-E$, and $-2E$ were produced by maintaining the pole voltages in the same conditions as shown in Figures 4.12 and 4.13.



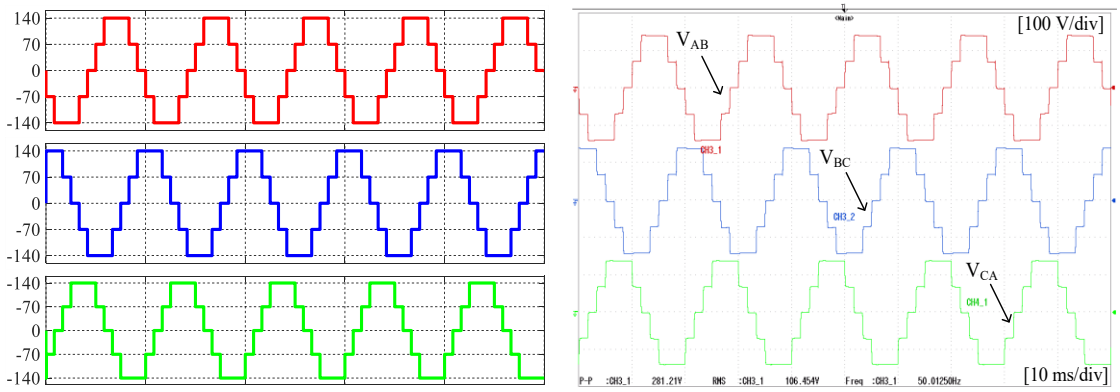
(a) (b)

Figure 4.12: Pole voltages V_{A0}, V_{B0}, and V_{C0} using LFM. (a) Simulation. (b) Experimental.



(a) (b)

Figure 4.13: Pole voltages V_{A0}, V_{B0}, and V_{C0} using LSPWM. (a) Simulation. (b) Experimental.

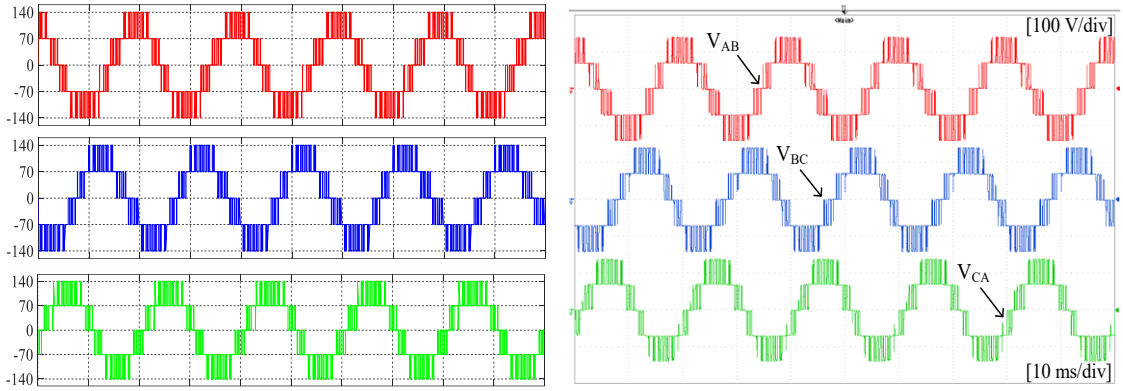


(a) (b)

Figure 4.14: Line voltages V_{AB}, V_{BC}, and V_{CA} using LFM. (a) Simulation. (b) Experimental.

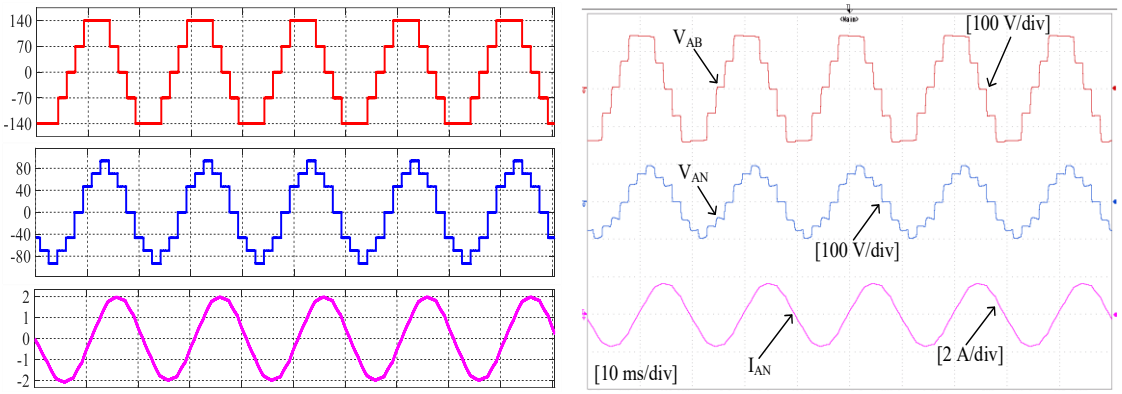
An R-L load is used to verify the performance of the proposed inverter under loading conditions. Figures 4.16 and 4.17 illustrate the obtained results when using

a load with a lagging power factor of 0.7. Further, Figures 4.16 and 4.17 show the five-level line voltage V_{AB} in the first trace, while the phase voltage V_{AN} and load current I_{AN} are shown in the second and third traces, respectively.



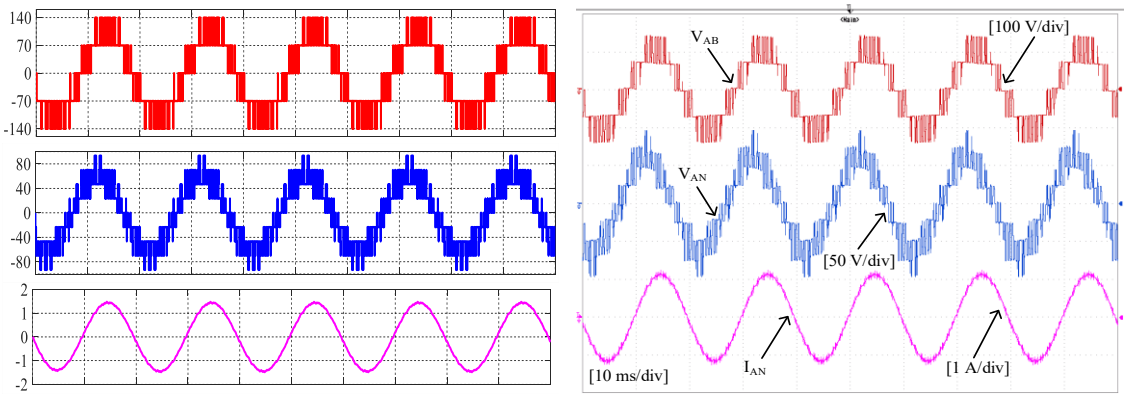
(a) (b)

Figure 4.15: Line voltages V_{AB}, V_{BC}, and V_{CA} using LSPWM. (a) Simulation. (b) Experimental.



(a) (b)

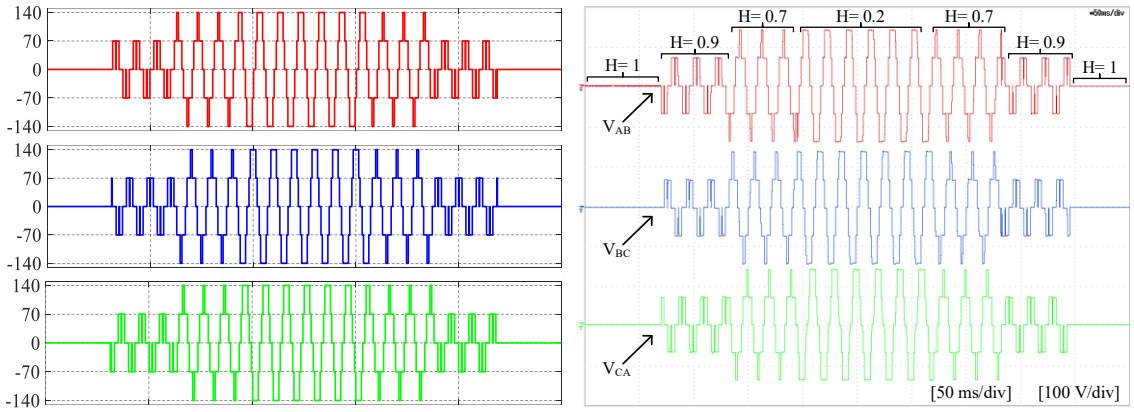
Figure 4.16: V_{AB}, V_{AN}, and I_{AN} for R-L load using LFM. (a) Simulation. (b) Experimental.



(a) (b)

Figure 4.17: V_{AB}, V_{AN}, and I_{AN} for R-L load using LSPWM. (a) Simulation. (b) Experimental.

Although the LFM scheme uses lower frequency signals for generating the switching pulses, the LSPWM switching scheme has a higher degree of flexibility. In the LSPWM, the output voltage frequency, RMS, and the number of levels can be controlled online by changing the frequency and magnitude of the modulation signal. In the LFM scheme, the proposed modulator H is integrated into the switching algorithm to add a degree of freedom for changing the output level count and RMS value while the frequency of the output voltage is changed by using the sinusoidal modulation signals. Figures 4.18 (a) and (b) show the simulation and experimental line voltage waveforms at different values of the modulator H. By changing H from 1 to 0, the RMS value of the line voltage is varied from 0% to 81.6% of the DC-link voltage. Further, the line voltage has zero-, three-, and five levels when H is 1, 0.9, and 0.2, respectively. Therefore, the proposed topology can produce the output voltage with variable magnitudes, frequency, and level counts for both the LSPWM and LFM.



(a) (b)

Figure 4.18: Line voltages V_{AB}, V_{BC}, and V_{CA} for different values of H. (a) Simulation. (b) Experimental.

The efficiency of the proposed topology and the loss distribution in the switches are detailed in paper IV, including the system specifications and the IGBT module parameters. The loss distribution of different switches is shown in Figure 4.19, where the losses are divided into conduction loss and switching loss. The conduction period and the blocking voltage of the switch have the main effects on the conduction loss and switching loss when the switching frequency and load are kept constant. For example, S_1, S_5, and S_9 have voltage stresses of $2E$, so their switching losses are higher than the other switches. On the other hand, S_2, S_6, and S_{10} have the highest conduction loss because their conduction durations are the longest among switches. The performance of the proposed topology is investigated

by changing the switching frequency and load while keeping all other variables constant. Figure 4.20 shows the efficiency variation when increasing the load from 10% to a full load of 4 kW in steps of 10% at the switching frequency of 5 kHz. The efficiency increases from 95.89% to 99.06% when the load is increased from 10% to 100% of the rated power. Figure 4.20 also shows the effect of increasing the switching frequency from 1 kHz to 10 kHz on the converter efficiency at full load. The efficiency decreases from 99.35% at 1 kHz to 98.71% at 10 kHz.

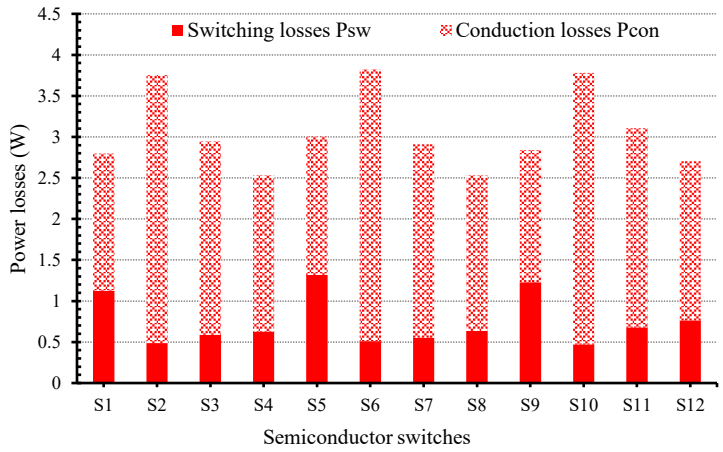


Figure 4.19: Loss distribution in various switches at P_{out} = 4 kW and F_S of 5 kHz.

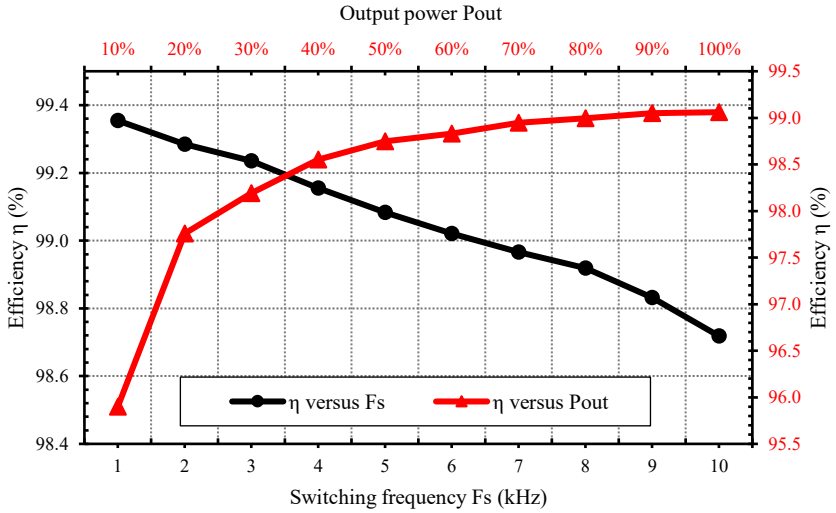


Figure 4.20: Efficiency at different loads and switching frequencies.

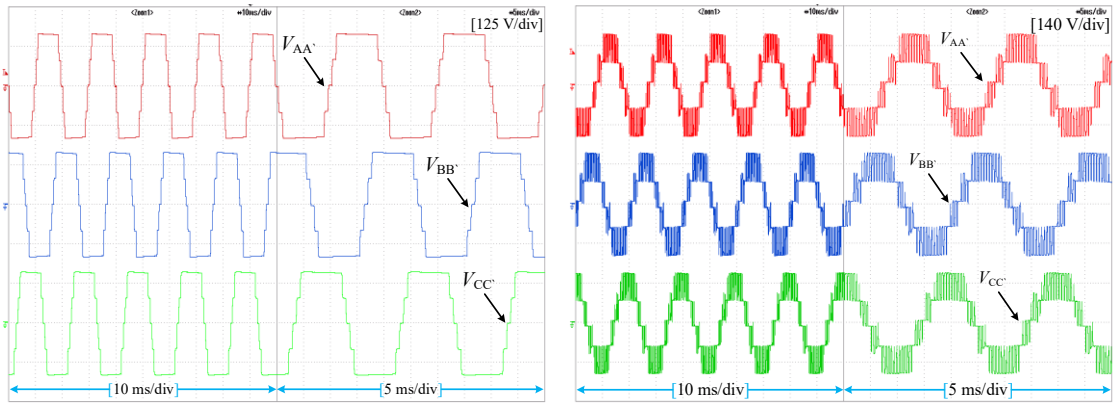
4.4 Key results of topology T_C

The five-level configuration of the proposed topology T_C is used to validate its operating principle and demonstrate its key waveforms. This section gives some of the obtained experimental results, while the simulation verifications are detailed in paper V. Table 4.3 shows the system parameters for experimental validation.

Table 4.3: System specifications for experimental validation.

Description	Value	Unit
DC-link voltage	180	V
Load resistor	100	Ω
Load inductor	100	mH
Switching frequency	2000	Hz
Modulation frequency	50	Hz
Modulation index, LSPWM	0.95	–
Sampling time	30	µs

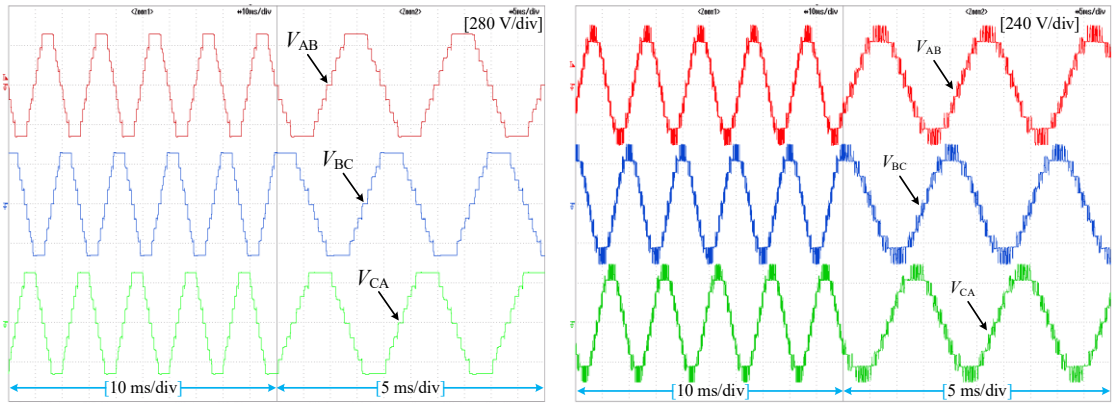
The operating principle of T_C is based on generating three five-level primary voltages $V_{AA'}$, $V_{BB'}$, and $V_{CC'}$ across the primary windings of transformers T_{FA}, T_{FB}, and T_{FC}, respectively. The three primary voltages are depicted in Figure 4.21, including five voltage levels of 0, ±0.5E, and ±E, where E=180 V. Figures 4.21 (a) and (b) show the generated waveforms under LFM and LSPWM control, respectively. Due to the 120° phase-shift between the primary voltages, subtracting any adjacent two voltages produces nine-level line voltages. Figure 4.22 shows the line voltages V_{AB}, V_{BC}, and V_{CA} for both modulation schemes, where each voltage has nine different voltage levels of 0, ±0.5E, ±E, ±1.5E, and ±2E.



(a) (b)

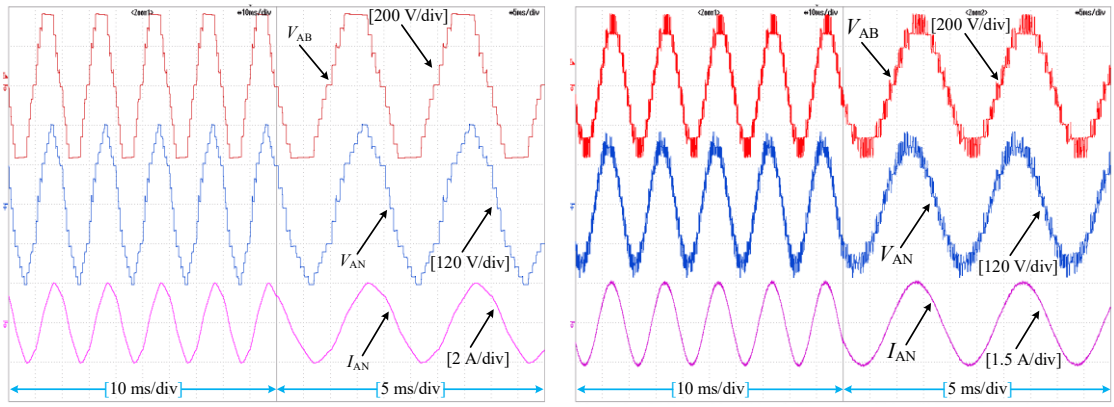
Figure 4.21: Experimental waveforms of the primary voltages $V_{AA'}$, $V_{BB'}$, and $V_{CC'}$. (a) LFM. (b) LSPWM.

The proposed topology is tested when supplying power to a load of 100 Ω and 100 mH. Figure 4.23 depicts the waveforms of V_{AB}, V_{AN}, and I_{AN} in the first, second, and third trace, respectively. It is noted that the phase voltage V_{AN} has lower voltage levels in the LFM scheme than those of LSPWM. It has thirteen and fifteen levels for LFM and LSPWM, respectively, as shown in Figures 4.23 (a) and (b). LSPWM has higher levels due to higher voltage combinations as compared to LFM, as detailed in paper III for T_B.



(a) (b)

Figure 4.22: Experimental waveforms of the line voltages V_{AB}, V_{BC}, and V_{CA}. (a) LFM. (b) LSPWM.



(a) (b)

Figure 4.23: Experimental waveforms of V_{AB}, V_{AN}, and I_{AN} for R-L load. (a) LFM. (b) LSPWM.

4.5 Key results of topology T_D

This section presents a numerical verification and experimental validation of the proposed topology T_D. The circuit configuration in Figure 3.11 is used to evaluate the T_D operation, and Table 4.4 lists the system parameters in simulation and experimental tests. The proposed topology is verified under LFM due to its simplicity, but other switching schemes can be used to control its output voltages.

Table 4.4: System specifications for simulation and experimental verification.

Description	**Value**	**Unit**
DC-link voltage	100	V
Load resistor	50	Ω
Load inductor	100	mH
Modulation frequency	50	Hz
Sampling time	20	µs
Transformer turns ratio β	1	–

The transformer turns ratio β affects the output voltage level count as detailed in paper VI. The proposed inverter can produce seven and nine voltage levels at β of 1 and 1.5, respectively. Figure 4.24 shows the voltage waveforms of the proposed inverter when selecting the turns ratio β of 1, while obtained results at β of 1.5 can be found in paper VI. Figure 4.24 (a) illustrates the synthesized pole voltage V_{A0}, being obtained by adding V_1 to V_0. Figure 4.24 (b) shows the three pole voltages V_{A0}, V_{B0}, and V_{C0}. The output line voltages V_{AB}, V_{BC}, and V_{CA}, are presented in Figure 4.24 (c), showing that the line voltages can have thirteen different voltage levels of 0, ±0.5E, ±E, ±1.5E, ±2E, ±2.5E, and ±3E. Figure 4.24 (d) shows the output waveforms when connecting an R-L load to the inverter outputs, where the line voltage V_{AB}, phase voltage V_{AN}, and load current I_{AN} are shown in the first, second, and the third trace, respectively.

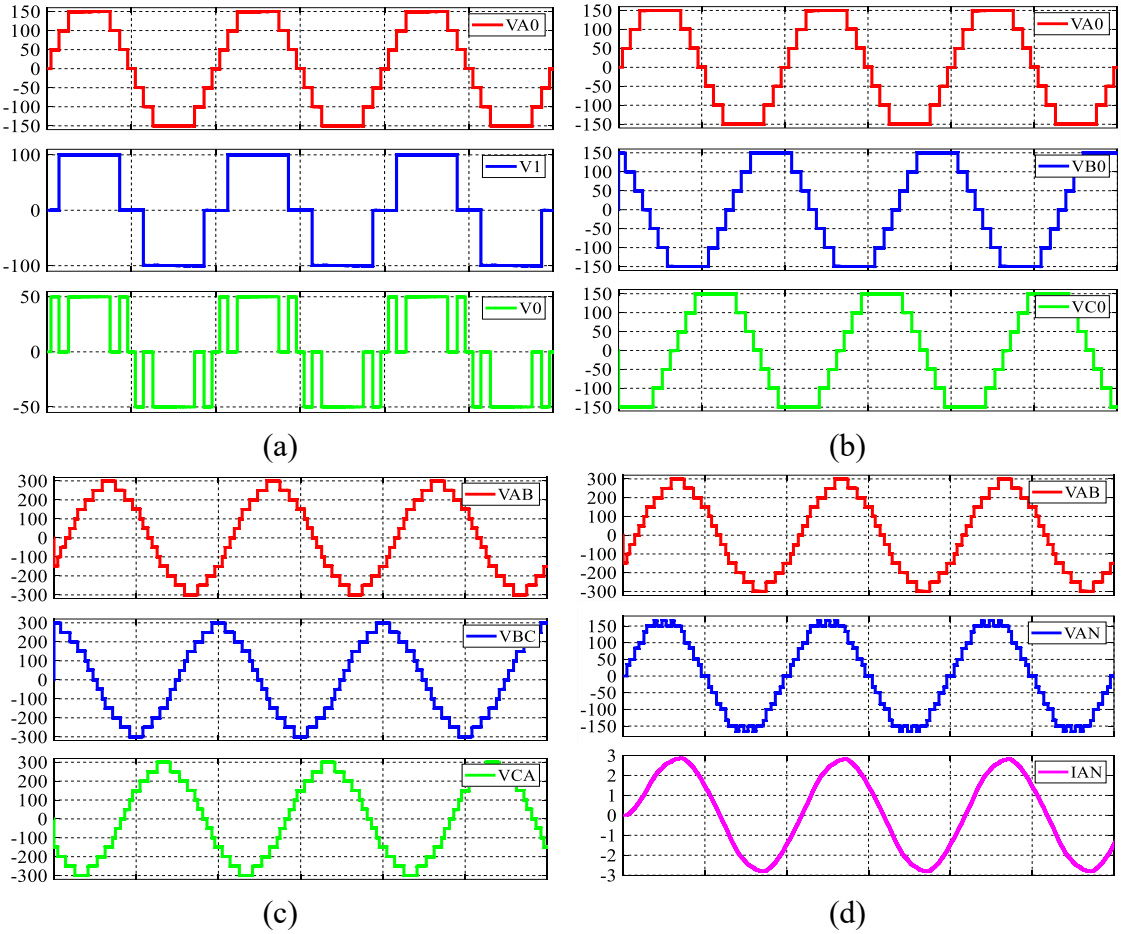
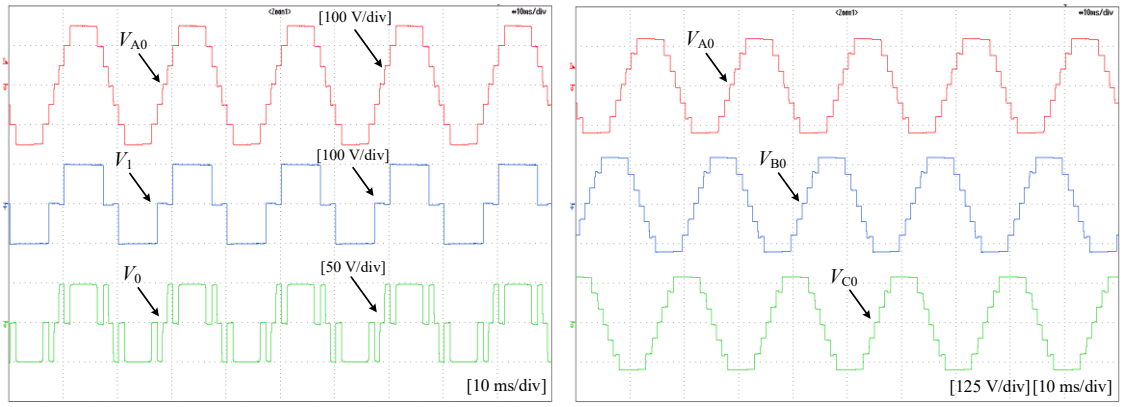


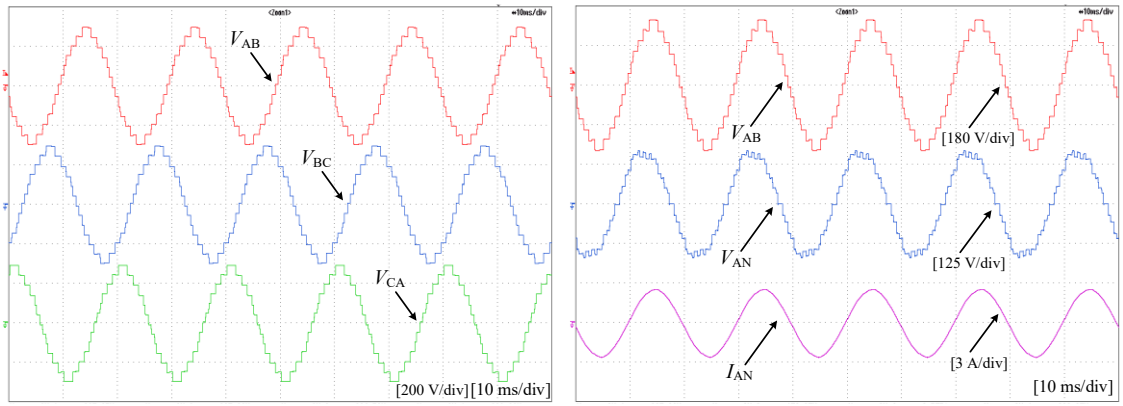
Figure 4.24: Simulation waveforms of T_D at β of 1. (a) Pole voltage V_{A0} synthesizing. (b) Pole voltages V_{A0}, V_{B0}, and V_{C0}. (c) Line voltages V_{AB}, V_{BC}, and V_{CA}. (d) V_{AB}, V_{AN}, and I_{AN} at R-L load.

The simulation findings are experimentally validated by the in-house inverter porotype in Figure 4.1. All system parameters are kept as same as in the simulation verifications. Figure 4.25 (a) presents the leg-A pole voltage V_{A0} and its two voltage components V_0 and V_1. By setting 100 V as the input voltage of the inverter E, the waveforms of V_0 and V_1 have voltages of (0 and ±50 V) and (0 and ±100 V), respectively, resulting in a seven-level pole voltage as shown in the first trace of Figure 4.25 (a). Figure 4.25 (b) shows the seven-level pole voltages of the three inverter legs V_{A0}, V_{B0}, and V_{C0}. These pole voltages having phase shifts of 120° produce three balanced line voltages of thirteen levels, as depicted in Figure 4.26 (a). Figure 4.26 (b) shows the obtained results when connecting an R-L load to the inverter outputs. The experimental results well validate and confirm the simulations and theoretical analysis of the proposed topology.



(a) (b)

Figure 4.25: Experimental waveforms of T_D at β of 1. (a) Pole voltage V_{A0} synthesizing. (b) Pole voltages V_{A0}, V_{B0}, and V_{C0}.



(a) (b)

Figure 4.26: Experimental waveforms of T_D at β of 1. (a) Line voltages V_{AB}, V_{BC}, and V_{CA}. (b) V_{AB}, V_{AN}, and I_{AN} at R-L load.

4.6 Comparison of the proposed topologies with recently developed MLIs

Comparative studies between the proposed topologies and other recently developed MLIs in terms of component count and voltage ratings are carried out and detailed in papers II to VI. This section summarizes those comparative studies and highlights the beneficial features of the proposed topologies and their limitations. The term "component" includes DC voltage sources, transformers, switches, power diodes, inductors, and capacitors.

4.6.1 Comparison assumptions and conditions

Some assumptions and conditions are used in the comparative studies to obtain a fair comparison among the different topologies as follows:

A) producing the same output voltages in terms of peak and step value. For example, the line voltage V_{AB} of all compared topologies with the proposed topology T_A must have seven levels of $E/3$ step and can reach a peak of $\pm E$ (i.e., E, $-2E/3$, $-E/3$, 0, $E/3$, $2E/3$, and E).

B) counting each part based on its primary unit structure. Therefore, a three-phase transformer is counted as three single-phase transformers, and a bidirectional switch is disassembled to its primary elements. For example, the proposed topology T_A has three bidirectional switches: each is configured by connecting two unidirectional switches in a common-emitter configuration, so they are counted as six switches.

C) freewheeling diodes are not included in the diode count N_D, and any coupled-inductor is counted as one inductor.

D) generating the same levels in the three pole voltages, so the state-of-art relationship between the number of levels in pole voltage N and line voltage $2N$-1 can be accomplished.

E) adopting the three-phase configuration of the compared topologies as some of them have single and three-phase configurations.

F) having equal current rating in all components, with some exceptions in the transformer-based MLIs because of winding turn ratio.

4.6.2 Comparative study for topology T_A

The SSC of the proposed topology T_A is compared with both the recently published four-level inverters [61-69] and the three conventional MLI topologies. A

summary of this comparative study is provided in this section, clarifying the salient features of T_A. The counterpart topologies are labelled by T_{A1} to T_{A10} and quantitively compared in terms of component counts. Table 4.5 summarizes the required components of the compared topologies, which are listed in descending order.

Table 4.5: Comparison of T_A with other four-level inverters [61-69] in terms of required components and voltage rating.

Topology	N_{DC}		N_{sw}			N_D		N_{Cap}		
	E/3	**E**	**E/3**	**2E/3**	**E**	**E/3**	**2E/3**	**DC-link**		**Flying**
								E/3	**E/2**	**E/3**
T_{A1} **[61], EI-MLI**	0	1	0	6	6	12	12	3	0	0
T_{A2}**, NPC-MLI**	0	1	18	0	0	18	0	3	0	0
T_{A3} **[62], 4L-NNPC MLI**	0	1	18	0	0	6	0	0	2	6
T_{A4} **[63], hybrid π-type MLI**	0	1	18	6	0	0	0	3	0	3
T_{A5}**, FC-MLI**	0	1	18	0	0	0	0	3	0	9
T_{A6} **[64], 4L-ANPC MLI**	0	1	24	0	0	0	0	3	0	0
T_{A7}**, half-HB MLI**	9	0	18	0	0	0	0	0	0	0
T_{A8} **[65-67], NT-type MLI**	0	1	12	6	0	0	0	0	0	6
T_{A9} **[68], DT-Type MLI**	0	1	12	0	6	0	0	3	0	0
T_{A10} **[69], π-type MLI**	0	1	6	6	6	0	0	3	0	0
Proposed topology T_A	0	1	9	6	3	0	0	3	0	0

According to Table 4.5, the topologies T_{A1} and T_{A2} require the highest component count while T_{A9}, T_{A10}, and the proposed topology have the lowest one. In terms of switch count, the topology T_{A1} has the lowest number of switches, but it needs twenty-four diodes, being the highest count among the compared topologies. However, topologies T_{A4}-T_{A10} and the proposed topology do not use clamping diodes. In terms of the capacitor count, T_{A5} requires nine flying capacitors, being the highest number among the addressed MLIs, while the proposed topology and topologies T_{A1}, T_{A2}, T_{A6}, T_{A7}, T_{A9}, and T_{A10} do not need flying capacitors.

It is noted that the topologies T_{A9} and T_{A10} have a similar component count like the proposed topology, and they do not require any clamping diodes or flying capacitors, making them the closest counterparts to the proposed inverter. Nevertheless, compared to T_{A9} and T_{A10}, the proposed topology has advantageous features: A) it has a 50% reduction in the high-voltage switches. Only three switches must withstand E while in the topologies T_{A9} and T_{A10}, six switches must block E; B) the proposed topology has a total standing voltage (TSV) lower than

the topology T_{A10}. It has a TSV of 10E while T_{A10} has TSV of 12E, reducing the total cost of the required switches; C) Although both the proposed topology and the topology T_{A9} have a TSV of 10E, the proposed topology has a lower switch count in the conduction paths than the topology T_{A9}. For each inverter leg, it reduces one switch, giving the proposed topology an extra advantage in reducing the conduction loss.

4.6.3 Comparative study for topology T_B

In this section, a comparison between the proposed topology T_B and the recently reported multilevel topologies in [4, 51, 92-101] is carried out to highlight its key features. The compared topologies are labelled by T_{B1} to T_{B11}, which are ordered in a descending manner in Table 4.6. Their merits and demerits were discussed in paper IV. In addition to the comparison conditions in Section 4.6.1, the DC-link structures in all single-source topologies are unified to be in the form of two symmetrical DC sources in series instead of one DC source divided into two parts by two capacitors. Therefore, the DC-link capacitors for single-source MLIs are replaced by DC sources. The rating of the DC sources in the DC-link of some topologies is changed to generate the same output line voltages, in terms of voltage step and peak voltage (condition A in Section 4.6.1). Each topology in Table 4.6 generates five-level line voltages with E step and peak of 2E.

Table 4.6: Comparison of T_B with the reported MLIs in [4, 51, 92-101] for three-level operation.

Topology	N_{DC}		N_{SW}				N_D		N_L	N_{Cap}
	E	**2E**	**0.5E**	**E**	**1.5E**	**2E**	**E**	**2E**	**2E**	**E**
T_{B1} **[93]**	0	3	0	3	0	6	12	0	0	6
T_{B2} **[92]**	1	1	4	1	3	6	12	0	0	0
T_{B3} **[4]**	3	0	0	18	0	0	3	0	0	0
T_{B4} **[98]**	1	1	0	6	0	3	3	6	3	0
T_{B5} **[4]**	3	0	0	18	0	0	0	0	0	0
T_{B6} **[4]**	3	0	0	15	0	0	3	0	0	0
T_{B7} **[51]**	2	0	0	18	0	0	0	0	0	0
T_{B8} **[95]**	4	0	0	12	0	0	0	0	0	0
T_{B9} **[101]**	2	0	0	9	0	3	0	0	0	0
T_{B10} **[97]**	1	1	0	6	0	6	0	0	0	0
*T_{B11} **[102]**	2	0	0	6	0	6	0	0	0	0
Proposed topology T_B	2	0	0	9	0	3	0	0	0	0

*T-type, as the proposed topology is topologically based on it.

Table 4.6 shows that the topologies T_{B9}-T_{B11} are considered the closest counterparts of the proposed topology in terms of component count. The proposed

topology has advantages of: A) lower TSV than T_{B10} and T_{B11}, due to 50% reduction of high-voltage switches (three instead of six). The TSV of the proposed topology is 15E, while it is 18E for T_{B10} and T_{B11}. B) simpler DC-link requirements than topology T_{B10}, as it requires two symmetrical sources while T_{B10} employs two asymmetrical sources. The proposed topology and T_{B9} have equal TSV of 15E for the three-level operation, but the proposed topology is more advantageous for level counts of more than three as detailed in paper IV.

4.6.4 Comparative study for topology T_C

A comparison between the proposed topology T_C and the existing five-level transformer-based topologies T_{C1}-T_{C7} is summarized in Table 4.7 to highlight its main merits. For comparison purposes, the symmetrical operation mode of compared topologies is adopted. Further, the DC-link of some topologies is reconstructed as a single source divided into two parts by two capacitors, making all DC-link structures identical. For example, T_{C4} has two DC sources of 0.5E, so they are replaced by one DC source of E and two capacitors. Due to the boosting feature of the transformer-based topologies, the peak value of the line voltage cannot be the same in all topologies as suggested by condition A in Section 4.6.1. Alternatively, the input voltage for all topologies in Table 4.7 is selected to be E volt, making them identical in their input voltage regardless of the peak value of the output voltage.

Table 4.7 shows that the highest switch count, diode count, and transformer count are in (T_{C1}, T_{C2}, T_{C4}, and T_{C6}), T_{C1}, and (T_{C2} and T_{C7}), respectively. Further, it is noted that the topologies T_{C1} and T_{C2} require the highest number of components, while the proposed topology has the least component count. Among the reported counterparts in Table 4.7, the topologies T_{C3}-T_{C7} requires the same counts of DC sources and capacitors as the proposed topology. However, the proposed topology has some advantageous merits as compared to the existing counterparts as follows: A) eliminating the six power diodes in T_{C3} and T_{C5}, B) employing six switches lower than T_{C4} and T_{C6}, C) reducing the transformer count to three instead of six in T_{C7}. On the other hand, twelve switches with rating of E are required in T_{C4}, T_{C6}, and the proposed topology, while only six switches at the same rating are required in T_{C3}, T_{C5}, and T_{C7}.

Table 4.7: Comparison of T_C with transformer-based MLIs in [78, 79, 86, 103, 104] for five-level operation.

Topology	N_{DC}	$N_{Cap,\ DC\text{-}link}$	N_{SW}		N_D	N_{Trf}	
	E	E/2	E/2	E	E/2	*E	*E/2
T_{C1} (Config.1) [86]	1	2	24	0	12	3	0
T_{C2} [79]	1	0	0	24	0	6	0
T_{C3} (Config.2)[86]	1	2	12	6	6	3	0
T_{C4} [78]	1	2	12	12	0	3	0
T_{C5} (Config.3)[86]	1	2	12	6	6	3	0
T_{C6} [103]	1	2	12	12	0	3	0
T_{C7} [104]	1	2	12	6	0	0	6
Proposed topology T_C	1	2	6	12	0	3	0

*The applied voltage across the primary windings, the load current is assumed to be the same for all topologies.

4.6.5 Comparative study for topology T_D

The proposed topology T_D is compared to recently developed transformer-based MLIs at nine-level operation in this section. The topology T_D aims to maximize the output voltage level count while reducing the required components. Therefore, a quantitative comparison is carried out between the counterparts and the proposed topology. Table 4.8 lists the considered MLI topologies in the comparative study T_{D1}-T_{D4} and their component counts. Further, it shows the voltage stress/rating of the necessary parts in each topology. Due to the difficulty of producing output voltages with the same peak in the transformer-based MLIs, as explained in Section 4.6.4, the total input voltage of all compared topologies is unified to be E volt. For example, the topology T_{D1} has a single DC-link, comprising four DC sources in series, so each one is selected to produce E/4, making the total input voltage equal to E.

Table 4.8: Comparison of T_D with transformer-based MLIs in [78-81] for nine-level operation.

Topology	N_{DC}			N_{Cap}				N_{SW}				N_D	N_{Trf}	
				DC-link	Flying									
	E/4	E/2	E	E/2	E/4	E/2	E	E/4	E/2	E	2E	E	*E	*2E
T_{D1} [78], CMLI	4	0	0	0	0	0	0	24	0	12	0	0	3	0
T_{D2} [80], H9LI	0	0	1	0	0	3	6	0	12	6	6	6	0	3
T_{D3} [81], MANPC	0	0	1	2	3	0	0	12	12	6	0	0	3	0
T_{D4} [79], TB-CHB	0	0	1	0	0	0	0	0	0	24	0	0	6	0
Proposed topology T_D	0	2	0	0	0	0	0	0	6	18	0	0	3	0

*The applied voltage across the primary windings, the load current is assumed to be the same for all topologies.

It is noted from Table 4.8 that the proposed topology, T_{D1}, and T_{D4} do not require any capacitor or power diodes, increasing their reliability and conversion efficiency. Contrarily, the topologies T_{D2} and T_{D3} are capacitor-based circuits, increasing the control complexity, sensor count, and failure rates. The proposed inverter and topologies T_{D1}-T_{D3} use the same transformer count. However, the proposed inverter has some salient advantages: lowering twelve switches and two DC sources as compared to T_{D1}, eliminating six power diodes and nine capacitors as compared to T_{D2}, reducing six switches and five capacitors as compared to T_{D3}. Both T_{D4} and the proposed topology are capacitor- and diode-free circuits, but T_{D4} requires one DC source while the proposed topology uses two DC sources. However, the proposed topology can save three transformers as compared to the topology T_{D4}. It is worth mentioning that the two DC sources in the proposed topology have a voltage rating of $0.5E$, while the DC source in the topologies T_{D2}-T_{D4} has a voltage rating of E. Table 4.8 confirms that the proposed topology employs the lowest component count among the compared transformer-based MLI topologies.

4.6.6 Applying the *CEL* factor on the compared topologies

The provided data in Tables 4.5-4.8 are used as inputs to (2.3)-(2.10) for calculating the *CEL* factor of the proposed topologies and counterparts. Figure 4.27 shows the graphical summary of the obtained values. As detailed in Section 2.1, the *CEL* produces numbers related to the rating of the components used in a topology. Low values of *CEL* in a topology mean that the majority of its components have low ratings.

Figure 4.27 (a) shows that T_A can be a promising solution in terms of low component count and good *CEL* value. For example, none of the reported topologies has a lower component count than T_A, but T_{A7} has a better *CEL* value with the cost of a higher component count. The comparison of T_B and its counterparts is shown in Figure 4.27 (b), indicating that the proposed topology T_B is the second-best topology after T_{B8} in terms of *CEL* value, while it employs a lower component count. It can be observed in Figures 4.27 (a) and (b) that T_{A9} and T_{B10} have similar numbers as the proposed topologies T_A and T_B, respectively. The merits of T_A and T_B against them were discussed in Section 4.6.2 and 4.6.3, respectively. Comparisons of the proposed transformer-based topologies T_C and T_D with counterparts are shown in Figures 4.27 (c) and (d), respectively. Figure 4.27 (c) confirms that none of the reported topologies in Table 4.7 has a lower

component count or *CEL* than the proposed topology T_C. The proposed topology T_D has the third-best value of *CEL* with the advantage of the lowest component count, as depicted in Figure 4.27 (d). Although topologies T_{D1} and T_{D3} have better *CEL* values than T_D, they employ a higher component count as detailed in Table 4.8. The above discussion of the proposed topologies against counterparts proves that they can decrease the component count without extensively increasing their ratings.

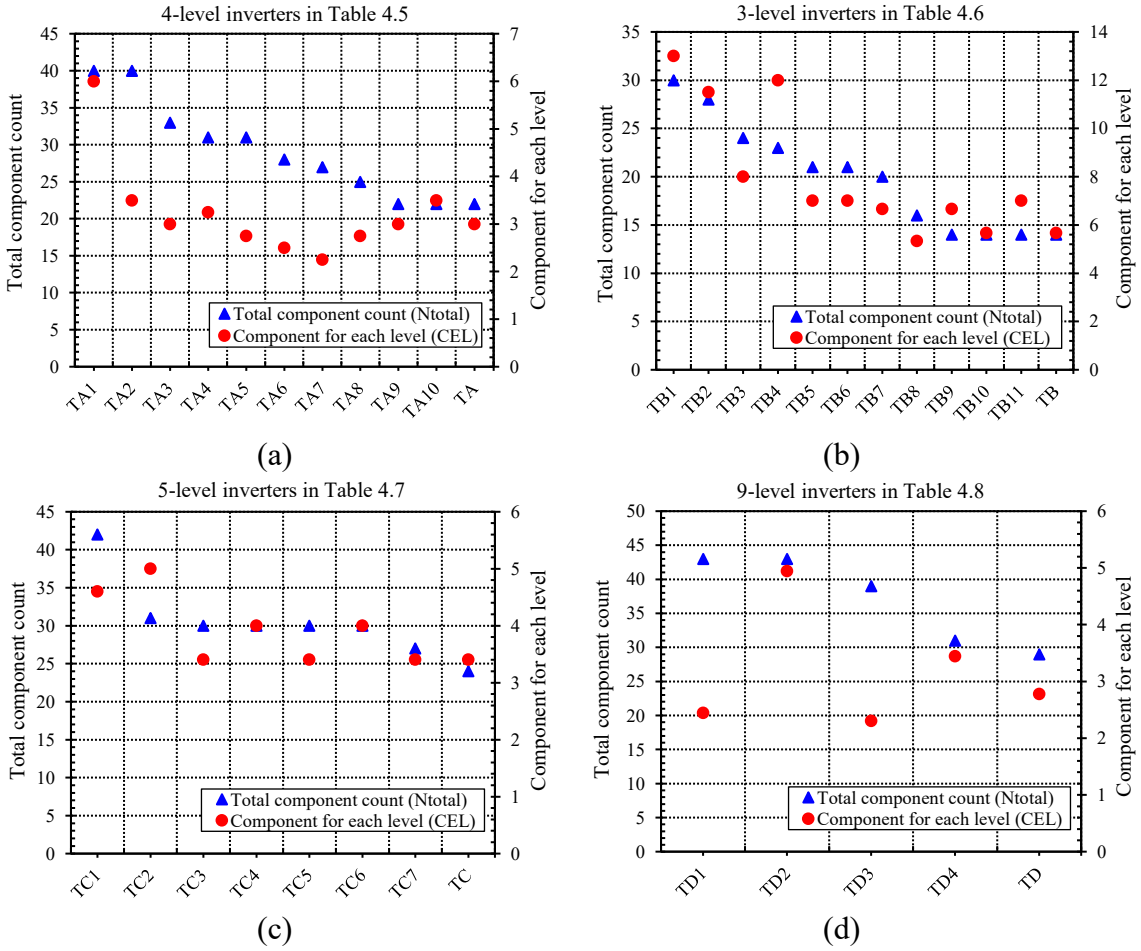


Figure 4.27: Comparison of the proposed topologies with counterparts in terms of total component count and *CEL* factor. (a) T_A with 4-level inverters in Table 4.5. (b) T_B with 3-level inverters in Table 4.6. (c) T_C with 5-level inverters in Table 4.7. (d) T_D with 9-level inverters in Table 4.8.

Chapter 5

Concluding remarks

5.1 Conclusions

This research focuses on proposing novel MLIs with a reduced component count. The existing MLI topologies suffer from two main drawbacks: A) high component count and B) high portion of semiconductor devices rated at the full input voltage. Accordingly, reducing component count and voltage stresses is of great importance to further improve the existing MLIs. Within the framework, four novel three-phase MLIs were proposed in this dissertation with reduced components and/or voltage stresses. They were theoretically demonstrated, numerically verified, and experimentally validated through the in-house setup. The proposed topologies can serve as reduced-component alternatives in different voltage levels with transformer and transformerless operations.

Only a few studies in literature have dealt with comparative methods to evaluate new topologies efficiently. The existing comparative factors *LSR* and *CLF* cannot consider component ratings, as detailed in Section 2.1. In this framework, paper I proposes novel comparative factors, so-called "component for each level (CEL)" and "stored energy factor (SEF)", to address the existing comparative factors drawbacks. Further, paper I presents a comprehensive review study of the most promising MLIs in terms of construction, salient features, and limitations, updating the research baselines with the newest reflections.

The three-level T-type inverter is a popular topology in low- and medium-voltage applications. However, 50% of its switches are rated at the full voltage of the DC-link, negatively impacting cost and loss. The low-voltage configuration of the proposed topology T_B can reduce this percentage to only 25% while keeping the same number of levels and component counts. Accordingly, T_B can be considered as a promising alternative in the T-type-based MLI topologies. The

topology T_B is applicable for both low-voltage and high-voltage applications as it can be extended to produce higher voltages without increasing the voltage stress.

Four-level topologies were introduced to improve the power quality of three-level inverters as detailed in Section 2.2.1, but the active and passive components are increased. The NT-type, DT-type, and π-type inverters are considered as attractive solutions with a reduced switch count to overcome the mentioned drawbacks, as explained earlier. However, six flying capacitors are required in NT-type, and one-third of switches in DT-type and π-type inverters are rated to the full input voltage. To address these issues, a novel four-level topology was proposed in paper II. It eliminates the flying capacitors in NT-type and reduces the switches rated at the input voltage in DT-type and π-type by 50%.

To increase voltage boosting and/or galvanic isolation, transformers are used in MLIs as detailed in Section 2.2.3, increasing their size and cost. Two topologies, T_C and T_D, are proposed to reduce transformers count and other components. The topologies T_{C5}-T_{C7} addressed in Section 4.6.4 are considered as the counterparts of the proposed topology T_C. However, T_C eliminates six diodes, six switches, and three transformers from T_{C5}, T_{C6}, and T_{C7}, respectively. On the other hand, the discussed topologies T_{D2}-T_{D4} in Section 4.6.5 are the counterparts of the proposed topology T_D. Despite reducing the components count compared to conventional transformer-based MLI, T_{D2}-T_{D4} still employ high counts of capacitors, switches, diodes, and transformers that can be further reduced. The proposed topology T_D can remove nine capacitors and six diodes from T_{D2}, five capacitors and six switches from T_{D3}, and three transformers from T_{D4} with one DC source more than T_{D2}-T_{D4}. Due to their modularity, T_C and T_D can be extended to produce higher levels without increasing the voltage stress.

5.2 Limitations and future works

Paper I has proposed new comparative factors, overcoming the existing factors drawbacks as detailed in Section 2.1. However, the proposed factors are not able to reflect the component count of a topology because of giving more priority to component rating than component count. Thus, the suggested factors should be used together with the total component count to provide a more comprehensive comparison. Further, the calculations of the proposed factors do not involve any cost function, making all components equally important. Therefore, using cost functions to identify which component has a higher effect than others is an interesting topic for a further work to improve these comparative factors.

The efficiency analyses of the proposed topologies T_A and T_B were made by considering narrow switching frequency and output power ranges. They might be considered as initial studies and not full investigations, justifying the obtained high efficiencies. Consequently, a comprehensive efficiency analysis is an attractive point to evaluate the efficiency of the proposed topologies against counterparts.

The proposed transformer-based topologies T_C and T_D are not advised for applications, where a wide range of frequencies is required to avoid transformer saturation. This is a common limitation in MLIs that employ low-frequency transformers. Therefore, in those applications, the transformers need to be designed to operate in wider frequency ranges. Another interesting topic in topologies T_C and T_D would be developing novel transformer solutions to reduce the magnetic element size. The possibilities of replacing the transformers with coupled inductors or three-phase transformers can be investigated. For example, the influence of using one three-phase transformer instead of three single-phase transformers on the total size might be a useful study.

The proposed topologies are controlled by LFM and LSPWM switching schemes, but other modulation techniques can improve their performance. For example, selective harmonic elimination (SHE) scheme can further reduce the harmonic contents in the output voltages. Consequently, a further work could explore the influences of different modulation strategies on the performance of the proposed topologies, allowing for selecting the best modulation for each topology.

Topologies T_B-T_D were not experimentally validated for higher voltage level count. They were experimentally validated for their low-level configurations alone. For example, T_D was experimentally validated when producing seven-level voltages, while its nine-level and N-level operation were numerically and theoretically demonstrated, respectively. This can be justified by the limited time and in-house facilities of the PhD project. It is important to experimentally validate their operation for producing higher level count to have a better justification of its performance.

T_D is more suitable for applications, where the component count and inverter footprint are more important than the isolation feature, as it does not provide isolation between source and load. Therefore, a further improvement of this topology would be useful to broaden its applicability in various applications.

During the design phase of the proposed topologies, capacitors were assumed to have higher effects on control complexity than switches because of their necessity for voltage balance algorithms and sensors. It would be interesting to study the

effects of each component on inverter size, cost, complexity, efficiency, and reliability, allowing researchers to know which component is more worthy than others. A comprehensive study that links each design aspect with component type would be of great importance to propose more worthy topologies.

This dissertation focuses on topological improvements of MLIs, but some other important topics related to reliability enhancement and lifetime extension can be worthy for future studies, for example, new strategies for fault prognosis and diagnosis in MLIs, thermal stress reduction of switches, and ageing mitigation control.

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Appendices

Paper I:

Voltage Source Multilevel Inverters with Reduced Device Count: Topological Review and Novel Comparative Factors

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Voltage Source Multilevel Inverters with Reduced Device Count: Topological Review and Novel Comparative Factors

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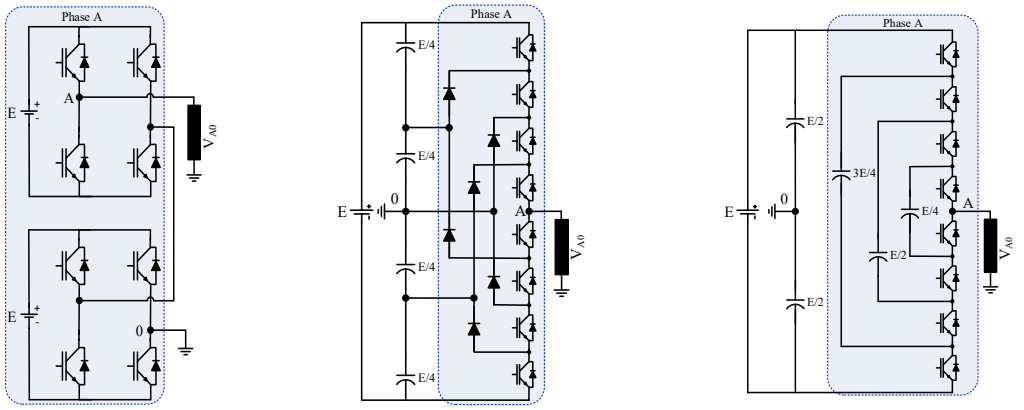
***Abstract*—Multilevel inverters have gained increasing interest for advanced energy-conversion systems due to their features of high-quality produced waveforms, modularity, transformerless operation, voltage and current scalability, and fault-tolerant operation. However, these merits usually come with the cost of a high number of components. Over the past few years, proposing new multilevel inverters with a lower component count has been one of the most active topics in power electronics. The first aim of this work is to update and summarize the recently developed multilevel topologies with a reduced component count, based on their advantages, disadvantages, construction, and specific applications. Within the framework, both single-phase and three-phase topologies with symmetrical and asymmetrical operations are taken into consideration via a detailed comparison in terms of the used component count and type. The second objective is to propose a comparative method with novel factors to take component ratings into account. The effectiveness of the proposed method is verified by a comparative study.**

Index Terms—Multilevel inverter (MLI), symmetric operation, asymmetric operation, comparison factor, component for each level (CEL), single-phase, three-phase, DC-AC converter.

I. INTRODUCTION

Multilevel inverters (MLIs) have been developed for more than five decades and gained increasing importance in industrial applications as one of the most attractive solutions for implementing medium-/high-voltage high-power converters [1-13]. The MLIs are configured by a distinct arrangement of single/several DC sources, namely batteries, rectifiers, flying capacitors, fuel cells, PV panels, and semiconductor devices, e.g. insulated-gate bipolar transistor (IGBT), metal–oxide–semiconductor field-effect transistor (MOSFET), and diodes, in a way to produce a near sinusoid voltage with low distortion. Combining low-voltage DC sources with semiconductors switches can efficiently generate high-voltage stepped waveforms at the output of converters. The rating of the switches is defined by the rating of linked DC sources, so the voltage stress on the switches is much lower than the output voltage. From the 1970s, Baker and Bannister in [14] have invented the first converter topology, which is widely

known as cascaded H-bridge (CHB) MLI, using several DC sources. Each source was linked to a single-phase inverter to form one cell. By connecting more cells in cascade as shown in Fig. 1 (a), a multilevel output can be achieved. A few years later, in the 1980s, a single source multilevel topology called diode clamped or neutral point clamped (NPC) MLI has been proposed by Baker in [15]. Despite using one DC source, it requires several diodes that are connected to a neutral point, as shown in Fig. 1(b). In 1981, Nabae et al. in [16] have presented the NPC implementation by using the pulse-width modulation (PWM) scheme. Fig. 1 (c) shows a flying capacitor (FC) or capacitor-clamped MLI, being introduced during the 1990s in [17] and [18] by Meynard et al. and Lavieville et al., respectively. Although it needs only one DC source, several flying capacitors result in increasing both size and control complexity of the FC-MLI. These three topologies have considered as the basic MLI topologies in literature [1-4]. The DC-to-AC conversions using MLIs are widely used in power systems, transportation, and renewable energy systems, for example, in flexible AC transmission systems (FACTS) [19, 20], high-voltage direct-current (HVDC) [21, 22], active power filters (APFs) [23, 24], variable frequency drives (VFD) [25-27], pumped storage power plants (PSPP) [28-30] and grid-connected or standalone PV systems [31-33].



(a) (b) (c)

Fig. 1 One leg of the basic MLI topologies for five-level configurations. (a) CHB MLI. (b) NPC MLI. (c) FC MLI.

The MLI based DC to AC converters have several attractive merits as reported in [1-13]: A) producing high-quality waveforms with low harmonic contents and low dv/dt stress, significantly reducing the total harmonic distortion (THD), filter dimensions, and electromagnetic interference (EMI). B) operating in both fundamental and low frequency switching schemes can lower switching losses, being beneficial for efficiency and cooling requirement, especially in high-power applications. C) using low-rated standard semiconductor devices for producing high voltage without connecting them in a series manner as in two-level medium-power inverters. D) having small/zero common-mode voltage (CMV) can eliminate drawbacks of CMV in many applications, for example, the stress in the bearing of a driven motor fed by MLIs can be reduced in drive systems. Moreover, several MLIs have further strategic merits, namely transformerless operation,

modularity, voltage and current scalability, high redundancy in switching states, and fault- tolerant operation. On the other hand, these merits come with the cost of a high number of passive and active components, such as DC sources, flying capacitors, inductors, diodes, and switches. Consequently, the volume, cost, and complexity of the inverter are increased [1-13]. Thus, proposing new MLIs, that can enlarge the level number along with a low component count is currently one of the key research trends in this research theme [3, 11]. Within the theme, improving efficiency, power density, control simplicity, reliability, cost, and broadening MLIs applications have attracted a large number of publications every year. Accordingly, reviewing the most advanced knowledge in this research field periodically is always of importance to update the research baselines or the newest reflections, resulting in many review studies presented in [1-13]. Most of those studies give a detailed review of MLIs based on a specific application or inverter family, e.g. transportation [8], medium-voltage drives system [13], modular MLIs [5-9], HVDC applications [10], and renewable energy integration [3]. Moreover, the existing reviews have used two conventional factors, namely the level-number per switch ratio (LSR) or component per level factor (CLF), to assess the component counts among topologies [34, 35], which are not able to take component ratings or cost and stresses of component into consideration.

To address the problem of existing comparative factors, this work proposes a novel comparative factor, so-called "component for each level (CEL)", in addition to a review of the most promising MLI topologies. Unlike the existing reviews focusing on a specific application, this work reviews diverse MLI topologies in a wide range of applications. Further, a comparative study is presented to verify that the proposed factor allows comparing the component count among MLIs more efficiently.

The rest of this paper is organised as follows: recently proposed voltage source multilevel inverters will be classified and reviewed in Section II in detail, while both existing and the proposed methods for comparing MLIs will be discussed in Section III. Finally, conclusions are drawn in Section IV.

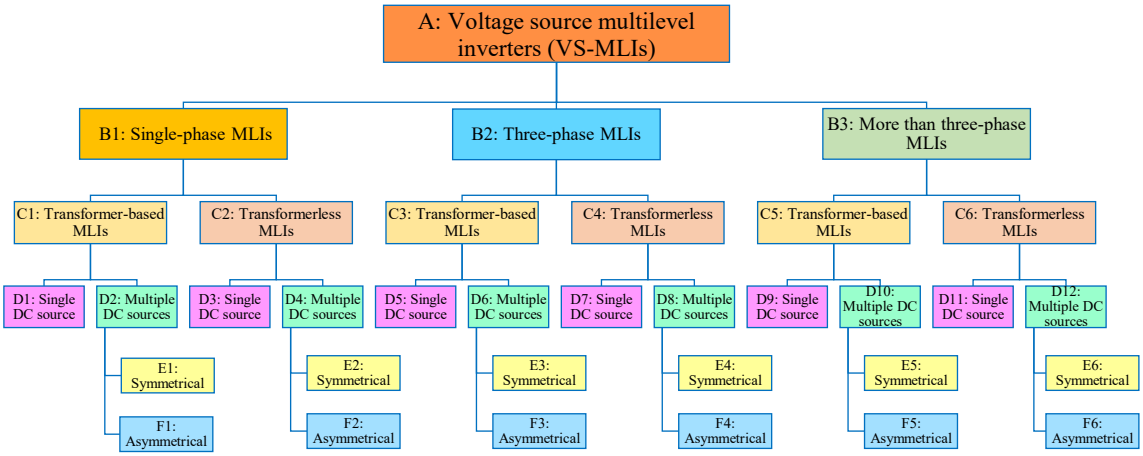
II. CLASSIFICATION OF MULTILEVEL INVERTERS

The recently developed MLI topologies are subdivided into three main groups based on the number of phases, i.e. single-phase, three-phase, and over-three-phase configurations as shown in Fig. 2. The selected topologies are allocated in different subgroups, namely single DC source, multiple DC sources, symmetrical MLIs, asymmetrical MLIs, transformer-based, and transformerless MLIs. The first two main groups are the main focus of this paper, being detailed in the following sections.

A. SINGLE-PHASE MULTILEVEL INVERTERS

This section presents a detailed review of the recently developed single-phase MLI topologies (or groups C2 and C1 in Fig. 2) in terms of construction, features and limitations. The addressed topologies are applied in renewable energy, motor drives, and power systems with diverse designs and characteristics. This review focuses on the MLI with a boosting capability, coupled inductors-based MLI,

transformers-based MLI, specially designed topologies for particular applications and hybrid unipolar MLI topologies.



A: In [36-83, 85, 86, 92-97, 101-104, 107, 109-116, 141-165]	C1: In [43, 46-54]	C6: In [143, 155, 160-165]	D4: In [36-42, 44, 45, 55, 56, 58-83, 85, 86, 102, 141-143]	D8: In [39, 95, 101-103, 109-115, 142, 143, 149, 152, 154-156]	E2: In [37-40, 42, 60-63, 65-67, 71, 78, 80, 82, 86, 102, 142]	F1: In [48, 50, 51]	F6: In [143, 162, 165]
B1: In [36-83, 85, 86, 102, 141-143]	C2: In [36-42, 44, 45, 55-83, 85, 86, 102, 141-143]	D1: In [43-47, 49, 51, 53, 54]	D5: In [44, 45, 144-146, 159]	D11: In [155, 161, 164]	E3: In [51, 147, 148]	F2: In [58, 60-62, 64-66, 68, 69, 74, 76, 78-80, 82, 102, 143]	
B2: In [39, 44, 45, 92-97, 101-104, 107, 109-116, 141-159]	C3: In [44, 45, 144-149, 159]	D2: In [48, 50-52]	D6: In [147-149]	D12: In [143, 160-163, 165]	E4: In [39, 60, 78, 95, 101-103, 109, 110, 113, 115, 142, 154, 155]	F3: In [51, 149]	
B3: In [143, 155, 160-165]	C4: In [39, 92-97, 101-104, 107, 109-116, 141-143, 149-158]	D3: In [36, 39, 41, 42, 44, 45, 55-57, 59, 66, 70, 72, 73, 75, 77, 81, 83, 85, 86, 141]	D7: In [92-94, 96, 97, 104, 107, 116, 141, 150-153, 157, 158]	E1: In [51, 52]	E6: In [160, 161, 163]	F4: In [60, 78, 102, 109-112, 114, 143, 149, 156]	

Fig. 2 Classification of multilevel voltage source inverters.

A novel single-phase MLI with the boosting capability is proposed in [36] as shown in Fig. 3, consisting of three stages, conventional boost converter, switch-diode-capacitor cell, and full H-bridge inverter. These three stages function as a step-up, level generator, and inversion stages, respectively. It can produce five voltage levels by using a single DC source, three power diodes, two capacitors, six switches, and an input inductor. Unlike other five-level inverters, the topology's main features include boosting capability, using a single DC source and low switch count. However, bulky size, high losses and limited lifetime are still a problem since it requires capacitors, inductor and a significant number of diodes. This circuit is suitable only for low-voltage applications because of high-voltage stress across the switches of the used H-bridge. To overcome these limitations, a quasi-cascaded H-bridge configuration was proposed in [37] as illustrated in Fig. 4 (a), consisting of two cascaded modules for generating five levels. Each module has one DC source, one inductor, one capacitor, two diodes, and four power switches. The problem of limited generated voltage was solved by using modules in a cascaded configuration. To improve the performance of the topology under unbalances of the DC sources, resulting in a voltage difference in the existing capacitors, and a DC offset at output, an additional capacitor C_d has to be used

between modules as shown in Fig. 4 (b). Although this capacitor has a low-voltage rating, it must carry the entire load current.

Other C2-group MLIs based on coupled inductors have been presented in [38-40]. In [38], a π-type MLI was proposed for single-phase applications. Additionally, the upgrading possibility for three-phase applications was discussed in [39]. The π-type MLI consists of two three-terminal switch network (SN) as illustrated in Fig. 5 (a), each SN is configured by using two switches and two diodes. The five-level circuit uses two DC sources, two capacitors, four diodes and two coupled inductors. The coupled inductors are connected in series, and the connection point produces the output node A, while the outer terminals B and C are connected to the middle points of SNs. One of the key advantages of the presented topology is using only four switches for producing five voltage levels $+E/2$, $+E/4$, 0, $-E/4$, and $-E/2$ without using any flying capacitor, resulting in control simplicity with a moderate size. However, lack of modularity and using coupled inductors limit the applicability of the proposed circuit. Belong to the same family, four nine-level coupled inductors-based topologies were proposed and analysed in [40]. Figs. 5 (b), (c), (d) and (e) show the suggested circuits, being formed by using two DC sources, switches, and pairs of coupled inductors. They have the common limitations of topologies in [38, 39], but do not use any diode or capacitor.

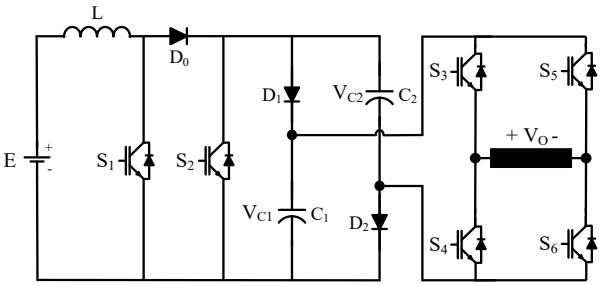
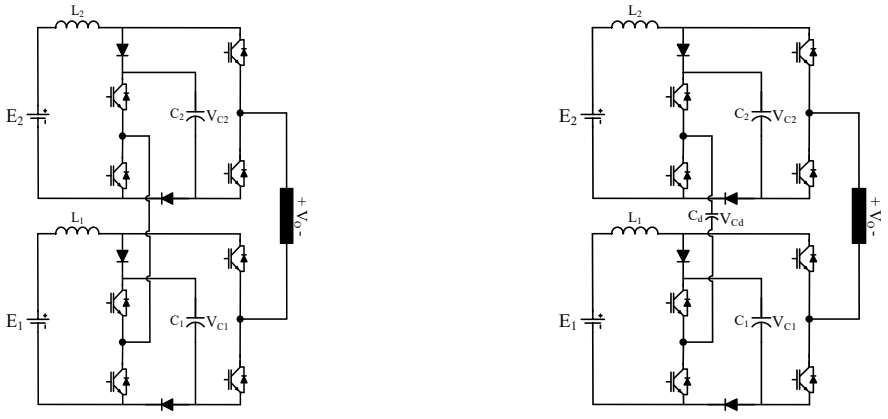


Fig. 3 Enhanced single-phase step-up five-level inverter [36]. Capacitor's voltage (V_{C1}, V_{C2}) = $E/(1 - D_{S1})$, where D_{S1} is the duty cycle of S_1.



(a) (b)

Fig. 4 Quasi cascaded H-bridge five-level boost inverter [37]. $V_{C1} = E_1/(1 - 2D_1)$, $V_{C2} = E_2/(1 - 2D_2)$, and $V_{Cd} = (D_1 - D_2)$ $V_{(C1 \text{ or } C2)}$, where D_1 and D_2 are the shoot-through duty cycles.

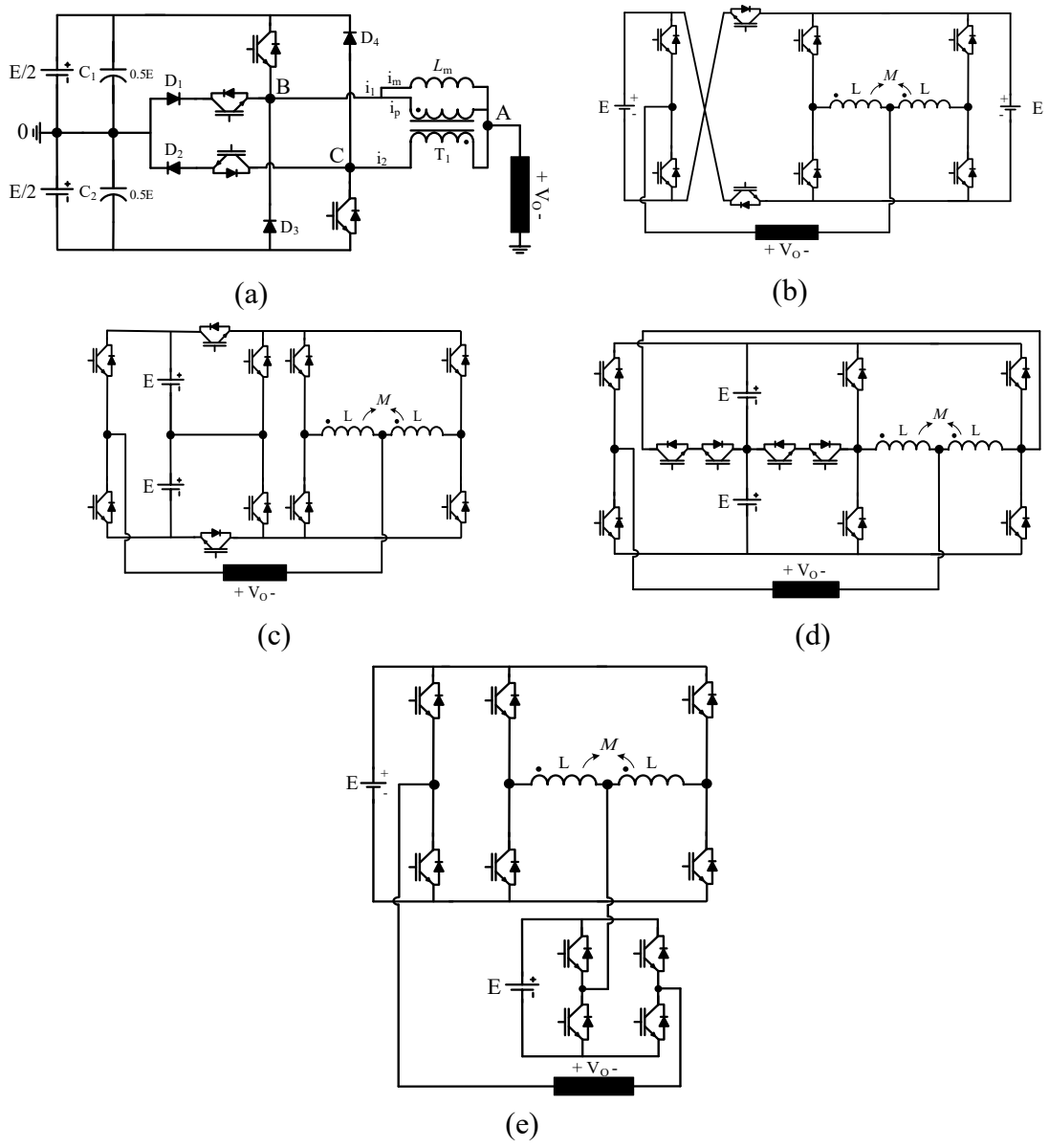


Fig. 5 Multilevel single-phase inverters with a pair of coupled inductors [38-40]. (a) Single-phase π-type five-level inverter [38, 39]. (b) Active series voltage sources with coupled inductors (AS-CI) [40]. (c) Active neutral point clamped with coupled inductors (ANPC-CI) [40]. (d) Extended ANPC-CIs (EANPC-CIs) [40]. (e) Cascaded with coupled inductors (C-CIs) MLI [40].

Two-hybrid MLI topologies were proposed in [41, 42], being formed by connecting three-level flying capacitor-fed-H-bridge (FCHB) cell with either three-level T-type cell in [41] or three-level active neutral-point-clamped (ANPC) cell in [42]. Connecting the FCHB cell with T-type or ANPC cells generates only five voltage levels of -*E*/2, -*E*/4, 0, *E*/4, and *E*/2, with a peak value equal to half of the DC-link voltage (i.e. 0.5*E*). Consequently, a two low-frequency switches (LFS) cell was recommended by the authors in [41, 42] to increase the peak value and level count of the output voltage. The peak value becomes *E* (i.e. the full DC-link voltage), and the level count is enlarged to nine levels instead of five (the additional four levels are: ±*E* and ±3*E*/4). Fig. 6 shows the nine-level configurations of the presented topologies in [41] and [42]. Fig. 6 (a) illustrates the presented topology

in [41], consisting of three capacitors, ten switches, and one DC source, while the introduced topology in [42] requires twelve switches, three capacitors and one DC source for producing nine voltage levels as depicted in Fig. 6 (b). The two topologies have the same count and rating of the capacitors (two of $E/2$ and one of $E/4$), the switches in the LFS (two of E), and FCHB (four of $E/4$) cells, but they require different switch counts and ratings of the utilised switches in ANPC and T-type cells. The presented topology in [42] needs two more switches as compared to the topology in [41]. Although the switches of ANPC and T-type cells have the same total standing voltage (TSV) of $3E$, they have different voltage ratings. All switches in the ANPC cell have the same voltage rating of $E/2$, while the switches in the T-type cell have different voltage ratings (two of E and two of $E/2$). From the industrial point of view, using switches of equal ratings is better than having different ratings, in terms of maintenance, manufacturing, and loss/temperature distribution, making the presented topology in [42] more advantageous than the presented topology in [41]. It is worth mentioning that the level count can be enlarged for both topologies by connecting additional FCHB cells. In [42], two methods were suggested (can be applied for the topology in [41] as well): either keeping a single DC source while repeating the FCHB cell or cascading the structure in Fig. 6 (a) (or Fig. 6 (b) for the topology in [42]) to construct a multiple DC source configuration. The two extension methods can be used as depicted in Fig. 6 (c) for gaining more benefits, depending on the availability of DC sources and the required output voltage. Using a single DC source and the possibility for generating a higher number of voltage levels by adding FCHB cells are the main features of these circuits, beside using a low component count. However, requiring a significant number of different rating capacitors for enlarging the voltage level count increases the inverter footprint and control complexity. Moreover, using the two-switch cell across the DC link makes these topologies more applicable in low-voltage applications alone.

Theoretically, the modularity feature enables producing an infinity number of voltage levels with high-voltage values by using low-rating semiconductors but requiring a higher number of components. In this direction, the cascaded transformer multilevel inverter (CTMLI) family (or C1 group in Fig. 2) has been proposed for eliminating the needs for numerous numbers of DC sources and floating capacitors while suffering the cost of required transformers [43-54]. Figs. 7 (a), and (b) show the conventional CTMLI, and a reduced component version was reported in [43]. The conventional topology uses four switches tied with a low-frequency transformer as a building cell, while the circuit in Fig. 7 (b) merges two cells to save almost half of switches count. Modularity, employing a single DC source, capacitor- and diode-free are the main merits while using bulky low-frequency transformers is the main demerit.

In [55-68], several topologies (belong to group D3 and D4 in Fig. 2) have been proposed for producing multilevel voltages as shown in Figs. 8, 9, and 10. All of them use two stages, one for generating unidirectional multilevel DC voltage and the other one for changing the polarity of the generated voltage from the first stage

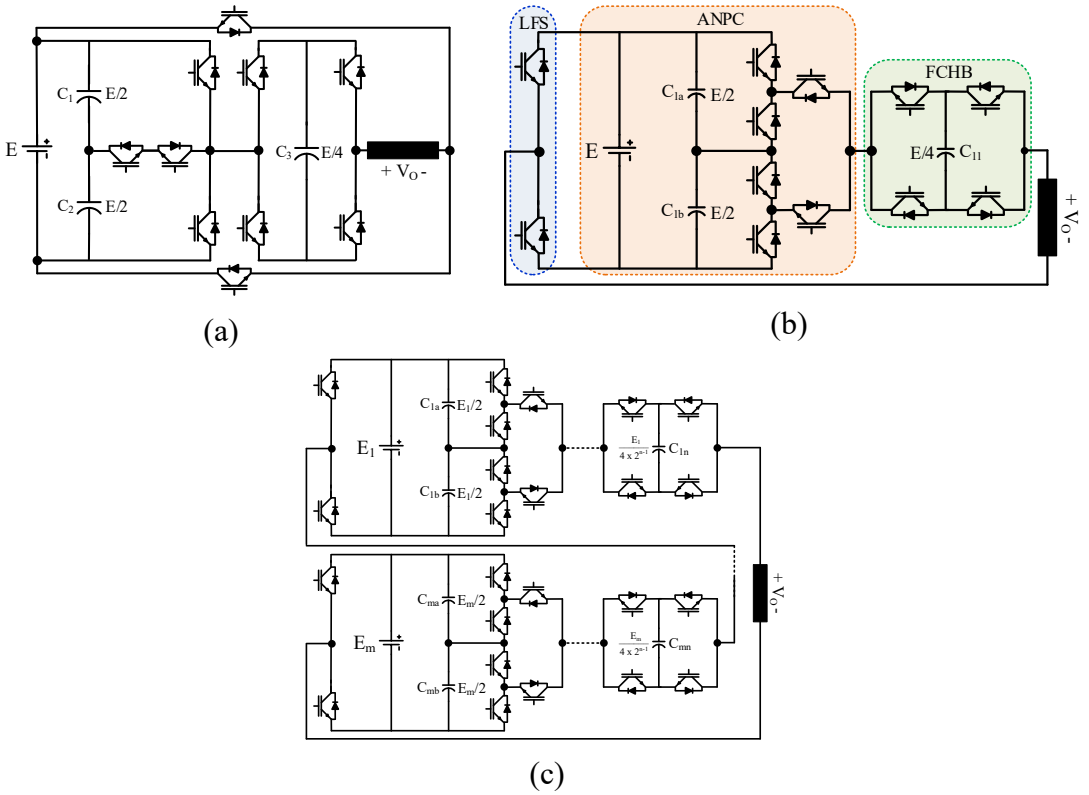


Fig. 6 Improved hybrid MLI topologies [41, 42]. (a) Nine-level inverter with reduced part count [41]. (b) Nine-level configuration of the double-hybrid ANPC inverter [42]. (c) *N*-level configuration for the double-hybrid ANPC inverter [42].

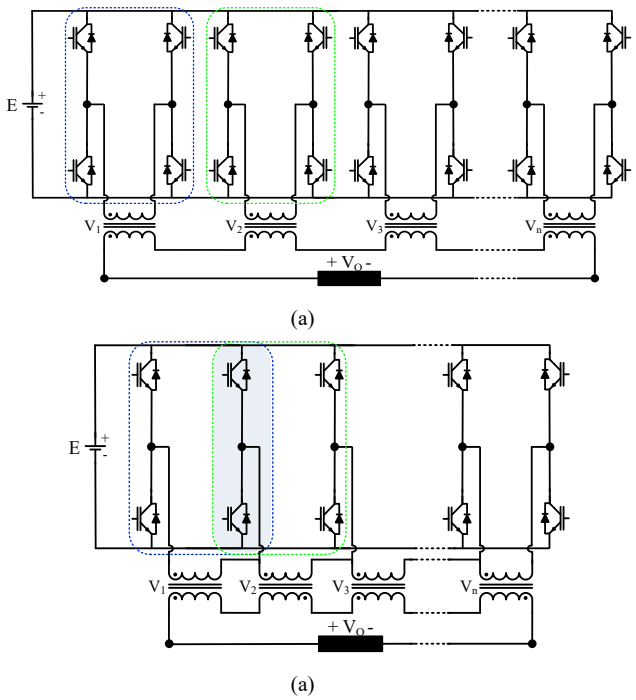


Fig. 7 Cascaded-transformer multilevel inverter (CTMLI) [43]. (a) The conventional CTMLI. (b) Low component merged cells CTMLI in [43].

to multilevel AC voltages. This common technique for obtaining AC voltage makes the mentioned circuits suffered from high-voltage stresses across the switches in the second stage, reducing the permissible operating voltage and limiting them to low-voltage applications. For example, the topology in [55] uses a new switched-capacitor (SC) as the first stage while a normal full H-bridge acts as a polarity changer stage for obtaining nine levels. Fig. 8 (a) shows this topology, having a reduced component count and the ability to avoid the voltage balance problem by the inherent self-voltage-balance feature. Therefore, the switching algorithms get simplified. Despite using one DC source, it requires two capacitors, two power diodes, and nine switches with different ratings for generating nine levels. By using a new quasi-resonant SC (QRSC) circuit instead of the existing SC in Fig. 8 (a), a new QRSC multilevel inverter has been developed in [56]. It allows producing N voltage levels by increasing the number of the capacitors, but it has high-voltage stress across the switches of the H-bridge, lowering the input DC source voltage. Further, the self-voltage balancing feature can be realised by fully connecting the capacitors in parallel or partially to the load or source. Because of this connection, current spikes appear, increasing the capacitance, and decreasing the inverter lifetime. To overcome this challenge, the quasi-resonant inductor in the QRSC circuit is used to suppress these spikes, reducing the capacitance and prolonging the expected lifetime. Fig. 8 (b) shows N-level version of QRSC topology, requiring one DC source, one inductor, X capacitors, X diodes, $2X+2$ switches, where $X = (N-1)/2$.

The proposed topology in [57] uses several unidirectional and bidirectional modules for building different substages, working as a level-generator stage. The H-bridge is to change the voltage polarity as demonstrated in Fig. 8 (c), in which a single source inverter uses nine capacitors and 42 switches for producing 49 levels. Although the proposed circuit does not use any inductor, it can boost the low input voltage to a high value. The output voltage is limited only by the voltage rating of the H-bridge four switches. For example, the voltage stress across theses four switches will be $24E$ for $N = 49$ levels, where E is the input voltage. Boosting feature is obtained by charging several capacitors stage by stage in a cascaded manner, i.e. the capacitors of the current substage can be charged by the capacitors of the previous substages. Using a single low DC voltage source for producing high voltage levels is the main merit of this topology, in addition to the diode-, inductor-free features. However, using many capacitors (nine for the 49-level version) with different capacitances and voltage values makes the control schemes complicated, decreasing the reliability and lifetime of the converter. An improved topology based on this circuit has been published in [58], having almost the same structure for the first two stages except replacing the two capacitors by two DC sources. For the last stage, it uses several full H-bridge cells instead of only one in [57], avoiding using the single-phase H-bridge to change the voltage polarity or high-voltage switches to obtain the negative voltage levels. Fig. 8 (d) shows the complete configuration, producing 55 voltage levels by using seven capacitors, 44 switches and three asymmetrical DC sources.

Fig. 8 (e) shows a new single-source seven-level topology investigated in [59], in which three-level DC-voltages are produced by using level-generator stages,

consisting of a single DC source, three capacitors, four switches, and four diodes, Moreover, a traditional H-bridge was used for producing the negative part, being more suitable for low-voltage applications alone. Using only one DC source is counted as an attractive advantage of this topology, but it has limitations regarding using diodes and capacitors as mentioned before. For example, to overcome the challenges for keeping the voltage of the capacitors in the DC-link balanced, the authors in [59] have recommended to use a resonant switched-capacitor unit (RSCU) as highlighted in Fig. 8 (e), increasing complexity, cost and the inverter size.

A new switched-capacitor MLI (SCMLI) was proposed in [60], which shares the same shortcomings like the topologies in [55-59] while using a new six-switch configuration for changing the polarity instead of using H-bridge. Further, multiple asymmetrical DC sources are used instead of using a single source, and voltage generator cells are required for generating multiple DC link voltages. Each one consists of two switches, one capacitor, one diode, and DC source. A 17-level version of the proposed MLI is shown in Fig. 9 (a), requiring ten switches, two capacitors, two diodes, and two isolated DC sources having asymmetrical values of E, and $3E$, respectively. To increase the output levels with a reduced component count, several topologies in the same family were proposed and summarized in Figs. 9 (b)- (h), being detailed in [61-67]. As seen from Figs. 9 (b)- (h), their key characteristics are realised as diode-, capacitor- inductor-free, boosting capability, using only a single DC source, a high number of capacitors, inductors and DC sources. However, they suffer from a common drawback, i.e. using polarity-changer stage, making the output voltage limited by the rated voltage of the switches.

A recently developed member of the unipolar MLIs family was proposed in [68]. Fig. 10 (a) shows the nine-level asymmetric structure of this topology, consisting of a unipolar level generator part followed by a conventional H-bridge cell to obtain bipolar multilevel voltages, similar to the topologies in [55-67]. Fig. 10 (a) shows the proposed topology, in which two trinary asymmetrical DC voltage sources (E_1:E_2 is 1:3) and ten switches are necessary for producing nine voltage levels of $4E$, $3E$, $2E$, E, 0, $-E$, $-2E$, $-3E$, and $-4E$. As suggested by the authors in [68], the voltage level count can be enlarged to 3^X levels by adding $(4K+2)$ switches and 'X' DC sources as depicted in Fig. 10 (b). The proposed topology has remarkable merits, namely reduced component counts, and being capacitor-, and inductor-free. However, the high total standing voltage of switches in both level generator and polarity changer parts is considered its main demerit. For example, the switches of the polarity changer H_1-H_4 must block the full dc-link voltage (i.e. $E_1+E_2+\ldots+E_X$), in addition to the different high-voltage stress across the remaining switches based on their location in the level generator part. The total standing voltage will be further increased when the level count or output voltage needs to be higher. The standing voltage is equal to $(((2(3^X-1)-3)+4(2(3^X-1)-3))E)$, where X is the number of DC sources. Accordingly, this topology is highly recommended for low-voltage applications, where high voltage levels are required at a low maximum output voltage.

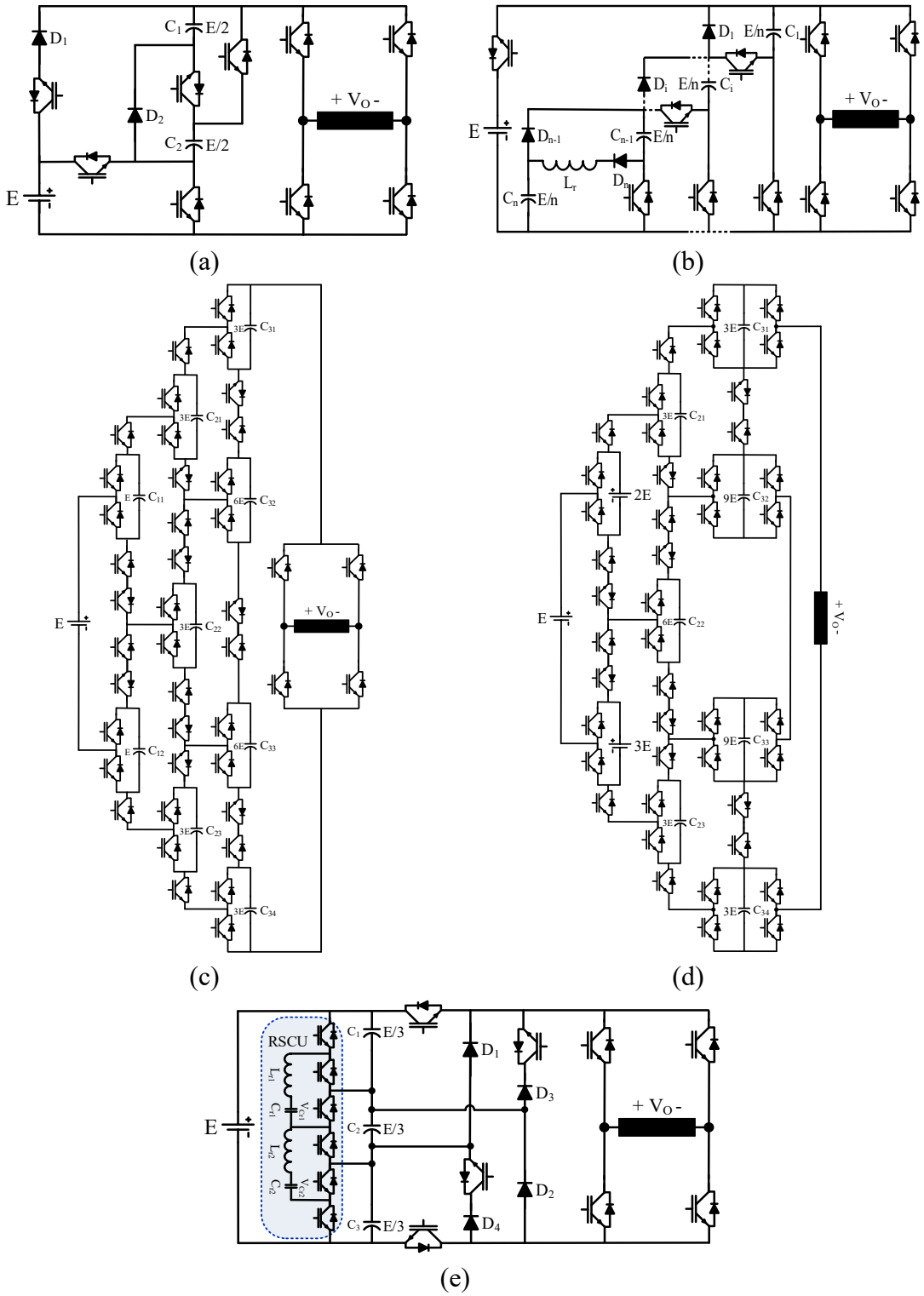


Fig. 8 Unipolar MLI topologies use polarity-changer stage for generating negative voltage levels [55-59]. (a) Nine-level inverter employing one DC source [55]. (b) Quasi-resonant switched-capacitor (QRSC) MLI [56]. (c) Step-up MLI with a single DC source [57]. (d) MLI structure based on a combination of SC and DC sources [58]. (e) Single source seven-level MLI topology [59].

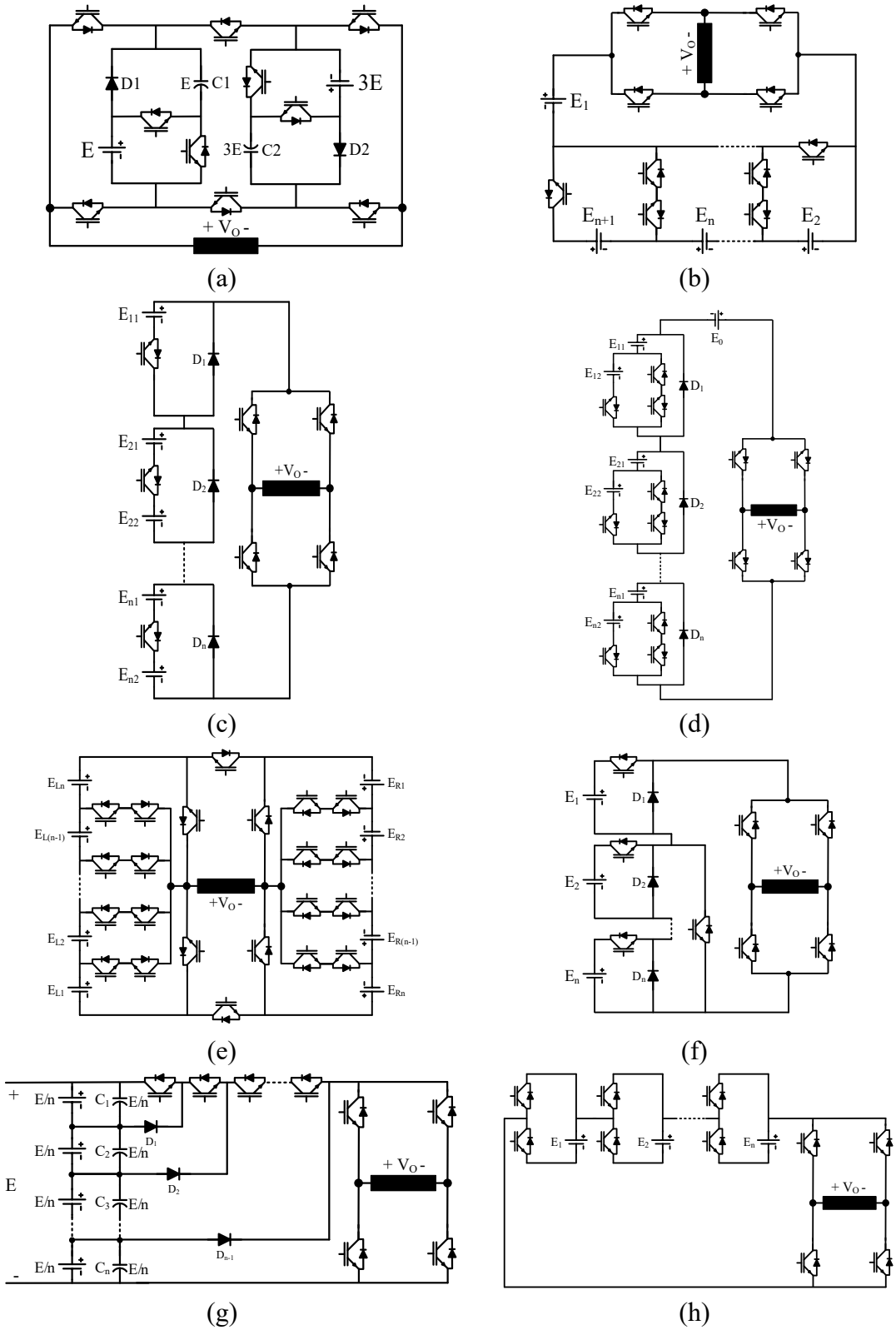
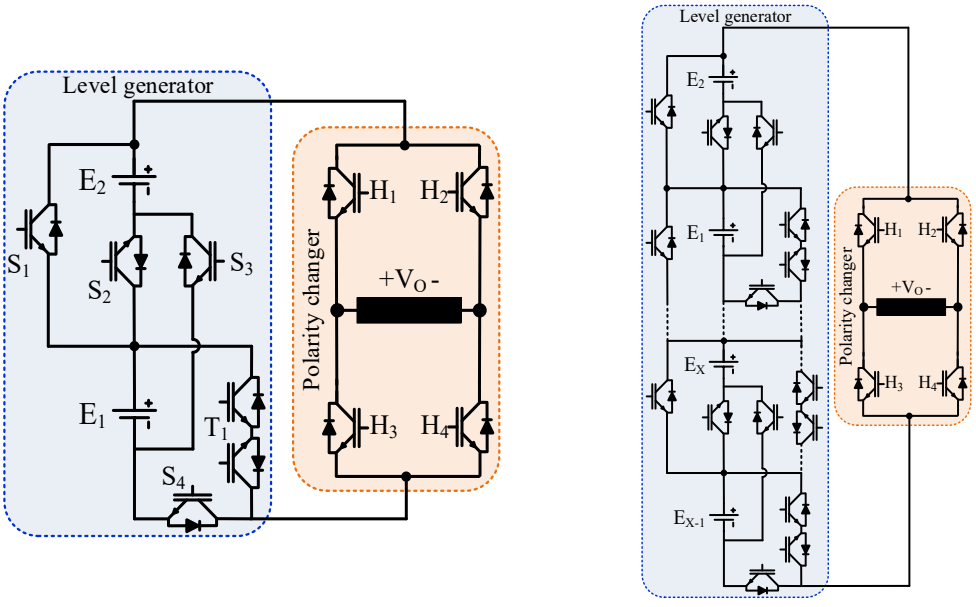


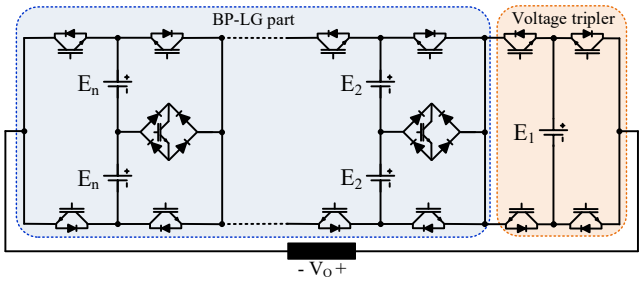
Fig. 9 Unipolar MLI topologies with the polarity-changer stage for generating negative voltage levels [60-67]. (a) 17-level structure for the single-phase SC-MLI [60]. (b) MLI for symmetric and asymmetric structures [61]. (c) MLI topology using single source and double source modules [62]. (d) Symmetric switched diode MLI [63]. (e) Cascaded switch-ladder MLI [64]. (f) Cascaded switched-diode MLI [65]. (g) Switched capacitor-diode MLI [66]. (h) Switched-battery boost-MLI [67].

Unlike the MLIs in [61-67], that use the level generator stage to produce a unipolar multilevel voltage and a polarity changer to obtain bipolar multilevel voltages, resulting in high voltage stresses across the polarity changer switches, the authors in [69] used bipolar units and a full H-bridge cell to construct a novel asymmetrical MLI topology. Fig. 11 (a) shows the generalized configuration of the proposed topology, in which the bipolar units act as a bipolar level generator (BP-LG) while the H-bridge is used to triple the voltage level count of the BP-LG part. For example, to produce fifteen levels, one five-level bipolar unit, which is linked to the H-bridge cell, is required as depicted in Fig. 11 (b). The bipolar unit uses two equal DC sources of $3E$, generating five levels of $6E$, $3E$, 0, $-3E$, and $-6E$, while the H-bridge uses single DC source of E to generate three levels of E, 0, and $-E$. Accordingly, fifteen voltage levels can be synthesized. The fifteen-level configuration of the proposed topology requires nine unidirectional switches and four power diodes. The main feature of this topology is its ability for producing high-voltage level count while having structure modularity and using a low number of components and active switches. However, its disadvantages include requiring high counts of DC sources and power diodes when enlarging the voltage levels and the high voltage stresses across the switches of the bipolar unit. For example, in the fifteen-level configuration, S_1-S_4 have to block voltages of $6E$, and S_5 must block $3E$. When using a second bipolar cell to produce 75 levels, the voltage stresses become $30E$ and $15E$ for the corresponding switches in the second unit. It is worth mentioning that this topology can produce N level either by increasing the number of bipolar cells as in Fig. 11 (a) or/and connecting several modules in cascade (each module has the same structure as the circuit in Fig. 11 (b)). More details for optimized selections of both cell and module counts can be found in [69].

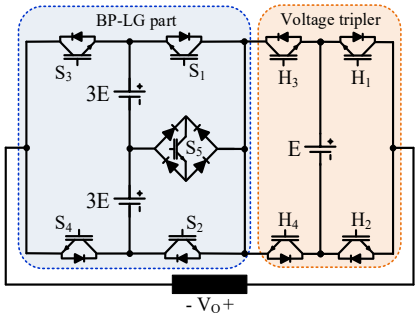


(a) (b)

Fig. 10 Asymmetrical MLI with trinary sequence proposed in [68]. (a) Nine-level configuration. (b) Generalized configuration for producing 3^X -level by using X DC sources.



(a)



(b)

Fig. 11 Asymmetrical MLI topology proposed in [69]. (a) Generalized configuration. (b) Fifteen-level configuration.

A newer single source inverter was proposed in [70], consisting of H-bridges integrated with a bridge-modular-switched-capacitor (BMSC) unit in a way to produce multilevel output with boosting capability. Fig. 12 (a) shows the generalised configuration that uses switched-capacitor (SC) blocks for increasing the voltage level. The boosting capability is a function of the SC blocks number (N_{sc}). The maximum output voltage V_o will be equal to $4*N_{sc}*E$. For example, using one SC block can produce five levels with the gain of four. Fig. 12 (b) shows the five-level circuit, requiring twelve switches, four capacitors, and one DC source. The traditional CHB MLI uses only eight switches and two isolated DC sources for producing the same levels number with a lower output voltage about 50% (e.g. E = 50 V, V_o = 100 for CHB, and 200 V for the proposed topology). On the other hand, in the proposed topology, the voltage stress is a function of N_{SC} while in CHB, it is not related to the number of generated levels.

MLIs topologies with the predefined features for specific applications have been designed in [71-75]. The authors in [71] have proposed a new five-level configuration for minimising the leakage current in transformerless photovoltaic (PV) systems. Fig. 13 (a) shows the proposed converter, consisting of two capacitors, eight switches, and two DC sources (to emulate two PV sources) for producing five levels. The basic concept here is to isolate the PVs from the grid during the zero-voltage state by turning off the four switches in H-bridge and using S_a and S_b for forming a new current path. Accordingly, the flow of the leakage current through the parasitic capacitance will be minimized. The switching losses in the switches of the H-bridge will be reduced effectively by enabling a complete turn-off for each half-cycle. On the other hand, the topology in [72] can eliminate the leakage current by connecting the negative terminal of PV to the grid neutral terminal. Therefore, the stray capacitance will be bypassed. Fig. 13 (b) shows the

five-level circuit for the proposed topology in [72]. As compared to the topology in [71], it can eliminate the leakage current in the PV system by using only six switches, three capacitors, and one DC source (to emulate PV source).

For a PV harvesting system, authors in [73] have developed a new seven-level topology for photovoltaic-battery three-input converter applications, including three cascaded H-bridge, one DC source, three capacitors and two switches for charging purpose. The functionality of the proposed circuit can be explained by two operating modes: when the solar energy is available for PVs during the day, the inverter will be used as a three-cascaded H-bridge topology for producing seven levels as shown in Fig. 13 (c). While during the night when the PVs are off, the converter will operate according to Fig. 13 (d), producing seven levels by using only one single source and three capacitors instead of three isolated DC sources (two sources emulate two PV generators) in the first mode.

In some situations, there is a need for connecting two renewable energy sources that generate a different voltage, e.g. PVs and fuel cells (FCs) to load/grid simultaneously by using fewer conversion stages to obtain high efficiency. To address this issue, dual-DC port MLIs (DP-MLIs) was developed in [74], presenting a new five-level DP-MLI. Fig. 13 (e) shows its simplified version based on T-type inverter, consisting of two asymmetrical DC sources, one diode, six switches. As seen in Fig. 13 (e), only one DC port is used for a high-voltage source while the low-voltage source is connected to the lower port. For grid-connected PV applications, the authors in [75] have developed six-switch 5L-ANPC (6S-5L-ANPC) based on the five-level active neutral point clamped inverter (5L-ANPC)

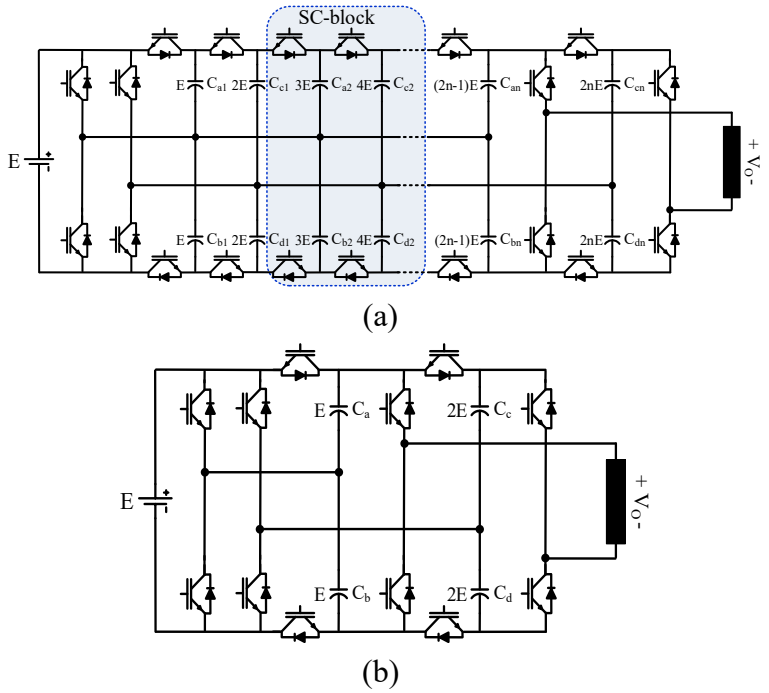


Fig. 12 Flying-capacitor-clamped MLI (FCC-MLI) [70]. (a) Generalised configuration. (b) Five-level configuration.

as shown in Fig. 13 (f). As named, it uses only six switches instead of eight switches like in the traditional 5L-ANPC for producing five levels while requiring two diodes. The idea of reducing the active switches count is based on the fact that

for the grid-connected PV system, the grid voltage and output current are required to be in phase, so it is possible to ignore some paths for reactive current, i.e. some switches can be replaced with diodes.

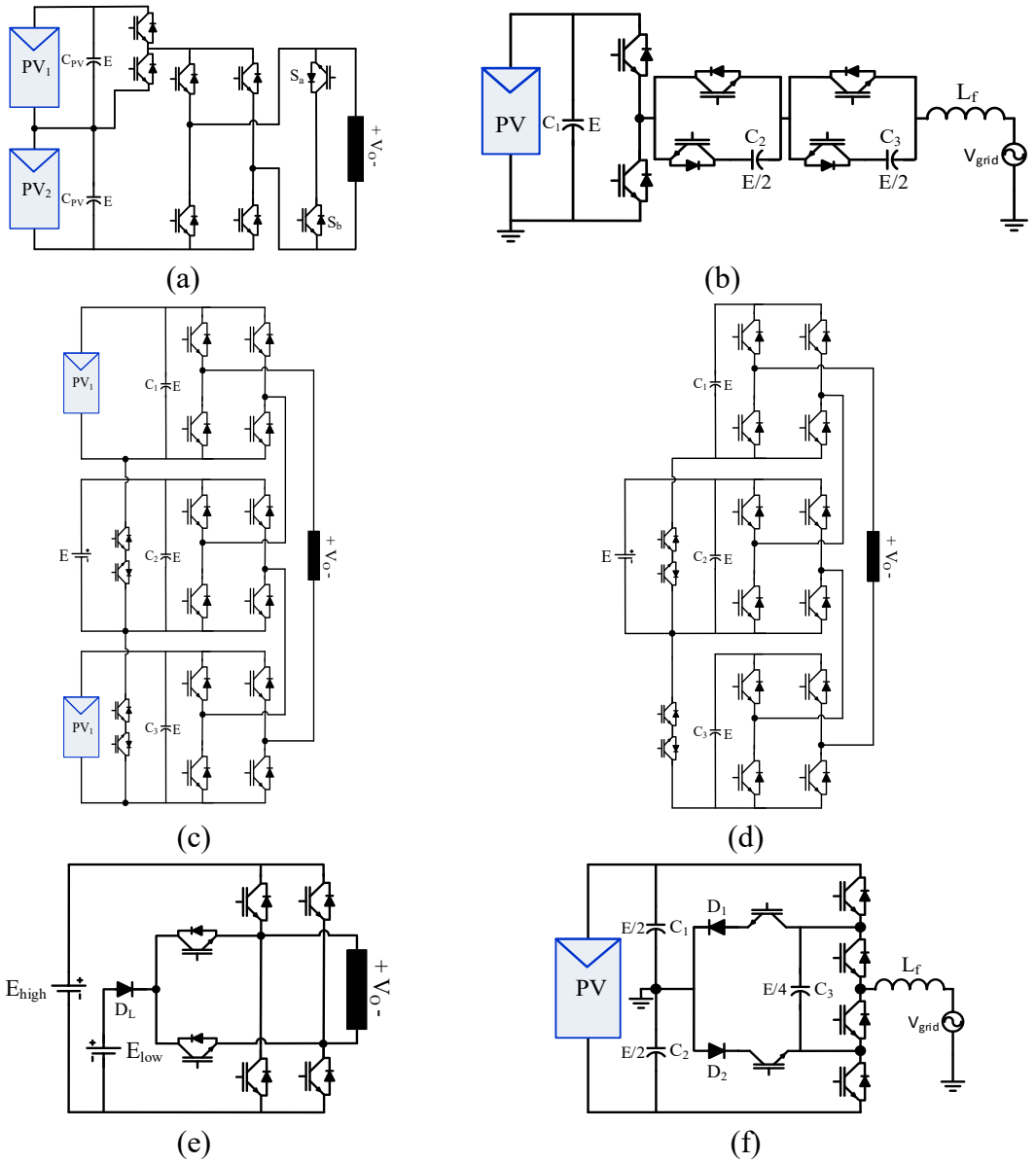


Fig. 13 MLI topologies have predefined features for specific applications [71-75]. (a) Five-level topology for PV systems [71]. (b) Transformerless MLI that eliminates leakage current in the PV system [72]. (c) Seven-level SC topology: when PVs are available during the day [73]. (d) Seven-level SC topology: when PVs are not available during the night [73]. (e) Dual-DC-port asymmetrical MLI [74]. (f) Six-switch five-level topology[75].

A new member of the asymmetrical MLI family was proposed in [76]. This topology has a novel arrangement of components for generating high output levels by using a reduced component count module. Each module needs only ten switches and four asymmetrical DC sources for producing 13 levels. Fig. 14 shows a 25-level configuration, consisting of two primary modules. Although switches have high-voltage stress, especially S_3 and S_4, the proposed circuit is more applicable in

high-voltage high-power industry because of its modularity feature. Inspired by its shape, it is called as envelope type MLI (E-Type-MLI).

Hybrid MLIs have been an attractive trend in literature. Authors in [77] have presented a hybrid *N*-level topology using only one DC source. It has three stages: high-voltage stage, connecting-switches stage and low-voltage stage, as seen in Fig. 15. The first and second stages are fixed while the third stage can be repeated for enlarging the voltage level number. Employing one single DC source is one of the main advantages of this configuration while increasing the cost of having a high number of capacitors is a problem. For this reason, the authors have suggested using the second stage to create extra redundant switching states for making the voltage balance of the flying capacitors easier. One repeated stage, e.g. T-type unit-along with the two fixed stages, is needed for producing five levels, requiring ten switches, four capacitors, and one DC source.

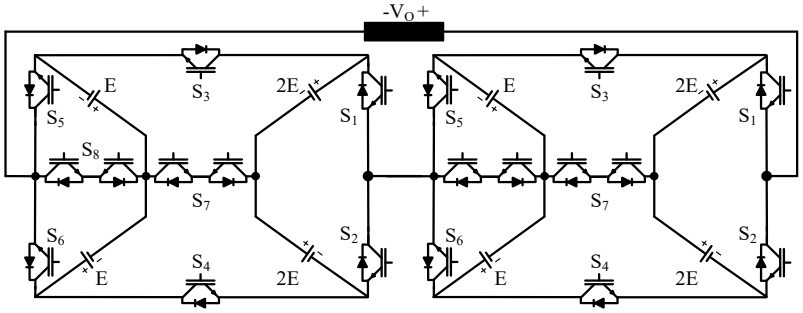


Fig. 14 Envelope type (E-Type) asymmetric MLI [76].

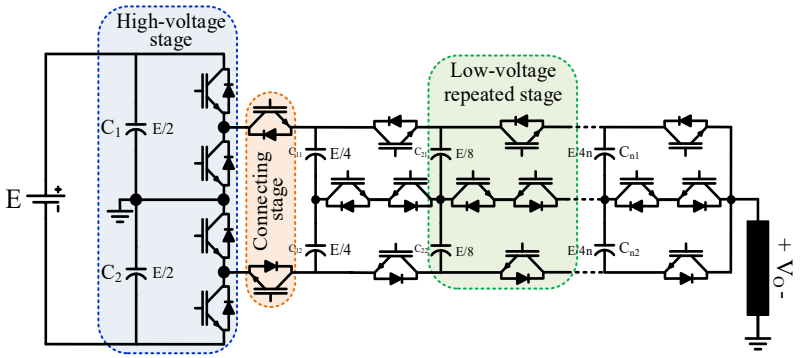


Fig. 15 Hybrid VSI based on T-type topology [77].

A cascaded MLI with a reduced component count was proposed in [78], in which each module has four asymmetrical DC sources. In addition to the four DC sources, it can produce 25 voltage levels with ten switches and eight diodes or can produce only nine-level if using symmetrical DC sources. Connecting modules in cascade results in the *N*-level configuration of the proposed MLI as shown in Fig. 16. Each module has two 'E' and two '5E' DC sources. The capability of producing negative and positive voltages without using the end-side H-bridge is considered one of the key merits of the proposed MLI. However, high-voltage stress across the switches is the main limitation. For example, the right-hand switches S_1, S_2, S_3, and S_4 have voltage stresses of 2*5E while those stresses over the left-side switches S_5, S_6, S_7, and S_8 are 2*E. Moreover, switches S_R and S_L have voltage stresses of 5E and E, respectively. The second asymmetrical *N*-level topology was presented in [79],

being divided into fixed and repeated stages. The N-level configuration is shown in Fig. 17, in which the fixed stage consists of four switches and two DC sources while the repeated stage comprises two switches and one DC source. Although it uses many asymmetrical DC sources for increasing the levels number, it does not use diodes and capacitors, being more attractive features. For generating 15 levels, it requires only eight switches, and three DC sources with a magnitude of E, $2E$ and $5E$. It is worth mentioning that the voltage stress of the switches is a function of levels number. For example, producing 15-level requires four pairs of switches withstand for voltage stresses of $2E$, $7E$, E, and $4E$, fitting well for low-voltage applications.

A group of cross-switched topologies was introduced in [80-82]. Connecting two T-type legs back-to-back was presented in [80], resulting in a new cross-switched T-type based MLI. It uses two cross-connected switches to connect two identical T-type modules in a back-to-back manner, as illustrated in Fig. 18 (a). The cross-switched T-type MLI requires six unidirectional switches (S_1-S_6), two bidirectional switches (T_1 and T_2), and four DC voltage sources (E_1-E_4) to produce nine voltage levels of $-4E$, $-3E$, $-2E$, $-E$, 0, E, $2E$, $3E$, and $4E$ when using symmetrical DC sources ($E_1 = E_2 = E_3 = E_4 = E$), while seventeen voltage levels can be synthesized for the asymmetric operation ($E_1 = E_2 = E$, and $E_3 = E_4 = 3E$). The high voltage stress across the six unidirectional switches is considered as the main disadvantage of this topology. For example, in the symmetrical operation, the voltage stress across switches S_1-S_4 is $2E$, while it is equal to $4E$ for both S_5 and S_6. The situation becomes worse for the asymmetrical mode of operation, where the voltage stress is $2E$, $6E$, and $8E$ for switches (S_1 and S_2), (S_3 and S_4), and (S_5 and S_6) respectively. Low component count, being capacitor-, inductor free, and generating negative voltage levels without using H-bridge are its advantageous features. Another merit of this circuit is the extension possibility. The level count can be enlarged to N levels by cascading the configuration in Fig. 18 (a), as recommended by the authors in [80] and shown in Fig. 18 (b). For producing N levels, $(1.25N\text{-}1.25)$ switches and $(0.5N\text{-}0.5)$ DC sources are required for the symmetrical operation, while under the asymmetrical mode, these numbers become $5(N\text{-}1)/8$ switches and $(0.25N\text{-}0.25)$ DC sources.

Unlike the cross-switched topology in [80], where only T-type modules are integrated with two cross-connected switches, the authors in [81] use the T-type module accompanied with two new modules for forming a single-source step-up MLI topology. Fig. 19 shows its generalized configuration, consisting of three structures: T-type module, cross-connected module, and input module. Among these three modules, only the cross-connected module can be repeated to configure an extendable structure. The N-level voltage requires $(N\text{-}1)/2$ capacitors, $((1.5N\text{-}1.5)+5)$ switches, and $(0.5N\text{-}2.5)$ diodes. For example, for building a thirteen-level configuration, six capacitors, twenty-three switches, and four diodes are required in addition to one DC source. The proposed topology can step up the input voltage (E) to reach a required value by using several capacitors, acting as floating power supplies. Each capacitor is charged to E, boosting the input voltage by a gain of $(N\text{-}1)/2$. However, this feature results in a problem of increasing the number of capacitors, or size and control complexity. Further, the current spikes, that are

common in several switched capacitor topologies [81], need to be reduced by some strategies as detailed in [81]. On the other side, the proposed topology has some of the remarkable merits, like producing higher counts of voltage level without increasing the voltage rating of switches (voltage stress does not exceed 4*E*) and generating bipolar voltage waveforms without the need of an H-bridge.

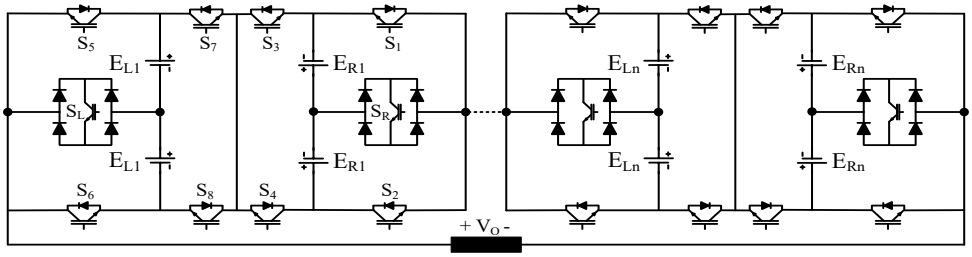


Fig. 16 Cascaded MLI based on a new module with symmetric or asymmetric DC sources [78].

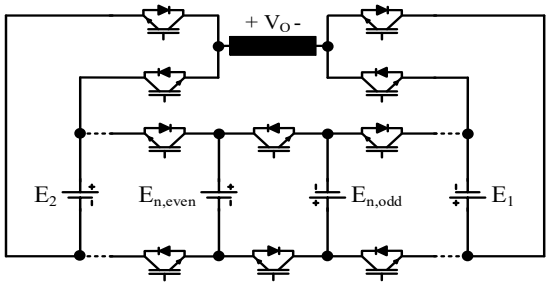
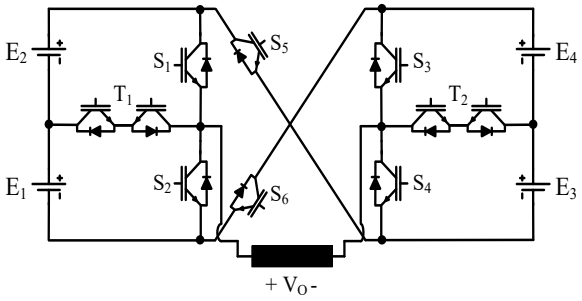
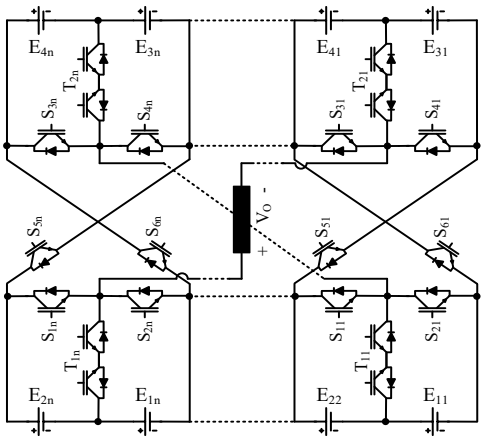


Fig. 17 Asymmetrical MLI with a reduced number of switches [79].



(a)



(b)

Fig. 18 Cross-switched T-type MLI [80]. (a) Nine-, seventeen-level configuration. (b) Generalized configuration.

Another member of the cross-switched MLIs was presented in [82]. It is a cascaded cross-switched topology that can be configured with symmetric or asymmetric DC sources for producing a high-resolution output voltage. Fig. 20 (a) shows its *N*-level configuration, consisting of cascaded *M* modules. Each module is structured by using *K* basic cells in cascade. The output level count can be enlarged by increasing the number of either module or basic cells, or both of them. For example, $(2MK+1)$ and $(4K-1)^{M}$ voltage levels can be obtained from symmetrical and asymmetrical DC sources, respectively, if using (MK) DC sources and $(2MK+2M)$ switches. The authors in [82] recommended a configuration as shown in Fig. 20 (b), being constructed by using two modules, where each has two basic cells (i.e. $M=2$ and $K=2$). It requires twelve switches and four DC sources for producing 9 and 49 levels for symmetrical and asymmetrical operations, respectively. Besides features of being capacitor- and inductor free, the modularity is considered its main merit, allowing for producing *N*-levels without increasing the total standing voltage of the switches. Having a low standing voltage of switches requires many isolated DC sources, making this topology more applicable to PV systems.

A boost active-neutral-point-clamped MLI (ANPC-MLI) was recently proposed in [83], which was derived from an improved five-level ANPC topology in [84]. As compared to the topology in [84], the topology in [83] improves both the voltage gain and level count. The voltage gain can be improved from 1 to either 1.5 or 2.5 while the level count is increased to seven, nine, and eleven levels. These positive features must be compensated by an increase of the switch and flying capacitor counts. Fig. 21 shows both structures of the proposed topology in [83], in which the structure A can generate seven voltage levels with a voltage gain of 1.5, requiring only one extra switch as compared to the five-level ANPC topology in [84]. The structure B can produce nine and eleven voltage levels with the voltage gains of unity and 2.5, respectively, increasing one flying capacitor and three switches as compared to the topology in [84]. The level count in the structure B has two values (nine or eleven) based on the charged voltage of the two flying capacitors C_3 and C_4. When being charged to $0.25E$, the obtained level count is nine. The level count becomes eleven when being charged to E. It is worth mentioning that the voltage stress across switches cannot exceed E for generating seven and nine voltage levels. The voltage stress does not exceed $2E$ for producing eleven voltage levels.

To combine the merits of quasi-Z-source (qZS) and multilevel inverters, the concept of qZS was applied to MLI topologies [85-87], resulting in a family of buck-boost single-stage MLIs with the shoot-through withstanding capability. The authors in [85] proposed a new qZS multilevel topology based on the diode-clamped five-level inverter as depicted in Fig. 22. Two identical qZS networks are used for boosting the input voltage of a single DC source by a factor of B_f, where B_f is equal to E'/E_{in} and called boost factor. Then the five voltage levels of $-B_f E$, $-0.5B_f E$, 0, $0.5B_f E$, and $B_f E$ are generated by the diode-clamped structure. Fig. 22 shows the proposed circuit, producing five voltage levels when using eight switches, six diodes, four inductors, four capacitors, and a single DC source. It is noted that the presented configuration in Fig. 22 can be extended to a three-level

three-phase qZS inverter by adding one more inverter leg (four switches and two diodes) [85]. Using low-rated switches, single DC source, and continuous input current are the advantageous features of the proposed topology. On the other hand, increasing the number of diodes in the circuit and having a boost factor similar to the classic qZS inverter are considered as its main shortcomings [86]. A novel quasi-Z-source (qZS) topology was proposed in [86], integrating a modified impedance network with the MLI topology introduced in [88]. Fig. 23 (a) shows its five-level configuration, in which four capacitors, two inductors, and three diodes are used for constructing the modified impedance network while six switches are used for producing multilevel output. The proposed topology requires a lower component count as compared to the five-level qZS-MLIs in [85, 87], reducing the inductor count by 50% while keeping the same count of switches and

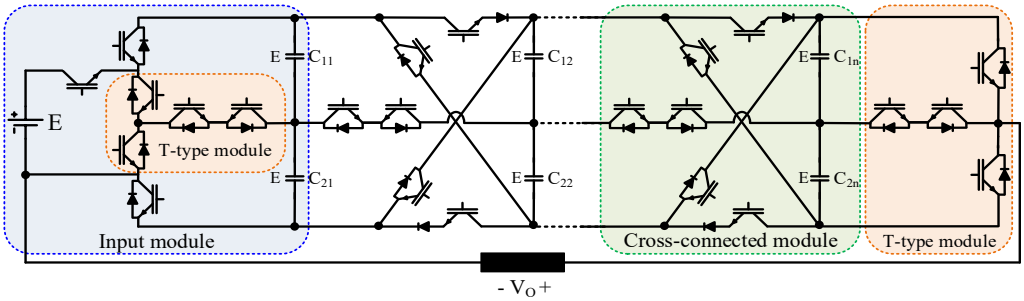


Fig. 19 Generalized configuration of the step-up topology in [81].

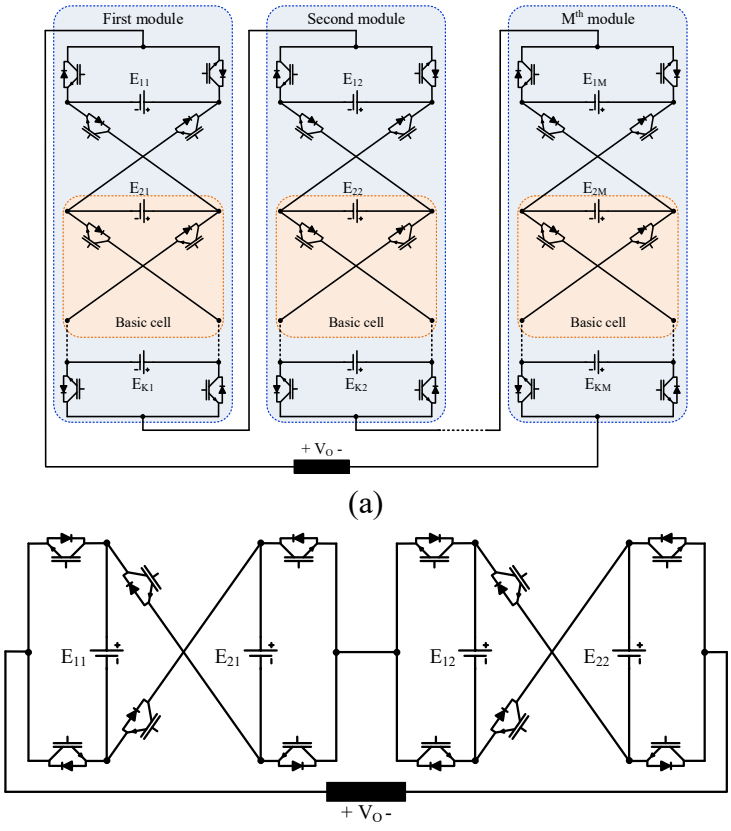
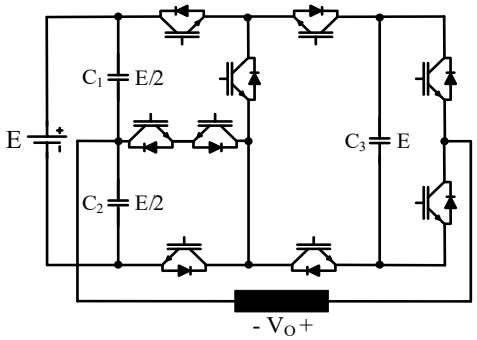
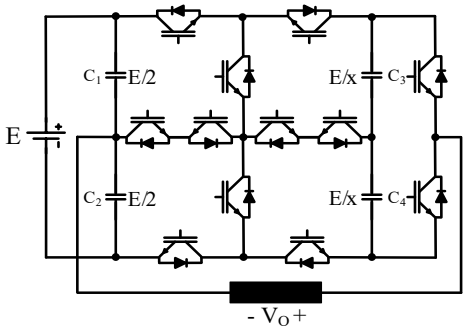


Fig. 20 Cascaded cross-switched topology in [82]. (a) Generalized configuration. (b) Nine-, 49-level configuration.

capacitors. As compared to the topology in [87], it saves one DC source, but requires one extra diode. When comparing with the circuit in [85], it reduces the diode count by three diodes. Further, the proposed topology can double the boost factor, which is not possible in [85, 87]. To achieve these remarkable features, the current stresses of inductors (L_1 and L_2) and the voltage stresses of four switches (H_1-H_4) are doubled. It is worth mentioning that the switches H_1-H_4 are necessary for producing bipolar voltage waveforms and have a rating of full dc-link voltage. Their voltage stress also rises when enlarging the level count. For example, Fig. 23 (b) shows the nine-level configuration of the proposed topology, in which two five-configurations are cascaded, doubling the voltage stresses across switches the H_1-H_4.



(a)



(b)

Fig. 21 Boost active-neutral-point-clamped MLI (ANPC-MLI) proposed in [83]. (a) Structure A, seven-level boost ANPC. (b) Structure B, nine-level (X= 4) or eleven-level (X= 1) boost ANPC.

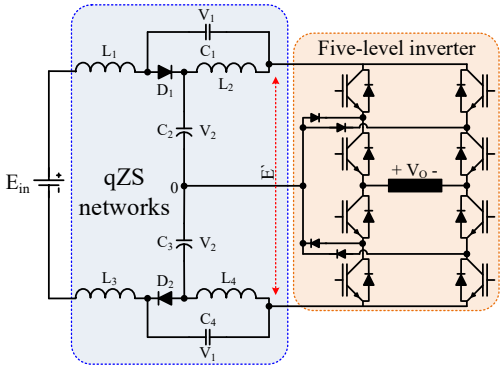
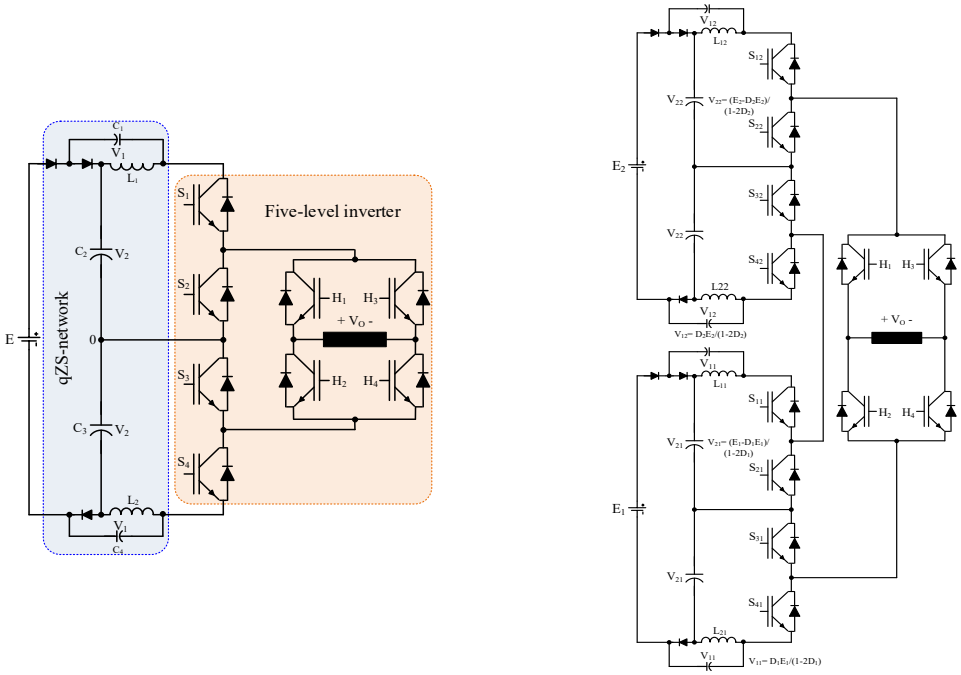


Fig. 22 Five-level quasi-Z-source inverter proposed in [85]. $V_1 = DE_{in}/(2 - 4D)$, $V_2 = (E_{in}(1 - D))/(2 - 4D)$, where D is the shoot-through duty cycle.



(a) (b)

Fig. 23 Modified qZS multilevel inverter in [86]. $V_1 = DE/(1 - 2D)$, $V_2 = (E - DE)/(1 - 2D)$, where D is the shoot-through duty cycle. (a) Five-level configuration. (b) Nine-level configuration.

B. THREE-PHASE MULTILEVEL INVERTERS

This section presents a review of the recently proposed three-phase MLIs based on their operation, advantages, and disadvantages, making the selection of suitable applications easier. The reported topologies in this section represent different types of MLIs such as single source, inductor-based, symmetrical, asymmetrical MLIs for hybrid and non-hybrid configurations. Further some topologies for improving the power quality of power system are included.

One of the salient members in the neutral-point clamped MLIs family is the T-type inverter. It is also known as a neutral-point-piloted inverter (NPPI) and considered as one of the most popular three-level topologies [89, 90]. A single-phase T-type inverter was patented by Conergy in [91], and the authors in [92] presented the three-phase T-type configuration. Fig. 24 shows the T-type inverter for three-phase applications, consisting of a conventional two-level VSI combined with three branches of bidirectional switches, being assumed as a common-emitter configuration. Each branch connects the midpoint of the DC link to one leg of the two-level VSI, forming a T-type shape. The six switches of the VSI (S_1-S_6) are rated at the input voltage E, while the remaining switches have voltage ratings of $0.5E$. One counterpart to the T-type MLI is the diode-clamped MLI, which requires six clamping diodes while the T-type uses six switches instead. Both of them uses a single DC source and two capacitors, and twelve switches for producing three voltage levels. The distinct feature of the diode-clamped inverter is that it has lower voltage stresses of the switches ($0.5E$) than those in the T-type (six switches of E, six switches of $0.5E$), reducing the switching losses. On the other hand, the T-type inverter has a lower component count in the current path, reducing the conduction

losses. Further, only one switch is required in the current path for positive or negative output voltage while two switches are needed in the diode-clamped inverter regardless of the output level [90-94]. Accordingly, the T-type MLI is more advantageous in applications, requiring low switching frequencies alone.

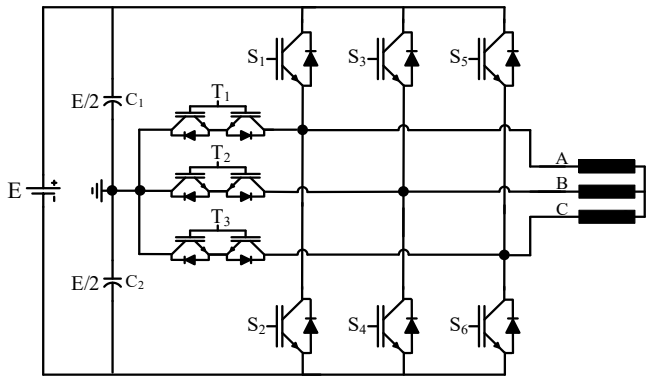


Fig. 24 Three-phase T-type multilevel inverter [92-94].

Single-stage multilevel inverters (SS-MLIs) with boosting capability have been recently proposed in [95-97] for PV, uninterruptible power supplies (UPS), and fuel cells (FCs) applications. Typically, the boosting stage and multilevel stage are merged to form single-stage converters that have both merits of boost converters and MLIs. For example, a new SS-MLI called three-level LC-switching based NPC (3L-LC-NPC), was presented in [95]. Fig. 25 (a) shows its complete configuration, consisting of a boosting circuit (BC) connected to a conventional three-level NPC, allowing for the capability for boosting the input voltage and producing improved quality output. The BC consists of four diodes, two switches, two inductors, and two capacitors, while twelve switches, six diodes, and two DC sources are required for the three-level NCP circuit. Compared to the conventional Z-source MLIs (ZS-MLIs) in [98, 99], the proposed topology reduces 50% of capacitor and inductor count, and having a continues input current, but uses two extra diodes and two switches. In addition to the NPC limitations, using several high-power passive elements in the boosting stage increases the weight, cost, complexity, and the losses of the inverter.

Another topology of SS-MLIs with the boosting feature was introduced in [96], producing the same voltage levels like the topology in [95]. Instead of using NPC, the topology in [94] uses a T-type MLI to produce multilevel waveforms. Two identical quasi-Z-source networks are used for the boosting circuit, as shown in Fig. 25 (b). Compared to the topology in Fig. 25 (a), only two diodes are required by using the T-type MLI. Without using switches in the BC, the count of capacitors and inductors is doubled. Three bidirectional switches in the topology increase the redundancy of the switching states, enabling fault-tolerant capabilities for some common faults, e.g. open-circuit failures. Fig. 25 (c) shows a new three-level topology proposed in [97], having the same number of the levels in [95, 96]. This topology is an upgraded configuration of the two-level split-source inverter (SSI) in [100]. Because of its ability for generating a boosted voltage with three-level waveforms, the direct connection of low-voltage energy sources, namely PVs and

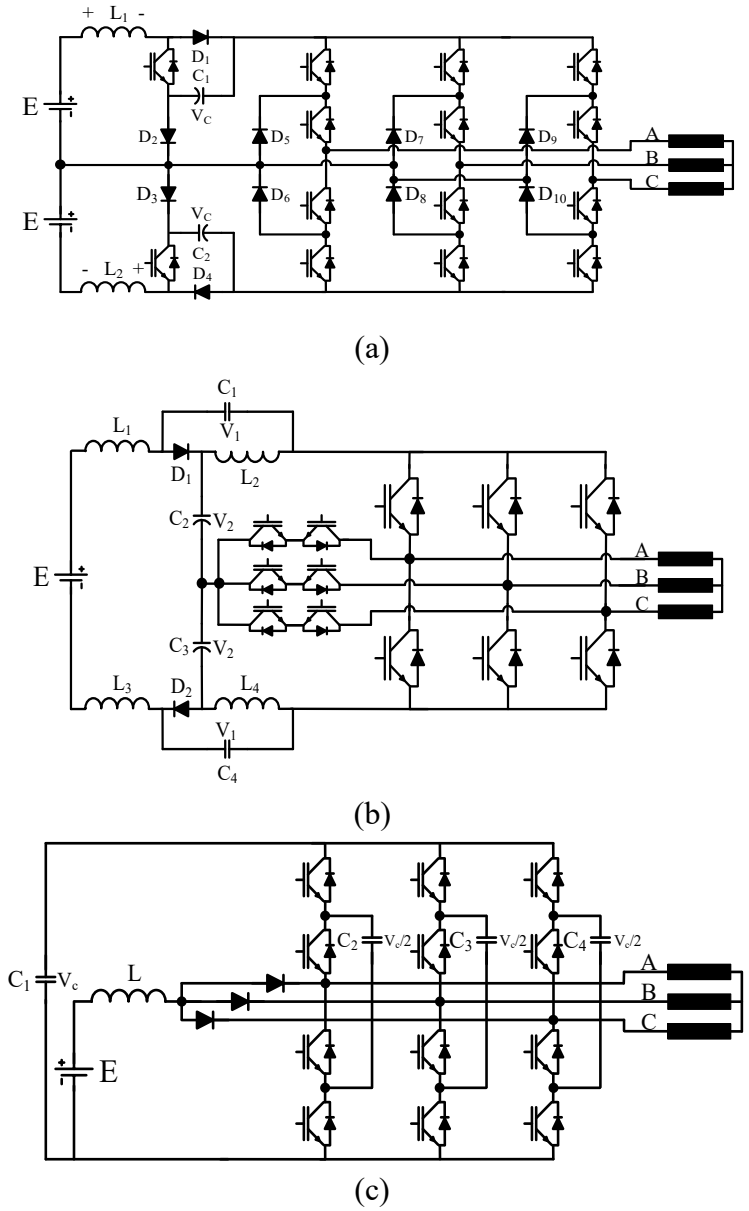


Fig. 25 Single-stage multilevel inverters with boosting capability [95-97]. (a) Three-level LC-switching-based voltage boost NPC MLI [95]. $V_c = E/(1 - 2D)$, where D is the shoot-through duty cycle. (b) Quasi-Z-source inverter with a T-type MLI [96]. $V_1 = DE/(2 - 4D)$, $V_2 = (E(1 - D))/(2 - 4D)$, where D is the shoot-through duty cycle. (c) Three-phase three-level flying capacitors split-source MLI [97]. To maintain a three-level operation, V_C should be larger than $2E$.

fuel cells, become more accessible and efficient. Producing three levels needs twelve switches, three diodes, four capacitors, one inductor, and one DC source. The proposed topology has several attractive features like boosting capability, using a single DC source, continuous input current, and having a reasonable number of passive components. On the other hand, several limitations can be found as high-current and -voltage stresses on the used semiconductor devices, lack of modularity, increasing the control complexity and system footprint, decreasing the expected lifetime because of using flying capacitors and inductor. Further, this topology needs extra efforts in control algorithms for removing the low-frequency

components from not only output voltages but also input currents caused by voltage oscillations of the flying capacitors.

A symmetrical hybrid MLI for high-speed motor drive systems was presented in [101] as shown in Fig. 26, consisting of 36 switches, twelve capacitors, and three DC sources for generating nine voltage levels. It uses two cascaded three-level flying capacitors (3L-FC) to work as a multilevel DC-link (MLDCL) generator stage, producing a five-level DC voltage waveform. Additionally, a full H-bridge is used as a polarity-changer. The MLDCL stage requires low-voltage switches to operate at high frequencies, while high-voltage switches are required for the low-frequency H-bridge. Using a reduced isolated DC source count and applying low-switching frequency for the four switches in each H-bridge are the main features of this MLI. However, the voltage balancing issues for capacitors under dynamic and nonideal conditions and the needs for high-voltage switches that can withstand the full voltage of the dc-link are considered the key drawbacks.

Authors in [102] have proposed a new unit acts as a building block for both low-voltage and high-voltage MLIs, as shown in Fig. 27 (a), generating 9-, 7-, and 11 levels by using two DC voltage sources with ratios of 1:1, 2:1, and 2:3, respectively. It requires one bidirectional switch, six unidirectional switches and a voltage divider network formed by connecting two capacitors in series. Despite using only two DC sources, a high number of capacitors are required for generating N levels, as shown in Fig. 27 (b). Accordingly, the proposed MLI suffers from the drawbacks mentioned above of using capacitors. Fig. 27 (b) shows that the switches S_c and S_d must withstand a voltage of (E_1+E_2), being applicable for low-voltage applications alone. The structure in Fig. 27 (c) can be used in high-voltage applications, but the advantage of using only two DC sources will be lost by cascading several units of two DC sources.

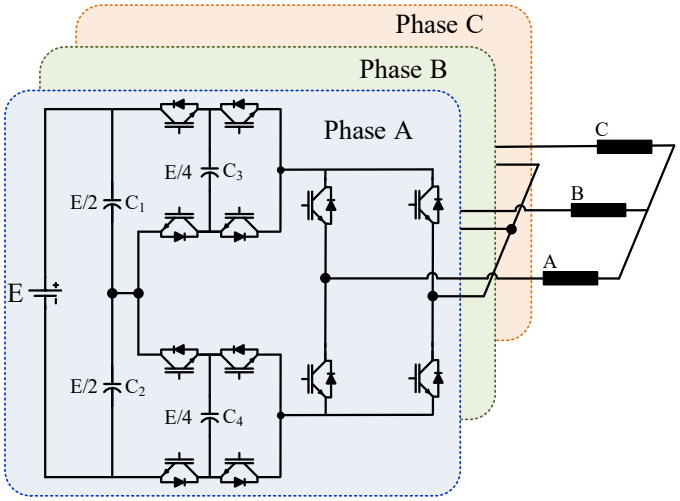


Fig. 26 Hybrid nine-level inverter for high-speed motor drives [101].

Alternatively, for medium-voltage applications, new MLI topologies were presented in [103, 104]. Fig. 28 shows the schematic diagram of the topology in [103]. It is an upgraded circuit of the nested neutral point-clamped (NNPC) converter in [105]. The presented topology requires extra six switches and three flying capacitors, but it can produce five voltage levels instead of only four levels

in [105]. As observed in Fig. 28, using a significant number of flying capacitors and diodes, along with lack of modularity are the main limitations of this circuit. However, using less DC sources and having low-voltage stress across the switches are its main features. In [104], the authors have proposed a new six-level topology, being formed by combining three three-level flying capacitor legs with six two-level legs as shown in Fig. 29. Despite using only one DC source, six capacitors and 24 switches are required for producing a three-phase voltage. While having a reduced count of switches and DC sources, the proposed inverter must use many capacitors that have diversified voltage ratings, requiring a voltage control for the flying and DC-link capacitors. Therefore, the authors have used the reported circuit in [106] for balancing the capacitors in the DC-link, along with a pre-charging process for the flying capacitors. For the proposed topology, it is important to mention that the auxiliary circuit for voltage balance of the DC-link capacitors is especially essential at a wide range of load power factor (PF) [104].

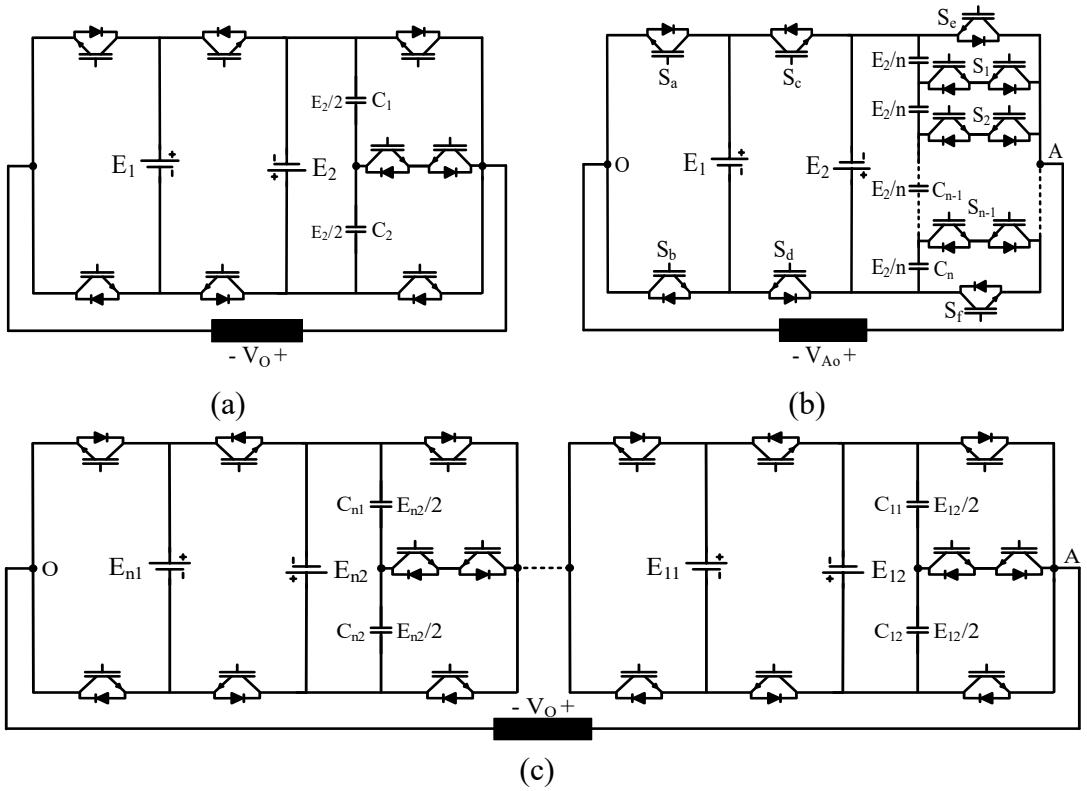


Fig. 27 MLI for interfacing renewable energy sources with low-, medium- and high-voltage grids [102]. (a) Basic unit for generating 7-, 9-, and 11-level. (b) Two DC sources *N*-level configuration (leg A). (c) Multiple DC sources *N*-level configuration (leg A).

In transformerless PV systems, designing converters requires features like boosting capability, longer lifetime and zero common-mode voltage (CMV) [107]. To design a zero CMV converter, a modified T-type three-level inverter was presented in [107], merging the traditional T-type inverter with a DC-link that has four capacitors through two pairs of switches as shown in Fig. 30. Contrary to other solutions for eliminating the CMV in [108], the proposed topology has a low count of switches and capacitors and uses only 16 switches and four capacitors while eight capacitors and 24 switches are required in [108]. However, the total standing

voltage of the switches in [107] is higher than that in [108]. Further, for PV systems connected to a microgrid, a new hybrid modular multilevel inverter (MMLI) was proposed in [109]. Because of using a high number of DC sources, it is most applicable for PV farms where realising DC voltage is easy. Fig. 31 shows the schematic diagram of its three-phase arrangement, in which a three-level T-type inverter works as the main stage, and a new four-level cell is connected in cascade for producing more levels. The new four-level cell is a modified full H-bridge and constructed from two capacitors, four switches and two DC sources. The reduced switch count and the ability for operating in symmetrical or asymmetrical modes are the main features of this MLI. By employing the asymmetrical mode, the output level number will be increased while the component count will be the same. However, the topology must use different DC sources with proper voltage ratings, increasing the voltage stress across some switches. By using only one cell per phase in addition to the main stage, nine voltage levels can be achieved with 24 switches, eight capacitors, and seven symmetrical DC sources.

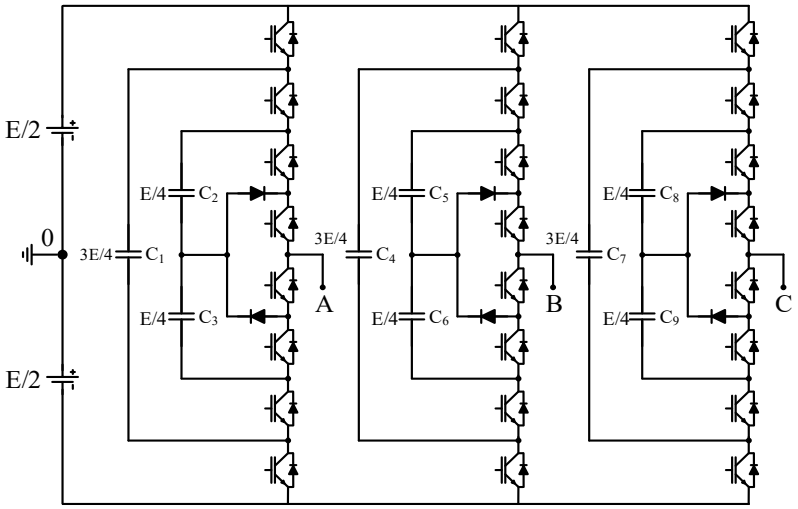


Fig. 28 Five-level VSI for medium-voltage applications [103].

A new optimised multilevel topology was presented in [110], and Fig. 32 shows its configuration for producing N levels. Despite using the same main stage as topology in [109], i.e. T-type MLI, it has a different level-generator (LG) stage for enlarging the level number. Further, it is noted from Fig. 32 that the LG stage is subdivided into two identical units of one DC source and N_{HBs} half H-bridge cells. This topology could work as a symmetrical and asymmetrical MLI, requiring $(4N_{\mathrm{HBs}} + 12)$ switches and $(2N_{\mathrm{HBs}} + 2)$ DC sources for producing $(N_{\mathrm{HBs}} + 3)$ and $(2^{N\mathrm{HBs}} + 2)$ levels for symmetrical and asymmetrical operation, respectively. Diode-, capacitor-, inductor-free and low component count are the main features of this circuit. In contrast, lack of modularity is considered the main demerit of this inverter, limiting the level count because of high-voltage stress across the six unidirectional switches in T-type stage. These switches must withstand a voltage equal to the generated voltage by the LG stage.

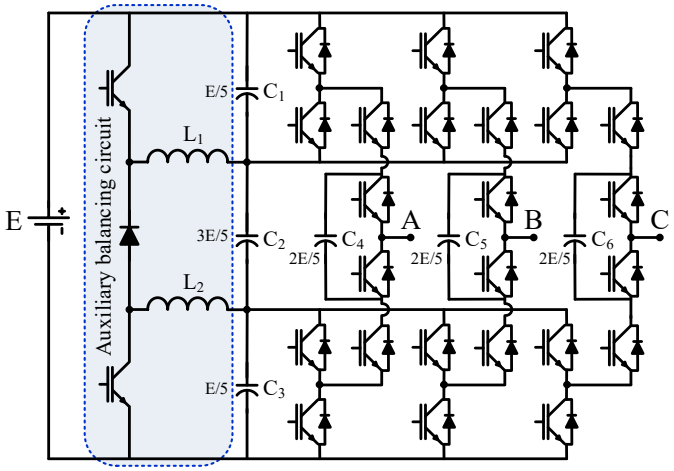


Fig. 29 Six-level MLI topology for medium-voltage applications [104].

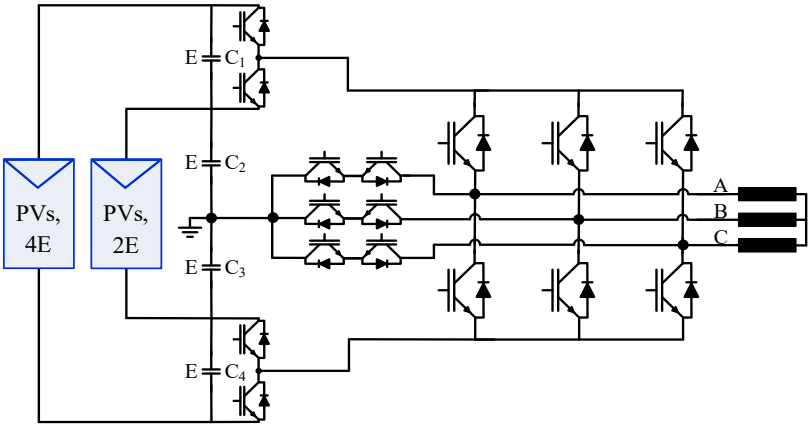


Fig. 30 Modified T-type three-level inverter for minimising CMV [107].

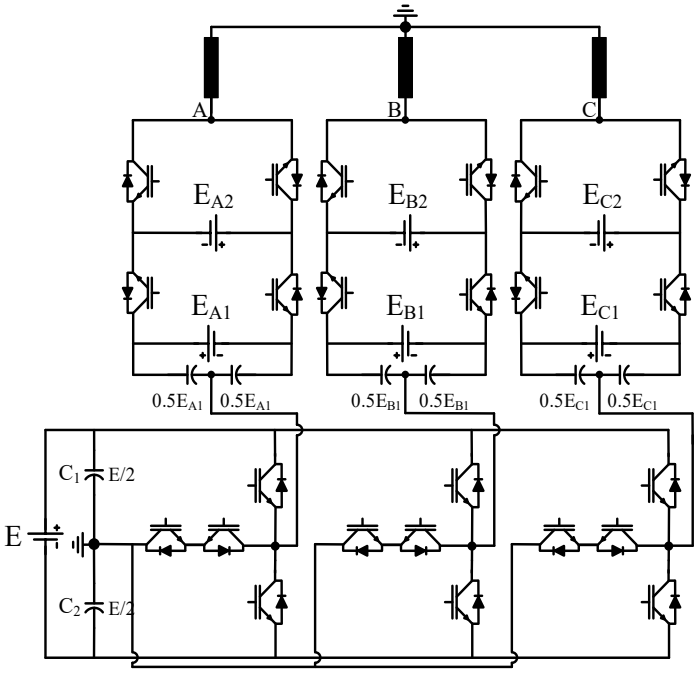


Fig. 31 Three-phase hybrid MLI for renewable energy [109].

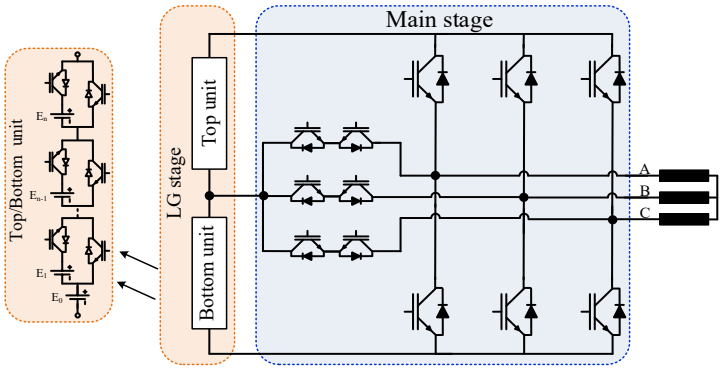


Fig. 32 Three-phase MLI topology with separate level and phase sequence generation part [110].

Novel asymmetrical hybrid inverters in [111, 112] can produce N levels with a reduced component count. The topology in [111] has two different stages, as shown in Fig. 33. Stage I consists of a traditional six-switch two-level inverter connected to DC-link through a bidirectional switch network, in which each DC source is connected through one switch to one inverter leg. Stage II consists of three half H-bridge cells (one cell for each phase). Stage II is responsible for doubling the level count, so it is called a doubling unit. In spite of reducing the component count, it increases the rating voltage of components. As seen in Fig. 33, by using N_{DC} voltage sources of E, six switches must withstand N_{DC}*E, and the other six switches in stage II have a rating more than N_{DC}*E and different ratings of the bidirectional switches based on its position. Alternatively, Fig. 34 shows the non-isolated-source based topology reported in [112], using stage II of topology in [111] to build a string of cascaded cells that are responsible for producing (N-2) levels. Moreover, two extra levels are generated by a new structured unit (NSU). As shown in Fig. 34, the NSU is formed by three modified cells connected in

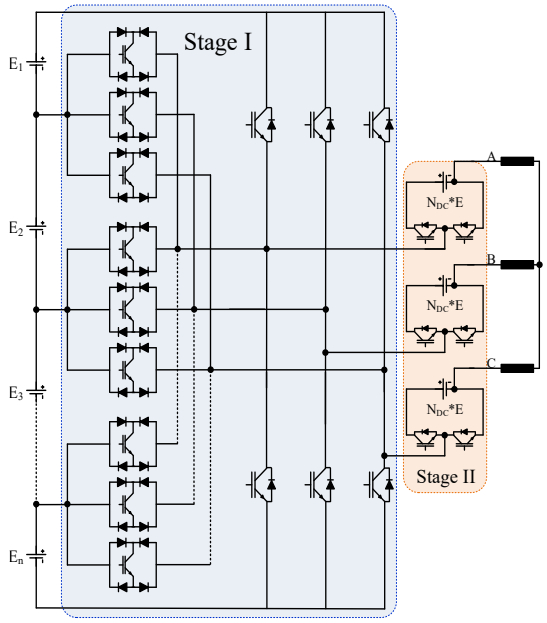


Fig. 33 Three-phase MLI using voltage doubling-unit [111].

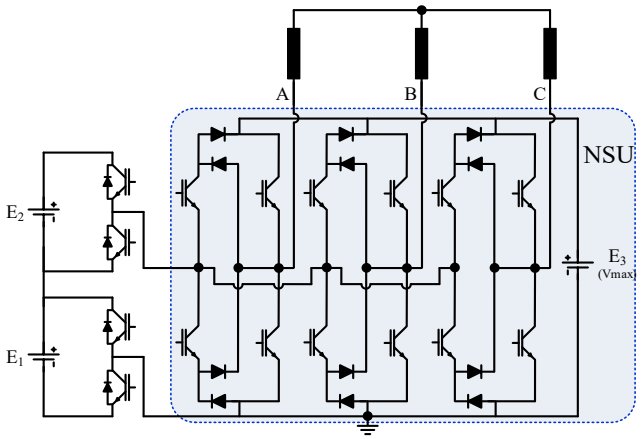


Fig. 34 Three-phase configuration based on cascaded half-bridge [112].

parallel with a DC source of V_{max}. The NSU can produce minimum and maximum levels of the generated voltage, i.e. 0 and V_{max}, while the half H-bridge string generates the rest of levels. Generating four levels requires three DC sources of E, E, and $3E$ besides sixteen switches and twelve diodes. Although the number of levels is maximized in term of the component count, the total standing voltage is dramatically increased in a similar way to the topology in [111].

The concept of generating a high number of levels by stacking capacitor-based full H-bridge cells was used in [113]. This concept is widely adopted for designing new circuits by using a low number of DC sources while increasing the number of flying capacitors. For enlarging the number of levels, each group of the capacitors has a different voltage reference as compared to previous and subsequent groups. Therefore, additional voltage balancing algorithms are required for maintaining the capacitor voltages at the respective values. The nine-level circuit for the topology in [113] is depicted in Fig. 35, in which each phase has two three-level FCs, one selector cell, and one capacitor-fed full H-bridge unit (CF-HB). Producing nine levels requires two symmetrical DC sources (each of $0.5E$ volt), 42 switches (6, 24, and 12 switches having blocking voltages of $0.5E$, $0.25E$, and $0.125E$, respectively), and nine capacitors (six of $0.25E$ and three of $0.125E$). It can generate N levels by increasing the number of FC and CF-FB cells, in addition to a modification in the selector cell.

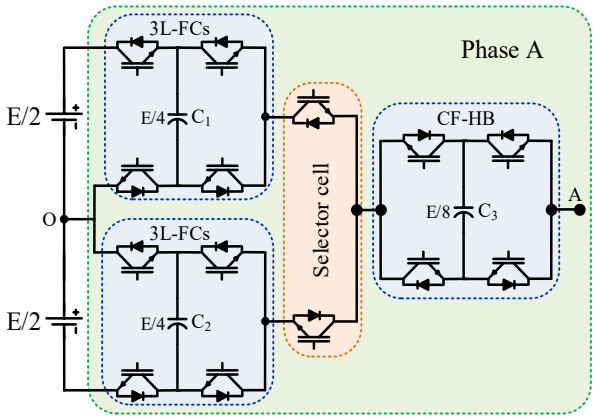


Fig. 35 One phase of a topology formed by stacking inverters of lower multilevel structures [113].

Based on the conventional two-level voltage source inverter (2L-VSI), two MLIs were proposed in [114, 115]. In [114], the authors have presented a novel arrangement of two 2L-VSI. The proposed topology can generate N levels by using N_{DC} voltage sources and $(2(N_{DC})^2 + 2N_{DCs})$ bidirectional switches, where each switch is built by connecting two unidirectional switches in the common-emitter configuration, reducing the required gate driver count. Fig. 36 shows its scaled-down circuit, being formed by connecting only two 2-level inverters in parallel while requiring 24 switches and two asymmetrical DC sources of E_1 and E_2 volt. Under the suggested PWM scheme by the authors, it can provide four levels $-E_1$, 0, E_2, and (E_1+E_2) in the pole voltage and six-level line voltage. Using a high number of switches is one key limitation of this topology while using a low number of DC sources and having low requirements for the gate driver circuits are the main features. Contrary to connecting the 2L-VSIs as in [114], the authors in [115] have merged them in a distinct way for constructing a novel three-level unit as depicted in Fig. 37, in which two symmetrical DC sources and only twelve unidirectional switches are used. Several units with extra three switches must be cascaded for enlarging the number of levels. This topology has merits of using a low count of DC sources, and capacitor- and diode-free, being beneficial for control simplicity, compact design, long lifetime and low cost. However, a moderate total standing voltage of the bottom three switches S_4, S_8, and S_{12} is the main limitation of this MLI.

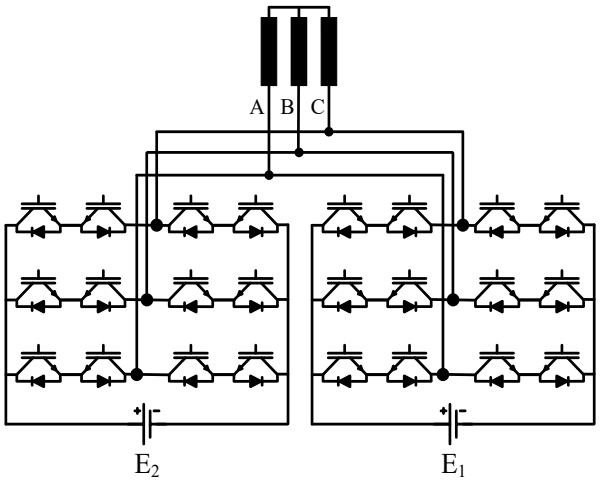


Fig. 36 Four-level topology for renewable energy grid integration [114].

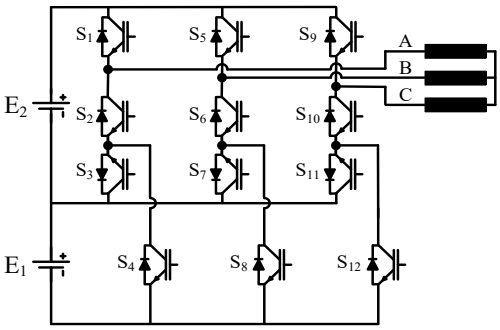


Fig. 37 Three-phase three-level MLI based on two-level VSI [115].

A three-phase single source topology for standalone applications was presented in [116]. It is formed by three identical legs, sharing the same DC-link. Each leg has two unidirectional switches and two bidirectional switches, as shown in Fig. 38. The DC-link consists of a single DC source accompanied by three voltage-divider capacitors C_1, C_2, and C_3. Controlling switches in each leg properly allows this topology to produce four levels 0, $E/3$, $2E/3$, and E in the pole voltage V_{A0}, or result in seven levels of E, $2E/3$, $E/3$, 0, $-E/3$, $-2E/3$, and $-E$ in the line voltages. Using a single DC source, low count of active switches, and having only three ON-switch at any level are its main advantages. Its key disadvantages include using three capacitors, twenty-four power diodes, and high-voltage stresses, which are

equal to the full dc-link voltage across the six unidirectional switches while the six bidirectional switches must block 66.67% of the full dc-link voltage.

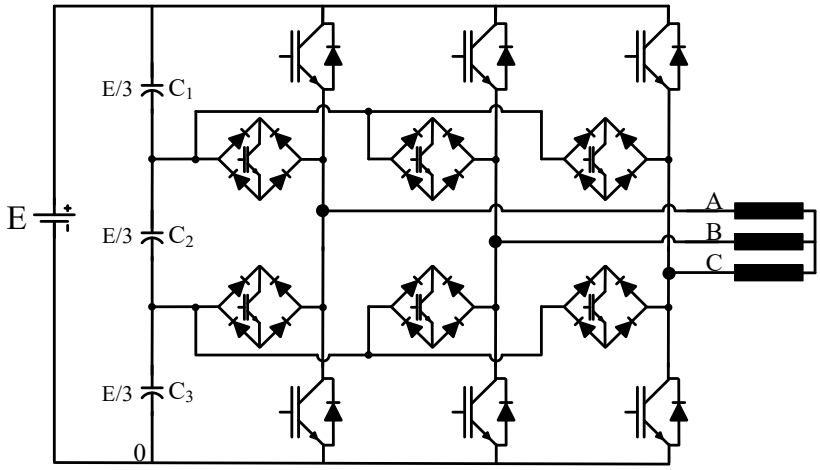


Fig. 38 Three-phase four-level inverter proposed in [116].

As highlighted above, the multilevel inverters are salient candidates for several applications in both renewable energy systems and motor drives. Further, MLIs become a featured solution for improving the power quality in power systems. They can operate as static synchronous compensators (STATCOMs) and unified power quality conditioners (UPQCs), handling reactive power demand, harmonics compensation, and voltage disturbances (e.g. sag/swell). Flying-capacitor MLI (FCMLI), diode-clamped MLI (DCMLI), and cascaded H-bridge MLI (CHBMLI) are widely used to form multilevel-based STATCOMs [117-121]. Both FCMLIs and DCMLIs have DC-link shared among the three phases, improving the compensation of the negative-sequence currents as compared to the star-connected CHBMLI. These two topologies have a problem of poor modularity and using high capacitor and diode counts. The CHBMLIs have a remarkable feature of modularity, making them more attractive than FCMLIs and DCMLIs. However, connecting the CHB in a star-configuration reduces the compensation capability of the negative-sequence current. This drawback is solved by applying a delta-configuration of CHB, but this would boost the arming voltage of the converter, increasing the submodule count or rating the components [122].

Scalability and transformerless capability of the modular multilevel converter (MMC) make it reasonably competitive for replacing the conventional MLIs in high-voltage STATCOM applications [123]. Fig. 39 shows the conventional MMC-based STATCOM configuration, consisting of three-phase legs connected to two bulk capacitors (C_U and C_L). Each phase has two arms (lower and upper arms) and two inductors (L_{a1} and L_{a2}). For constructing both arms, several submodules are cascaded, typically a flying capacitor connected to either half-bridge (HB) or full-bridge (FB). The arm inductors L_{a1}-L_{a6} are necessary for limiting the current during faults and reducing the harmonic content in the circulating current. Balancing the voltage of flying capacitors is a significant challenge in STATCOM-based MMC, requiring complex control algorithms and a high number of voltage sensors [122-124]. The authors in [122] proposed a solution to keep the capacitor voltage in different submodules balanced, reducing

the sensor count and computational burden in control algorithms. The conventional arm structure based on cascaded HB cells is depicted in Fig. 40 (a), while Fig. 40 (b) shows the proposed one. In the proposed structure, a balancing branch (BB), formed by a series connection of low-power rating inductor and diode, is added between the neighbored cells. The diodes are used to clamp the voltage of capacitors naturally from the bottom cell upwards. Using inductors is mandatory to suppress the current pulses during abnormal conditions, protecting the switches and reducing the diode current ratings. According to the proposed solution, only the voltage of the capacitor in either the top or bottom of each arm must be controlled and monitored. The remarkable features of simplifying voltage balancing control and low sensor count come with the cost of increasing the component count (diodes and inductors) as compared to the conventional MMC.

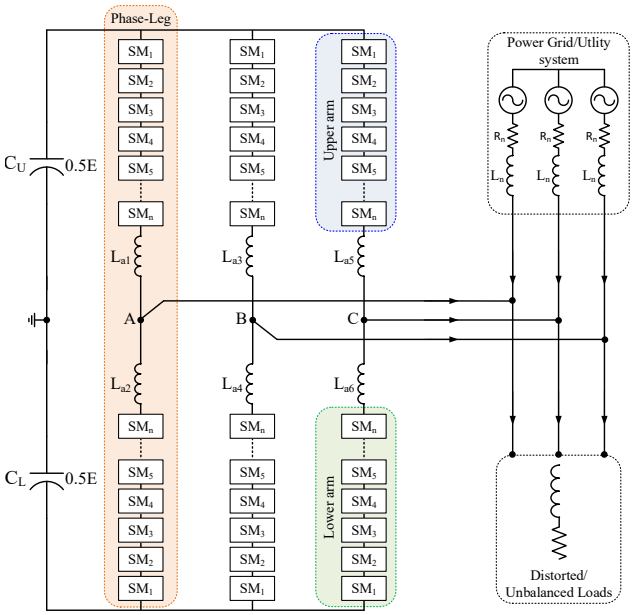
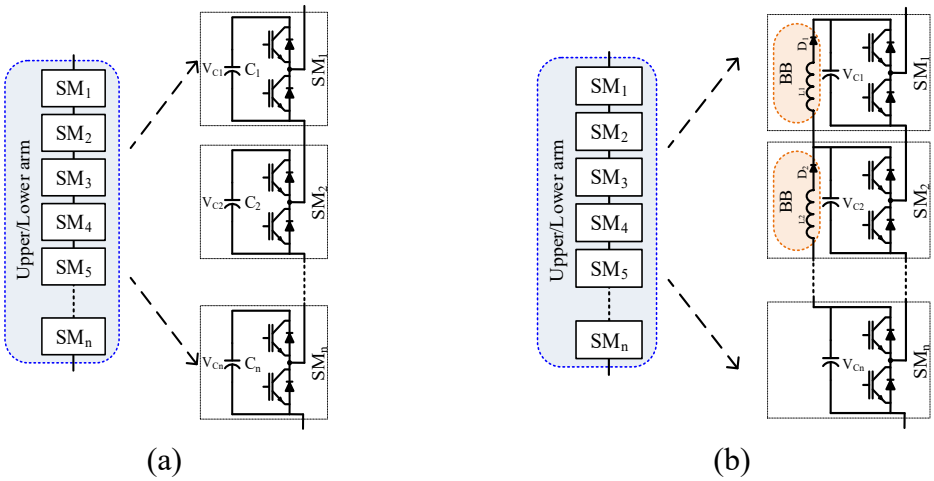


Fig. 39 MMC-based STATCOM configuration.



(a) (b)

Fig. 40 Arm structures based on half-bridge cells for MMC-based STATCOM. When capacitors voltage is balanced, V_{Ci}= E/n where i= 1, 2,…, n. (a) Conventional structure of an arm in MMC-based STATCOM. (b) Proposed diode-clamped arm structure in [122] for MMC-based STATCOM.

To synthesise a desired multilevel AC voltage, a large count of floating capacitors is required in the MMC-based STATCOM, in which electrolytic capacitors are normally used to fulfil the high-capacitance requirements for buffering energy variations. Besides the well-known disadvantages of using a large number of capacitors [125], the electrolytic ones have a higher failure rate than other components in the systems [125-127]. To lower capacitor count and voltage rating of switches while producing higher voltage levels, some transformer-based solutions were proposed in [128, 129]. The authors in [128] introduced a four-level STATCOM configuration based on cascading two conventional two-level inverters as depicted in Fig. 41. Two corresponding legs of the two-level inverters are connected through one winding of a three-phase transformer. The low-voltage (LV) windings are used for cascading the two inverters while the three windings of the high-voltage (HV) side are connected to the grid terminals. To obtain a four-level operation, the voltages of the two DC-link capacitors are regulated to have asymmetrical values. One three-phase transformer is needed in addition to twelve switches and two capacitors. This topology has a simple structure and a low component count. However, the demerit of using a three-phase transformer (in term of size and cost) restricts its applicability, being more advantageous in low-capacity STATCOMs. A modified topology of the presented STATCOM configuration in [128], was proposed in [129]. Three two-level inverters and a three-phase transformer are used to construct the proposed STATCOM in Fig. 42. One leg in each inverter is used to connect the three inverters in a Y-configuration, while the remaining two legs are connected to different windings in the low-voltage side of the transformer. This connection makes the applied AC voltage of the transformer windings double the DC voltage across the capacitor. Under the regulation of the capacitor voltages at symmetrical values, the proposed configuration produces five voltage levels of $-2E$, $-E$, 0, E, and $2E$ across each transformer winding, requiring one three-phase transformer, three capacitors, and eighteen switches. As compared to [128], the proposed topology needs one extra two-level inverter (i.e. one capacitor and six switches). Consequently, the applied voltage across the transformer winding is increased from 1.33 to double the capacitor voltage while producing five levels instead of four, lowering both THD value and component ratings. It is worth mentioning that the topologies in [128, 129] have been introduced for driving open-end winding induction motors [130, 131].

Another significant application of the MLIs in the field of power quality is constructing more competitive unified power quality conditioners (UPQCs). Briefly, UPQC consists of two compensators, in which the series compensator is responsible for handling voltage related issues (e.g. voltage sag/swell, flickers, etc.) and the shunt compensator is to tackle issues of harmonic and reactive power compensations [132-140]. Several configurations for UPQCs based on conventional MLI topologies were proposed in [133-136], suffering from a high component count or limited level count due to using many capacitors or diodes or transformers. The modular multilevel converter (MMC) concept was applied to obtain UPQCs with higher power levels [137-139]. Fig. 43 shows the UPQC based on two MMCs. The MMC-A acts as a series compensator, being connected to the

grid through a series injection transformer (T_C), while three coupling inductors (L_a, L_b, and L_c) are used to interface the shunt compensator (i.e. MMC-B) to the grid. It is worth noting that the coupling inductors can be used for smoothing the currents. Attractive features, namely high-quality waveforms, fast current control, and easy scalability of voltage and current, are important in applying MMC to UPQC. On the other hand, using many floating capacitors as storage elements, increasing size and failure rates, is its main limitation for UPQCs.

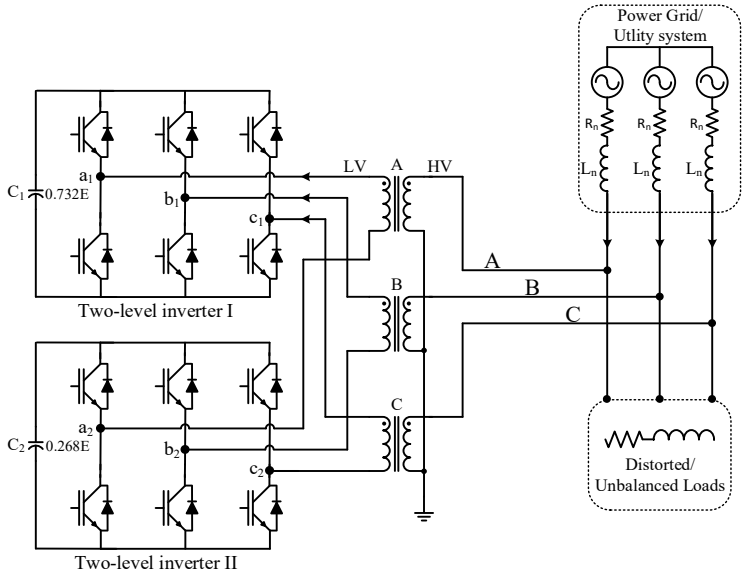


Fig. 41 STATCOM based on cascading two two-level VSIs in [128].

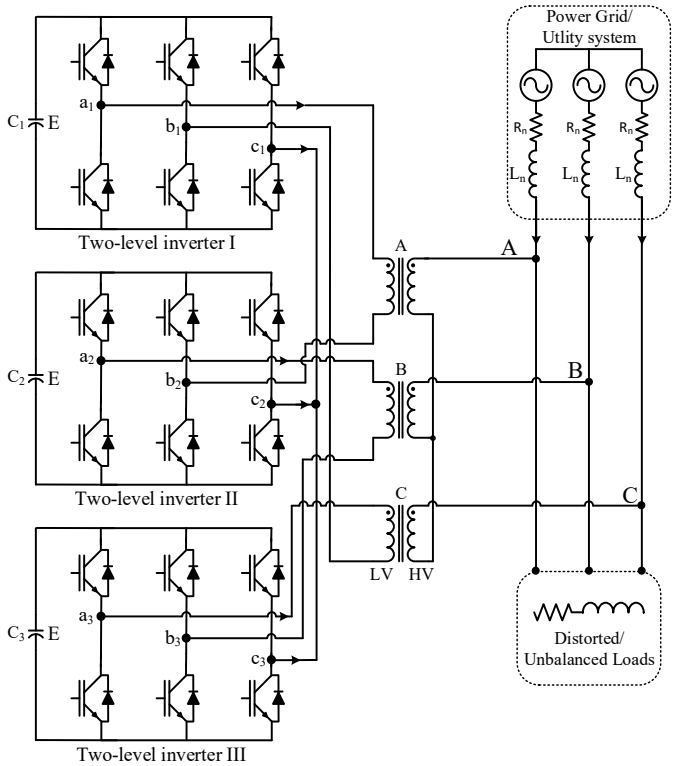


Fig. 42 STATCOM based on three two-level VSIs in [129].

Another MLI-based UPQC was proposed in [140], and the proposed configuration is shown in Fig. 44. It consists of two identical MLIs, being connected in back-to-back assembly. Each inverter requires twenty-four switches and three floating capacitors for producing five levels. Two capacitors C_1 and C_2 are used for constructing a DC-link with a middle point called M. As compared to the introduced diode-clamped UPQC in [136], the proposed UPQC configuration saves 36 diodes, but needs eight capacitors instead of four. Although both UPQC configurations require the same switch count, the total standing voltage of switches in [140] is higher than that in [136]. Further, both must use a sophisticated control for balancing capacitors voltage at specific values.

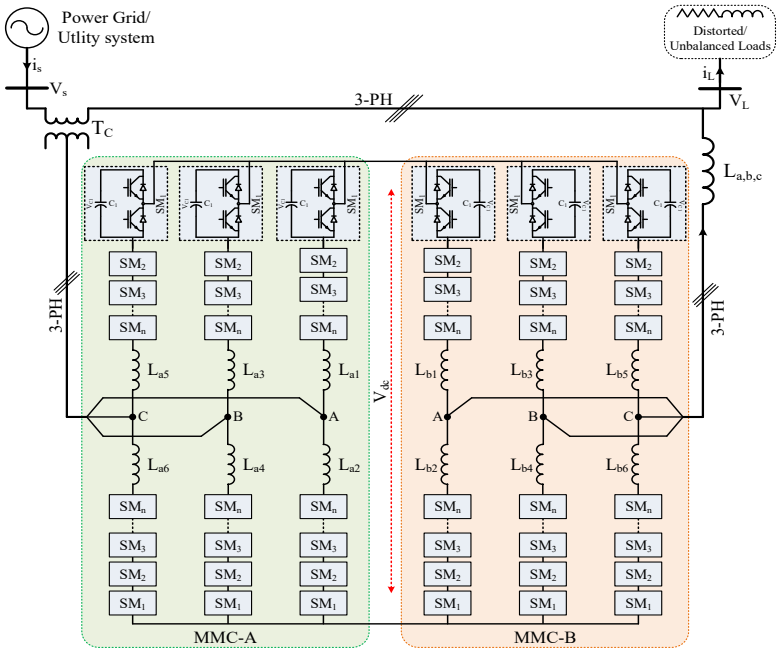


Fig. 43 Configuration of MMC-based UPQC in [137-139].

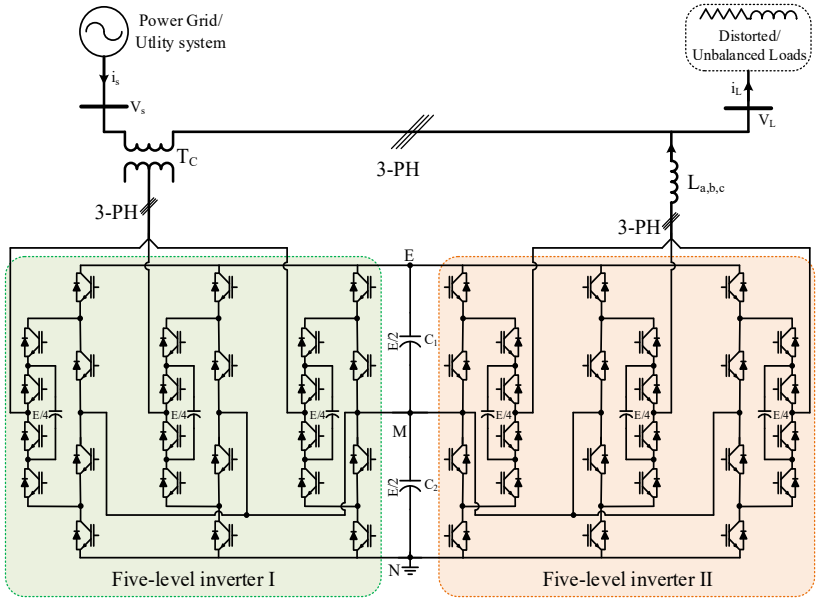


Fig. 44 Configuration of UPQC implemented by the back-to-back connection of two five-level inverters [140].

III. THE PROPOSED BENCHMARK FOR COMPARING MULTILEVEL INVERTER TOPOLOGIES

A. EXISTING FACTORS FOR COMPARING MULTILEVEL TOPOLOGIES

Over the past few years, several MLI topologies have been proposed for improving the power conversion efficiency, system reliability, power quality in several applications. The significant number and diversity of the proposed topologies allow the customers to select the suitable one to their needs, but selecting the best one is always a challenge. Different aspects and aims are set in a design process, for example, low semiconductors count, low passive elements, isolation features, boosting abilities, modularity, etc. To make the comparative process easier and more efficient for both industry and academia, two strategies have been presented in [34, 35]. The strategy in [34] is based on the level-number per switch ratio (LSR) for comparing different MLIs. As described in (1), the *LSR* is calculated by the number of levels N over the switch count (N_{SW}), indicating number of levels generated by each switch. Accordingly, topologies with higher *LSR* are better than those with a lower one from the switch count point of view.

$$LSR = \frac{N}{N_{SW}} \tag{1}$$

LSR cannot figure out other component counts, e.g. capacitors (N_C), inductors (N_L), diodes (N_D), transformers (N_{Trf}), DC sources (N_{DC}), and other components (N_X). To overcome this drawback, the component per level factor (CLF) was proposed in [35] as a comparative factor. Instead of counting only switches, *CLF* is to count all the used components for producing one level, as calculated in (2). Therefore, it can be used to compare MLI topologies by the total component count. A reduced component circuit has a lower *CLF*.

$$CLF = \frac{N_C + N_D + N_L + N_{SW} + N_{DC} + N_{TRF} + N_X}{N} \tag{2}$$

The proposed MLI topologies in [36-56, 58-83, 85, 86, 92, 95-97, 101-104, 107, 109-116, 141-156] are compared together by using the two comparative factors *LSR* and *CLF* in terms of component count. The compared MLIs in this work are named from *T*1 to *T*120, in which the same reference can be seen in different categories because some authors have proposed two or more configurations in one publication. Tables I and II show comparisons for single-phase MLI topologies of single/symmetrical and asymmetrical DC sources in literature while the three-phase MLIs are compared and summarized in Tables III and IV. The presented topologies were very diverse, in which some of them can generate N levels while the others were designed for a specific voltage level number. Therefore, to make a fair comparison, they are grouped based on the number of levels, for example, group A represents five-level topologies that use either symmetrical or single DC sources. The last row of each group highlights a topology that has the least component count. In the comparison, several aspects are adopted/assumed: each battery or PV string is counted as one DC source, and each winding of a coupled

TABLE I
COMPONENT REQUIREMENT FOR SINGLE-PHASE MULTILEVEL INVERTERS IN [36-47, 49, 51-56, 59, 61-63, 65-67, 70-73, 75, 77, 80, 81, 83, 85, 86, 102, 141, 142]

	Topology	In	N	N_{DC}	N_{SW}	N_{D}	N_{L}	N_{Cap}	N_{Trf}	N_{Total}	*LSR*	*CLF*
Group A	T120	[85]	5	1	8	6	4	4	0	23	0.63	4.60
	T38	[37]	5	2	8	4	2	3	0	19	0.63	3.80
	T119	[86]	5	1	8	3	2	4	0	18	0.63	3.60
	T48	[70]	5	1	12	0	0	4	0	17	0.42	3.40
	T59	[77]	5	1	10	0	0	4	0	15	0.50	3.00
	T34	[39]	5	2	4	4	2	2	0	14	1.25	2.80
	T37	[38]	5	2	4	4	2	2	0	14	1.25	2.80
	T54	[36]	5	1	6	3	1	2	0	13	0.83	2.60
	T47	[75]	5	1	6	2	0	3	0	12	0.83	2.40
	T52	[71]	5	2	8	0	0	2	0	12	0.63	2.40
	T43[a]	[65]	5	2	7	2	0	0	0	11	0.71	2.20
	T51	[72]	5	1	6	0	0	3	0	10	0.83	2.00
Group B	T49	[73]	7	1	16	0	0	3	0	20	0.43	2.85
	T58	[59]	7	1	8	4	0	3	0	16	0.88	2.29
	T30	[66]	7	1	7	2	0	3	0	13	1.00	1.86
	T45	[67]	7	3	10	0	0	0	0	13	0.70	1.86
	T65	[141]	7	1	8	0	0	4	0	13	0.88	1.86
	T110	[83]	7	1	9	0	0	3	0	13	0.78	1.86
	T24[a]	[62]	7	3	6	2	0	0	0	11	1.17	1.57
	T26[a]	[61]	7	3	8	0	0	0	0	11	0.88	1.57
	T46	[63]	7	3	7	1	0	0	0	11	1.00	1.57
Group C	T35	[39]	9	1	8	8	4	2	0	23	1.13	2.56
	T1	[43]	9	1	16	0	0	0	4	21	0.56	2.33
	T56	[56]	9	1	10	4	1	4	0	20	0.90	2.22
	T44[a]	[65]	9	4	9	4	0	0	0	17	1.00	1.89
	T110	[83]	9	1	12	0	0	4	0	17	0.75	1.89
	T33	[42]	9	1	12	0	0	3	0	16	0.75	1.78
	T36	[39]	9	1	6	4	2	2	0	15	1.50	1.67
	T17	[54]	9	1	8	0	0	2	4	15	1.13	1.67
	T40	[40]	9	2	10	0	2	0	0	14	0.90	1.56
	T41	[40]	9	2	10	0	2	0	0	14	0.90	1.56
	T42	[40]	9	2	10	0	2	0	0	14	0.90	1.56
	T53	[41]	9	1	10	0	0	3	0	14	0.90	1.56
	T55	[55]	9	1	9	2	0	2	0	14	1.00	1.56
	T2	[44]	9	1	10	0	0	3	0	14	0.90	1.56
	T3	[45]	9	1	10	0	0	3	0	14	0.90	1.56
	T111	[80]	9	4	10	0	0	0	0	14	0.90	1.56
	T25[a]	[62]	9	4	7	2	0	0	0	13	1.29	1.44

[a] Addressed for symmetrical mode alone, more details for their operation under asymmetrical mode (DC sources have asymmetrical values) can be found in [61, 62, 65]. Only number of levels will be changed while using same component count.

TABLE I
COMPONENT REQUIREMENT FOR SINGLE-PHASE MULTILEVEL INVERTERS IN [36-47, 49, 51-56, 59, 61-63, 65-67, 70-73, 75, 77, 80, 81, 83, 85, 86, 102, 141, 142] (Continued)

Group C (Continued)	T39	[40]	9	2	8	0	2	0	0	12	1.13	1.33
	T62	[102]	9	2	8	0	0	2	0	12	1.13	1.33
	T14	[52]	9	2	8	0	0	0	1	11	1.13	1.22
	T64	[142]	9	2	8	0	0	1	0	11	1.13	1.22
	T8	[49]	9	1	8	0	0	0	1	10	1.13	1.11
	T16	[53]	9	1	8	0	0	0	1	10	1.13	1.11
Group D	T117	[81]	15	1	26	0	0	7	0	34	0.58	2.27
	T46	[63]	15	7	13	3	0	0	0	23	1.15	1.53
	T5	[46]	15	1	8	0	0	2	3	14	1.88	0.93
	T13	[51]	15	1	8	0	0	0	2	11	1.88	0.73
Group E	T6	[47]	27	1	12	0	0	0	3	16	2.25	0.59
	T14	[52]	27	2	12	0	0	0	2	16	2.25	0.59
	T15	[52]	27	2	12	0	0	0	2	16	2.25	0.59

TABLE II
COMPONENT REQUIREMENT FOR ASYMMETRICAL SINGLE-PHASE MULTILEVEL INVERTERS IN [48, 50, 51, 58, 60, 64, 66, 68, 69, 74, 76, 78-80, 82, 102, 143]

	Topology	In	N	N_{DC}	N_{SW}	N_{D}	N_{L}	N_{Cap}	N_{Trf}	N_{Total}	*LSR*	*CLF*
Group F	T115	[74]	5	2	6	1	0	0	0	9	0.83	1.8
Group G	T61-a	[102]	7	2	8	0	0	2	0	12	0.88	1.71
	T4	[143]	7	2	8	0	0	0	0	10	0.88	1.43
Group H	T112	[68]	9	2	10	0	0	0	0	12	0.90	1.33
	T116	[82]	9	2	8	0	0	0	0	10	1.12	1.11
Group I	T63	[102]	13	4	16	0	0	4	0	24	0.81	1.85
	T61-a	[102]	13	2	14	0	0	5	0	21	0.93	1.62
	T19	[76]	13	4	10	0	0	0	0	14	1.30	1.08
Group J	T113	[69]	15	3	9	4	0	0	0	16	1.67	1.06
	T61-b	[102]	15	2	10	0	0	3	0	15	1.50	1.00
	T60	[143]	15	3	10	0	0	0	0	13	1.50	0.87
	T18	[79]	15	3	8	0	0	0	0	11	1.88	0.73
	T12	[51]	15	2	8	0	0	0	1	11	1.88	0.73
Group K	T22[a]	[60]	17	2	10	2	0	2	0	16	1.70	0.94
	T111	[80]	17	4	10	0	0	0	0	14	1.70	0.82
	T29	[64]	17	4	10	0	0	0	0	14	1.70	0.82
Group L	T61-b	[102]	19	2	12	0	0	4	0	18	1.58	0.95
	T7	[48]	19	2	10	2	0	0	2	16	1.90	0.84
	T9	[50]	19	2	12	0	0	0	2	16	1.58	0.84

[a]Addressed for asymmetrical mode alone, more details for their operation under symmetrical mode (DC sources have symmetrical values) can be found in [51, 60, 78]. Only number of levels will be changed while using same component count.

TABLE II
COMPONENT REQUIREMENT FOR ASYMMETRICAL SINGLE-PHASE MULTILEVEL INVERTERS IN [48, 50, 51, 58, 60, 64, 66, 68, 69, 74, 76, 78-80, 82, 102, 143] (Continued)

Group M	T61-a	[102]	23	2	24	0	0	10	0	36	0.96	1.57
	T31	[66]	23	2	13	3	0	5	0	23	1.77	1.00
	T61-b	[102]	23	2	14	0	0	5	0	21	1.64	0.91
Group N	T63	[102]	25	8	32	0	0	8	0	48	0.78	1.92
	T61-a	[102]	25	2	26	0	0	11	0	39	0.96	1.56
	T32[a]	[78]	25	4	10	8	0	0	0	22	2.50	0.88
Group O	T6-b	[102]	31	2	18	0	0	7	0	27	1.72	0.87
	T28	[64]	31	6	14	0	0	0	0	20	2.21	0.65
Group P	T63	[102]	49	16	64	0	0	16	0	96	0.77	1.96
	T23[a]	[60]	49	3	14	3	0	3	0	23	3.50	0.47
	T11[a]	[51]	49	2	12	0	0	0	2	16	4.08	0.33
	T116	[82]	49	4	12	0	0	0	0	16	4.08	0.33
Group Q	T63	[102]	55	18	72	0	0	18	0	108	0.76	1.96
	T21	[58]	55	3	44	0	0	7	0	54	1.25	0.98
	T61-b	[102]	55	2	30	0	0	13	0	45	1.83	0.82

[a]Addressed for asymmetrical mode alone, more details for their operation under symmetrical mode (DC sources have symmetrical values) can be found in [51, 60, 78]. Only number of levels will be changed while using same component count.

TABLE III
COMPONENTS REQUIREMENT FOR ASYMMETRICAL THREE-PHASE MULTILEVEL INVERTER TOPOLOGIES IN [102, 109-112, 114, 143, 149, 156]

	Topology	In	N	N_{DC}	N_{SW}	N_D	N_L	N_{Cap}	N_{Trf}	N_{Total}	*LSR*	*CLF*
Group R	T81	[112]	4	3	16	12	0	0	0	31	0.25	7.75
	T82	[114]	4	2	24	0	0	0	0	26	0.17	6.50
Group S	T80	[111]	7	6	18	24	0	0	0	48	0.39	6.86
	T86	[102]	7	6	24	0	0	6	0	36	0.29	5.14
	T74	[143]	7	6	24	0	0	0	0	30	0.29	4.29
Group T	T81	[112]	10	9	28	12	0	0	0	49	0.36	4.90
	T79	[110]	10	8	24	0	0	0	0	32	0.42	3.20
Group U	T80	[111]	11	8	24	48	0	0	0	80	0.46	7.27
	T88	[102]	11	6	24	0	0	6	0	36	0.46	3.27
Group V	T80	[111]	15	10	30	72	0	0	0	112	0.50	7.47
	T75	[143]	15	9	30	0	0	0	0	39	0.50	2.60
Group W	T81	[112]	17	16	42	12	0	0	0	70	0.40	4.12
	T89	[156]	17	6	36	0	0	9	0	51	0.47	3.00
Group X	T80	[111]	19	12	36	96	0	0	0	144	0.53	7.58
	T85	[109]	19	13	36	0	0	14	0	63	0.53	3.32
Group Y	T81	[112]	31	30	70	12	0	0	0	112	0.44	3.61
	T76	[143]	31	12	36	0	0	0	0	48	0.86	1.55
Group Z	T71	[149]	33	4	36	0	0	6	3	49	0.92	1.48
	T90	[149]	33	6	36	0	0	6	0	48	0.92	1.45

TABLE IV
COMPONENT REQUIREMENT FOR THREE-PHASE MULTILEVEL INVERTERS IN [39, 44, 45, 92, 95-97, 101-104, 107, 109, 110, 113, 115, 116, 141, 142, 144-148, 150-155]

	Topology	In	N	N_{DC}	N_{SW}	N_{D}	N_{L}	N_{Cap}	N_{Trf}	N_{Total}	*LSR*	*CLF*
	T94	[95]	3	2	14	10	2	2	0	30	0.21	10.00
	T103	[96]	3	1	12	2	4	4	0	23	0.25	7.67
	T107	[150]	3	1	14	4	1	2	0	22	0.21	7.33
Group	T93	[107]	3	1	16	0	0	4	0	21	0.19	7.00
A1	T104	[97]	3	1	12	3	1	4	0	21	0.25	7.00
	T114	[116]	4[a]	1	12	24	0	3	0	40	0.58	5.71
	T118	[92]	3	1	12	0	0	2	0	15	0.25	5.00
	T96	[115]	3	2	12	0	0	0	0	14	0.25	4.67
	T97	[103]	5	2	24	6	0	9	0	41	0.21	8.20
	T108	[151]	5	1	21	12	0	5	0	39	0.24	7.80
	T77	[39]	5	2	12	12	6	2	0	34	0.42	6.80
	T99	[154]	5	2	20	6	0	2	0	30	0.25	6.00
Group	T69	[147]	5	2	24	0	0	0	3	26	0.21	5.80
B1	T100	[154]	5	2	20	0	0	2	0	24	0.25	4.80
	T105	[152]	5	1	18	0	0	4	0	23	0.28	4.60
	T67	[144]	5	1	16	0	0	2	2	19	0.31	4.20
	T109	[153]	5	1	15	0	0	3	0	19	0.33	3.80
	T66	[145]	5	1	12	0	0	2	2	15	0.42	3.40
Group	T78	[110]	6	8	24	0	0	0	0	32	0.25	5.33
C1	T102	[104]	6	1	24	0	0	6	0	31	0.25	5.17
Group	T98	[155]	7	2	36	0	0	9	0	47	0.19	6.71
D1	T106	[141]	7	1	24	0	0	8	0	33	0.29	4.71
	T91	[113]	9	2	42	0	0	9	0	53	0.21	5.89
	T95	[101]	9	3	36	0	0	12	0	51	0.25	5.67
	T72	[44]	9	1	30	0	0	9	3	40	0.30	4.78
Group	T73	[45]	9	1	30	0	0	9	3	40	0.30	4.78
E1	T83	[109]	9	7	24	0	0	8	0	39	0.38	4.33
	T101	[142]	9	6	24	0	0	9	0	39	0.38	4.33
	T87	[102]	9	6	24	0	0	6	0	36	0.38	4.00
	T70	[148]	9	2	16	0	0	0	6	18	0.56	2.67
Group	T78	[110]	15	26	60	0	0	0	0	86	0.25	5.73
F1	T84	[109]	15	13	36	0	0	14	0	63	0.42	4.20
Group	T84	[109]	21	19	48	0	0	20	0	87	0.44	4.14
G1	T68	[146]	21	1	48	0	0	0	12	49	0.44	2.90
Group	T69	[147]	49	24	156	0	0	0	3	180	0.31	3.73
H1	T92	[113]	49	3	84	6	0	18	0	111	0.58	2.27

[a] It can generate four levels, so it is inserted in the closest group, i.e. 3-level inverters group.

inductor is considered one inductor, input and output filter components are discounted, a three-phase transformer is calculated as three single-phase transformers and the same for multi-winding/secondary transformers cases. The unidirectional switch is considered as the base for counting the switch number, so bidirectional ones are disassembled into their primary components.

Based on Tables I-IV, the drawbacks of using *LSR* for comparing MLIs have been solved by *CLF*. However, important factors like component ratings have been ignored when computing *CLF* values for the compared circuits since the *CLF* alone is not able to compare the used components in term of ratings. One device with a voltage rating of 10*E* has been equally counted as a device with the voltage rating of 0.5*E*. Consequently, a new indicator or method for comparing MLI topologies more accurately is very important for both industry and academia to select the best circuit in term of the component count.

B. THE PROPOSED COMPARATIVE FACTOR: COMPONENT FOR EACH LEVEL (CEL)

In this section, a new method is proposed to compare MLI topologies. First, the MLI components are subdivided into two groups: semiconductors and passive elements. The semiconductor group includes switches and diodes while capacitors, inductors, and transformers are classified as passive elements. Second, for simplicity, the peak current passing through each component is assumed to be the same and equal to the load current. Further, the peak voltage (VPK) is considered as an indicator for the rating of the component.

For calculating the equivalent semiconductor count NE_{SEMI}, the total standing voltage (TSV_{SEMI}) for NE_{SEMI} elements is calculated as in (3). Afterwards, NE_{SEMI} is defined by TSV_{SEMI} and the base value of the voltage (V_{BASE}) in (4). For the passive elements, several parameters, such as capacitance, inductance, equivalent resistance, are used in the evaluation. Each topology has different specifications based on input/output waveforms or depending on facility conditions of research groups. In the proposed comparative strategy, the voltage is a dominant factor as the current has been assumed equal to the load current. The equivalent numbers of capacitors NE_{C}, inductors NE_{L}, transformers NE_{Trf}, and DC sources NE_{DC} are calculated by (5)-(8), respectively. For example, if topology T_{X} requires two DC sources of E and $2E$ volt, the number of DC sources N_{DC} is 2, while the equivalent number NE_{DC} is equal to three ($NE_{\mathrm{DC}}=(E+2E)/E$). The same rule can be applied for the rest of the used components. The total equivalent component count NE_{Total} and *CEL* are defined by (9) and (10), respectively.

$$TSV_{\mathrm{SEMI}} = \sum_{i=1}^{N_{\mathrm{SEMI}}} VPK_{\mathrm{i}} \tag{3}$$

$$NE_{\mathrm{SEMI}} = \frac{TSV_{\mathrm{SEMI}}}{V_{\mathrm{BASE}}} \tag{4}$$

$$NE_{\mathrm{C}} = \frac{\sum_{i=1}^{N_{\mathrm{C}}} VPK_{\mathrm{i}}}{V_{\mathrm{BASE}}} \tag{5}$$

$$NE_{\mathrm{L}} = \frac{\sum_{i=1}^{N_{\mathrm{L}}} VPK_{\mathrm{i}}}{V_{\mathrm{BASE}}} \tag{6}$$

$$NE_{\mathrm{TRF}} = \frac{\sum_{i=1}^{N_{\mathrm{TRF}}} VPK_{\mathrm{i}}}{V_{\mathrm{BASE}}} \tag{7}$$

$$NE_{\mathrm{DC}} = \frac{\sum_{i=1}^{N_{\mathrm{DC}}} VPK_{\mathrm{i}}}{V_{\mathrm{BASE}}} \tag{8}$$

$$NE_{\mathrm{TOTAL}} = NE_{\mathrm{SEMI}} + NE_{C} + NE_{L} + NE_{TRF} + NE_{DC} \tag{9}$$

$$CEL = \frac{NE_{\mathrm{TOTAL}}}{N} \tag{10}$$

The passive elements in the MLI topologies, such as capacitors and inductors, have distinctive natures as compared to other components since they store energy either in magnetic or electric fields. An additional comparative factor, namely stored energy factor (SEF), is proposed to take their stored energy (SE) into consideration when comparing topologies beside their equivalent numbers. The total stored energy (TE) of stored energy elements (N_{SE}) is calculated in (11) and used to obtain the proposed *SEF* in (12).

$$TE = \sum_{i=1}^{N_{\mathrm{SE}}} SE_{\mathrm{i}} \tag{11}$$

$$SEF = \frac{TE}{TE_{\mathrm{BASE}}} \tag{12}$$

where SE_{i} is the stored energy on a passive element i in a topology. TE_{BASE} is the total stored energy base value. The value of the TE_{BASE} can be the total stored energy of an interested or proposed topology.

The *SEF* can be calculated for different stored energy elements in a compared topology *T*x, indicating the stored energy in a percentage. *SEF* should be accompanied to the equivalent counts of the stored energy elements (i.e. NE_{C} and NE_{L}) when comparing *T*x with other topologies. These factors allow for a fairer comparison of topologies that contain stored energy elements. For example, two

MLI topologies (T_A and T_B) use capacitors. T_A has two capacitors of 1 mF and voltage rating of 100 V, while T_B has three capacitors, (two of 0.25 mF and one of 0.5 mF) and all of the capacitors have voltage rating of 75 V. The equivalent count of the capacitor is defined by (5), and their *SEFs* are calculated by (11) and (12). The equivalent capacitor counts of T_A and T_B are 2 and 2.25, respectively (V_{BASE} is selected at 100 V). The *SEFs* of T_A and T_B are 1 and 0.28 , respectively (TE for T_A is "2*0.5 *1e^{-3}*100^2" and for T_B is "(2*0.5*0.25e^{-3}*75^2) + (0.5*0.5e^{-3}*75^2)", TE_{BASE} is selected to be T_A stored energy). Accordingly, T_A has a less equivalent count of capacitors (2 instead of 2.25) as compared to T_B, but T_B has a lower *SEF* (0.28 instead of 1). Although the topology T_B requires a higher equivalent capacitor count, the capacitors store 28.1% of the stored energy in T_A, affecting the cost and size of the capacitors. It is worth mentioning that the same procedure can be applied to inductors as well.

To verify the effectiveness of the proposed factor *CEL* over the existing factor in ranking MLIs in term of component counts, five-level topologies *T*99, *T*100, CHB, NPC, and FC are selected in a comparative study as shown in Table V. CHB, NPC, and FC are the conventional MLIs, while *T*99 and *T*100 are novel MLI topologies in [154]. A fair comparison among the selected topologies can be achieved because both number and value of the output voltage levels are the same for all of them (i.e. five levels of -0.25*E*, -0.5*E*, 0, 0.25*E*, and 0.5*E* volt). Table V also shows the voltage rating/stress for all components in the case-study topologies.

Topology *T*99 shown in Fig. 45 is selected as an example to clarify the *CEL* calculation. It consists of two DC sources, twenty switches, two capacitors, and six diodes. It requires eight switches with a voltage rating of 0.25*E* and twelve switches with 0.5*E*, in addition to six diodes with a rating of 0.5*E* and two 0.25*E* capacitors. It does not have any transformers or inductors. For calculating the equivalent semiconductor count, NE_{SEMI}, first (3) is used for obtaining TSV_{SEMI} value, and then (4) is used to define NE_{SEMI}. TSV_{SEMI} is 11*E* (= 8*0.25*E*+12*0.5*E*+6*0.5*E*), so the value of NE_{SEMI} is 11. Using (5) and (8), NE_C and NE_{DC} can be calculated as ((0.25*E*+025*E*)/*E*) and ((0.5*E*+05*E*)/*E*), respectively. Using (9) and the obtained values of NE_{SEMI}, NE_{DC} and NE_C, results in the total component count of 12.5. Finally, *CEL* is calculated by using (10) to be 2.5. For the *T*100, CHB, and FC, the same procedure can be repeated.

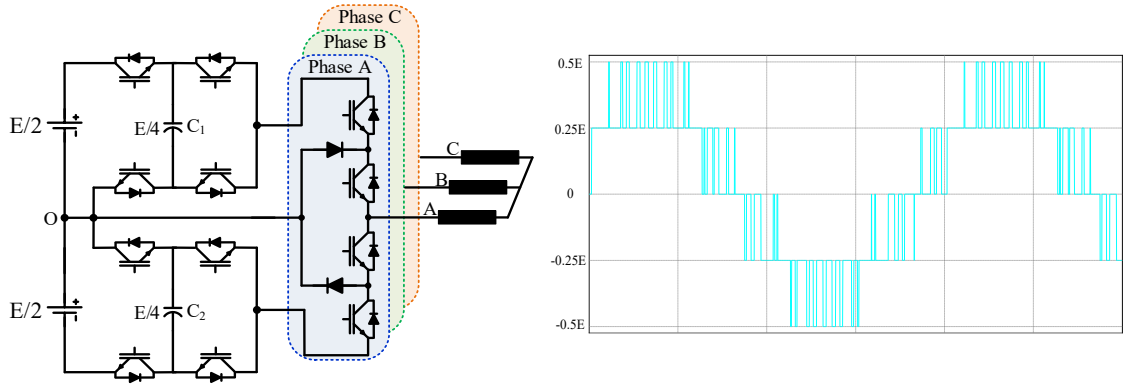
In Table V, the differences between the existing method and the proposed one can be well observed. For example, in T99, the *CLF* factor results in the total component count N_{Total} of 30 regardless of their voltage rating while NE_{Total} is only 12.5 when using *CEL* factor. Without considering the component voltage rating or based on *CLF* values alone, the CHB requires more components than those in T100 since its *CLF* is higher than that of *T*100. However, when considering the voltage rating by the proposed indicator *CEL*, the total equivalent component count of the CHB is lower than that of *T*100 since the *CEL* of CHB is smaller than that of *T*100.

As mentioned before, in addition to the equivalent numbers of the used components in each topology to find *CEL* values, the stored energy factor (SEF) is recommended for a better description of stored energy elements in the compared topologies. Table VI lists the total energy TE and *SEF* for each topology based on

(11) and (12). It is worth noting that the listed *SEFs* are a function of the utilised capacitors in the circuits, and not given as numerical values. Obtaining the numerical values requires detailed parameters of rated power, operating voltage, switching frequency, and voltage ripple, etc. It is important to consider all parameters that affect the stored energy element selection during the design process, when using *SEF* for obtaining a fairer comparison.

TABLE V
USING CLF AND CEL FOR COMPARING THE FIVE-LEVEL INVERTERS IN [154] AND THE THREE BASIC MLI TOPOLOGIES

Topology	DC sources			Switching devices			Diodes			Capacitors			Existing method		Proposed method	
	E/4	E/2	E	E/4	E/2	E	E/4	E/2	3E/4	E/4	E/2	3E/4	N_{Total}	CLF	NE_{Total}	CEL
T99	0	2	0	8	12	0	0	6	0	2	0	0	30	6	12.5	2.5
T100	0	2	0	8	6	6	0	0	0	2	0	0	24	4.8	12.5	2.5
CHB	6	0	0	24	0	0	0	0	0	0	0	0	30	6	7.5	1.5
NPC	0	0	1	24	0	0	6	6	6	4	0	0	47	9.4	17	3.4
FC	0	0	1	24	0	0	0	0	0	7	3	3	38	7.6	12.5	2.5



(a) (b)

Fig. 45 Five-level three-phase topology *T*99 [154]. (a) Circuit configuration. (b) Output pole voltage for the compared MLI circuits in Table V.

The comparison suggests that each topology should be evaluated by some of these factors, i.e. NE_{SEMI}, NE_{DC}, NE_{C}, NE_{L}, NE_{Trf}, *SEF*, and *CEL*, to highlight its merits, allowing for finding the most suitable application. For example, in PV farms, NE_{DC} is less important than that in motor drives while NE_{C}, NE_{L}, NE_{Trf}, and *SEF* should be reduced for more compact designs. For control simplicity, NE_{SEMI} and NE_{C} have the salient effects as compared to other factors. Finally, the *CEL* factor is the most important for having a reduced component count regardless of distinct features in each topology.

TABLE VI
CALCULATION OF THE STORED ENERGY FACTOR FOR THE FIVE-LEVEL INVERTERS IN [154] AND THE THREE BASIC MLI TOPOLOGIES

Topology	Capacitors[a]			Stored energy factor calculation		
	E/4	E/2	3E/4	TE_{BASE}	TE	SEF
T99	2	0	0	$E^2/32\ (C_{A1}+C_{A2})$	$E^2/32\ (C_{A1}+C_{A2})$	1
T100	2	0	0	$E^2/32\ (C_{A1}+C_{A2})$	$E^2/32\ (C_{B1}+C_{B2})$	$(C_{B1}+C_{B2})/(C_{A1}+C_{A2})$
CHB	0	0	0	$E^2/32\ (C_{A1}+C_{A2})$	0	0
NPC	4	0	0	$E^2/32\ (C_{A1}+C_{A2})$	$E^2/32\ \sum_{i=1}^{4} C_{Ci}$	$\sum_{i=1}^{4} C_{Ci}\ /(C_{A1}+C_{A2})$
FC	7	3	3	$E^2/32\ (C_{A1}+C_{A2})$	$0.4375E^2 \sum_{i=1}^{13} C_{Di}$	$14 \sum_{i=1}^{13} C_{Di}\ /(C_{A1}+C_{A2})$

[a] C_{A1} and C_{A2} are the capacitors in T_{99}. C_{B1} and C_{B2} are the capacitors in T_{100}. C_{C1}, C_{C2}, C_{C3}, and C_{C4} are the capacitors in NPC. C_{D1}, C_{D2},….. C_{D12}, and C_{D13} are the capacitors in FC.

IV. CONCLUSION

This paper presented a review study for the recently developed topologies in terms of construction, salient features and limitations, giving guidelines to further improve the current multilevel topologies more efficiently and compactly. A detailed comparison in terms of switch, diode, capacitor, inductor, transformer count was performed and systematically summarized in tables. New comparative factors - component for each level (CEL) and stored energy factor (SEF) were introduced to compare MLI topologies more effectively. A comparative study was presented to verify the usefulness of the proposed factors for comparing multilevel inverters, making it easier in evaluating newer topologies in the future.

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Paper II:

Four-Level Three-Phase Inverter with Reduced Component Count for Low and Medium Voltage Applications

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Four-Level Three-Phase Inverter with Reduced Component Count for Low and Medium Voltage Applications

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***Abstract*—This paper proposes a novel three-phase topology with a reduced component count for low- and medium-voltage systems. It requires three bidirectional switches and twelve unidirectional switches for producing four-level voltages without using flying capacitors or clamping diodes, reducing the size, cost, and losses. Removing flying capacitors and clamping diodes allows it to simplify control algorithms and increase the reliability, efficiency, and lifetime. A modified low-frequency modulation (LFM) scheme is developed and implemented on the proposed topology to produce a staircase voltage with four steps. Further, a level-shifted pulse width modulation (LSPWM) is used to reduce the filter size and increase the output voltage controllability. In this study, a voltage balancing control algorithm is executed to balance the DC-link capacitor voltages. The performance of the proposed topology is numerically demonstrated and experimentally validated on an in-house test setup. Within the framework, the power loss distribution in switches and conversion efficiency of the proposed circuit are studied, and its main features are highlighted through a comparative study.**

Index Terms—DC-AC converters, four-level inverters, low and medium voltage applications, multilevel inverters, three-phase inverters.

I. INTRODUCTION

Multilevel inverters (MLIs) have gained popularity in DC-AC converters, with a wide range of voltage levels, due to their attractive features of low harmonic contents, low dv/dt voltage stress, low filtering requirements, low switching frequency, and using low-rated semiconductor devices. Further, some MLIs have a modularity feature, enabling transformerless operation and increasing the reachable output voltage without increasing the semiconductor device rating [1-5]. These unique features make the MLIs remarkable among other DC-AC converters. The cascaded H-bridge MLI (CHB-MLI) [6], neutral-point clamped MLI (NPC-MLI) [7, 8], and flying capacitor MLI (FC-MLI) [9, 10] are considered as the baseline topologies of MLIs. On the other hand, producing a higher count of voltage levels dramatically increases the counts of clamping diodes, flying capacitors, and isolated DC sources in NPC-MLI, FC-MLI, and CHB-MLI, respectively, raising the inverter footprint and cost [11]. Further, in NPC-MLI and FC-MLI, enlarging level count renders extra challenges of balancing the capacitor voltages, increasing switching frequency, sensor count and control complexity, reducing the inverter reliability and lifetime [12]. To address those shortcomings of the conventional MLIs, many MLIs have been intensively introduced with a focus on a high-level count or specific

applications [12-28]. However, only few publications [20-28] aim to develop four-level MLIs for low- and medium-voltage three-phase systems, which are briefly discussed hereafter and detailed in [20-28].

The authors in [20] introduced an eighteen-step inverter (EI) topology, generating four voltage levels by using twelve switches, twenty-four diodes, three DC-link capacitors, and one DC source. As compared to most four-level topologies, the EI topology requires fewer active switches and does not need any flying capacitor. However, it suffers from using a high count of clamping diodes and high-voltage rating of the semiconductor devices (e.g. when applying a DC-link voltage of 3*E*, six switches block 3*E*, six switches block 2*E*, twelve diodes withstand for 2*E* and twelve diodes subject to *E*). To mitigate the drawbacks of EI topology, a four-level nested neutral-point-clamped (NNPC) was presented in [21], combining the FC-MLI and NPC-MLI. It consists of eighteen switches, six clamping diodes, six flying capacitors, two DC-link capacitors and one DC source. It reduces the clamping diodes count to only six instead of twenty-four diodes in the EI, but the numbers of the flying capacitors and switches are increased to six capacitors and eighteen switches, respectively. Although the NNPC has a lower count of diodes and DC-link capacitors than the EI circuit, it must use higher flying capacitor and switch counts, increasing the size, cost, and control requirements. However, its salient features include the low total standing voltage of the switches, and using switches of equal rating, attracting more investigations to mitigate its shortcomings [29, 30].

A hybrid π-type topology was reported in [22], eliminating clamping diodes in both EI and NNPC. However, the hybrid π-type requires an addition of twelve switches and three flying capacitors as compared to the EI circuit, or needs six additional switches while saving three flying capacitors as compared to the NNPC. Despite removing clamping diodes, the hybrid π-type topology still has a high count of switches (twenty-four) besides using three flying capacitors, increasing its cost and size. Alternatively, a four-level active neutral-point clamped (4L-ANPC) topology was reported in [23] to eliminate flying capacitors in the hybrid π-type inverter while using the same switch count. It consists of twenty-four switches, three DC-link capacitors, and single DC source. It is worth mentioning that the switch count can be reduced to eighteen instead of twenty-four by replacing twelve switches with only six switches at the double voltage rating.

The authors in [24-26] presented a nested T-type (NT-type) MLI, consisting of six switches and two flying capacitors per each inverter leg. The three inverter legs share the same DC-link, which is formed by a single DC source without using DC-link capacitors. The NT-type MLI can be used as a solution to deal with the high switch count of the hybrid π-type topology in [22] while keeping the diode-free feature of the hybrid π-type against EI and NNPC circuits. The switch count is reduced to eighteen instead of twenty-four while the DC-link capacitors are eliminated. These benefits came with the cost of using six flying capacitors instead of three in the hybrid π-type circuit, increasing the control complexity and decreasing the lifetime.

To solve the drawbacks of using flying capacitors in the NT-type inverter while preserving the reduced switch count and removing clamping diodes, the authors in [27, 28] presented the dual T-type (DT-type) and π-type MLIs. The DT-type

topology in [27] uses eighteen switches, three DC-link capacitors and one DC source. The eighteen switches are configured in a way to build six T-type legs, being connected back-to-back through three bidirectional switches. Similarly, the π-type inverter in [28] uses the same counts of switches, DC sources, and DC-link capacitors. Both two circuits can eliminate flying capacitors and clamping diodes, being considered as their main merits. However, they still suffer from a high-voltage stress of the full DC-link voltage applied on six switches out of eighteen switches, restricting the reachable output voltage and increasing the switching losses.

To tackle the limitations of the aforementioned MLI topologies, namely high counts of flying capacitors, diodes, switches, and DC sources, this paper proposes a novel three-phase four-level topology with a reduced component count to mitigate those problems in low and medium voltage systems. The proposed topology does not need any clamping diode or flying capacitor and uses only eighteen switches for producing same 4-level voltages, resulting in a compact design, and increasing efficiency and lifetime. Section II introduces the proposed topology, including its circuit description and operation principles. The two switching schemes based on low-frequency and level-shifted pulse width modulations are presented in Section III. Section IV presents a voltage balance control for the DC-link capacitors. Section V provides simulation results and experimental validations. Afterwards, the efficiency of the proposed topology is analysed and highlighted in Section VI. The effectiveness of the proposed topology is proven through a comparative study between the proposed topology and other four-level MLIs in Section VII. Finally, the paper is concluded in Section VIII.

II. PROPOSED TOPOLOGY

Fig. 1 shows the proposed topology, consisting of twelve unidirectional switches (S_1-S_{12}) and three bidirectional switches (B_1-B_3). It does not use any power diode or flying capacitor, reducing control algorithms complexity, power loss and increasing the inverter lifetime. To simplify the gate-drive circuits, the common-emitter structure is adopted to configure the bidirectional switches. Further, the three-phase legs share the same DC-link, reducing the counts of DC sources and DC-link capacitors. Depending on the availability of the DC sources or applications, the DC-link of the proposed topology can be configured in two ways: either using three low-voltage DC sources or single medium-voltage DC source linked to three DC-link capacitors as shown in Figs. 1 (a) and (b), respectively. Renewable energy systems based on PVs and fuel cells (FCs) have multiple DC sources, thus the first configuration is recommended to be used in those energy systems. Accordingly, DC-link capacitors and their associated control algorithms can be eliminated. However, power electronic conditioner circuits are needed to control/maximize the raw generated power from those renewable energy sources. On the other hand, the second configuration or single source configuration (SSC) in Fig. 1(b) is recommended for industrial applications, where a single medium-voltage bus is available. Both configurations are detailed in this paper.

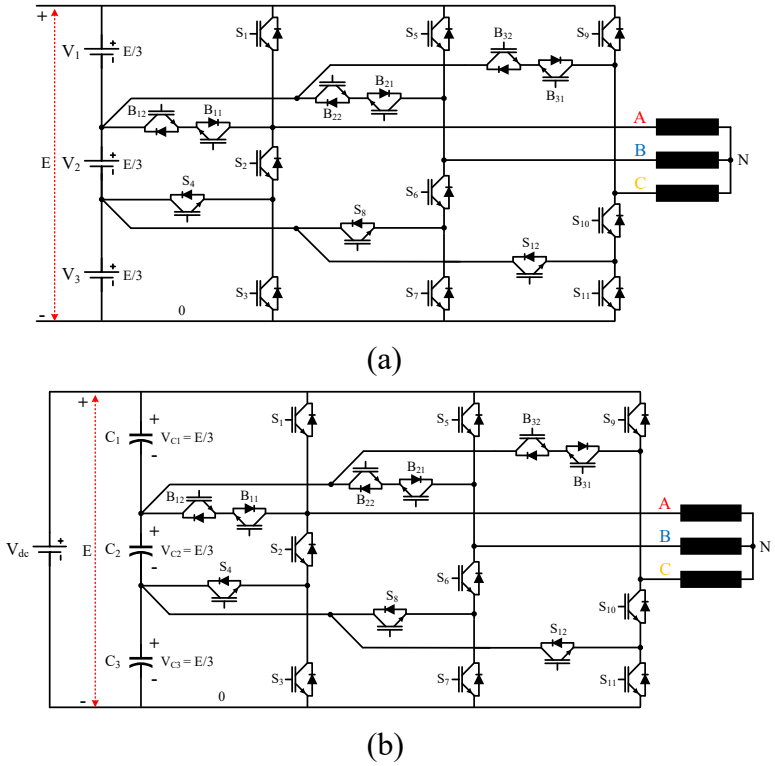


Fig. 1 The proposed four-level topology. (a) Multiple sources configuration (MSC), recommended for energy systems, (b) Single source configuration (SSC), recommended for industrial applications.

The inverter switches are controlled to produce four unipolar voltage levels of 0, $E/3$, $2E/3$, and E in the pole voltages V_{A0}, V_{B0}, and V_{C0}. Seven-level bipolar voltages can be generated in the line voltages V_{AB}, V_{BC}, and V_{CA} by subtracting the adjacent pole voltages. For example, V_{AB} is synthesized by subtracting V_{A0} from V_{B0}, producing a seven-level voltage of $-E$, $-2E/3$, $-E/3$, 0, $E/3$, $2E/3$, and E. The operating modes of the proposed topology are illustrated in Fig. 2, showing the switching states for producing seven voltage levels in the line voltage V_{AB}. Each state is accompanied by its corresponding paths for the positive and negative currents. For example in Fig. 2(a), the state I shows that the switches S_1, S_6, and S_7 must be in ON-state to obtain the maximum positive voltage of E in the line voltage V_{AB} while switches (S_2-S_4), (S_5, S_8) and (B_1, B_2) are in OFF-state. The positive and negative currents are highlighted in blue and red dash lines, respectively. Similarly, switching states from II to VIII in Fig. 2 explain the different switching modes of the proposed topology for producing the remaining voltage levels. It should be noted that some switching states are removed when forming these switching paths, preventing the short-circuit faults in the inverter. For example, in leg A, the switching combinations of (S_1, S_2, S_4), (S_1, S_2, S_3), (S_3, S_4), (S_1, B_1), and (B_1, S_2, S_4) are marked as unused states in both switching algorithms.

III. Modulation Strategies

Two modulation strategies are utilized in this section to control the output voltage of the proposed topology. The low-frequency modulation (LFM) is adopted for reducing the switching loss, while the level-shifted pulse width

modulation (LSPWM) is implemented for increasing the controllability of the output voltage. Both switching strategies follow the provided switching states in Table I to create the switching pulses for the proposed inverter. Table I shows the switching pattern of switches (S_1-S_4) and B_1 for producing four levels in the pole voltage V_{A0}.

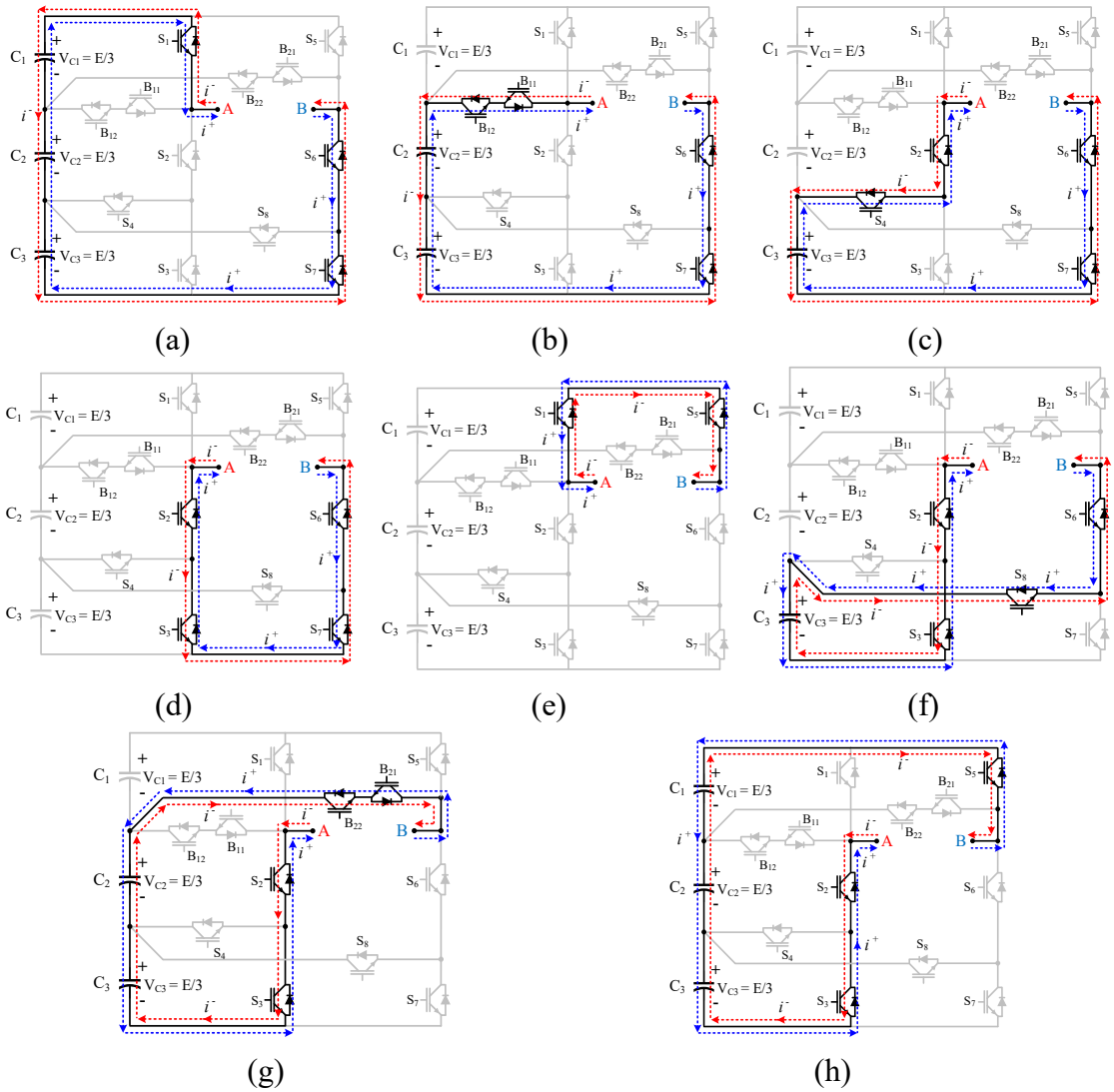


Fig. 2 Switching states of the proposed topology: (a) State I: V_{AB}= E, (b) State II: V_{AB}= 2E/3, (c) State III: V_{AB}= E/3, (d) State IV: V_{AB}= 0, (e) State V: V_{AB}= 0, (f) State VI: V_{AB}= -E/3, (g) State VII: V_{AB}= -2E/3, (h) State VIII: V_{AB}= -E.

TABLE I
SWITCHING STATES FOR PRODUCING FOUR VOLTAGE LEVELS IN POLE VOLTAGE V_{A0}

State	V_{A0}	S_1	S_2	S_3	S_4	B_1
A	E	ON	OFF	OFF	OFF	OFF
B	2E/3	OFF	OFF	OFF	OFF	ON
C	E/3	OFF	ON	OFF	ON	OFF
D	0	OFF	ON	ON	OFF	OFF

Fig. 3 shows the LFM switching pattern accompanied by the pole voltage V_{A0}. In the LFM scheme, three sinusoidal reference signals (only SR_A is shown in Fig. 3) and two modulator signals (H^+ and H^-) are used for generating three controlling signals (M_1-M_3). For instance, M_1 and M_2 are produced by comparing the SR_A signal with H^+ and H^-, respectively, while comparing the SR_A signal with zero produces the M_3 controlling signal. Simple logical operators summarized in (1)-(5) are applied on the three controlling signals M_1-M_3 for producing five switching signals of switches S_1-S_4 and B_1 in leg A. Similarly, switching signals for the switches in legs B and C can be generated. Both sinusoidal and modulator signals can be varied in their magnitude from 0 to 1, providing two degrees of freedom for producing voltages at different RMS, level counts, and THDs. For example, selecting a magnitude value of 1 for the three sinusoidal signals and ±0.35 for H modulators can produce seven-level line voltages with THD of 11. 81%. On the other hand, five-level line voltages with the THD of 34.88% are produced when H modulators are equal to ±0.9.

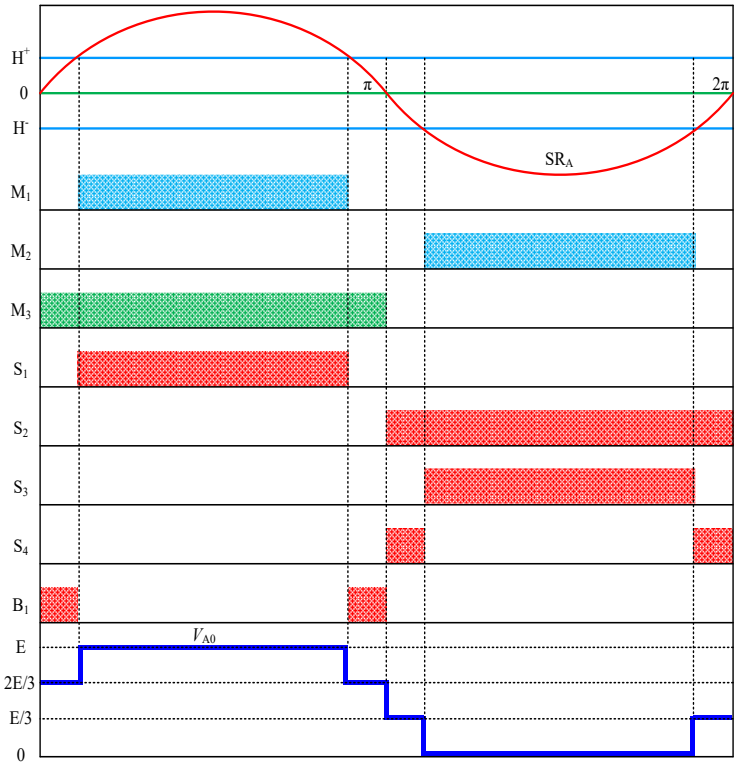


Fig. 3 Switching pattern and pole voltage under the LFM scheme (leg A).

$$S_1 = M_1 \tag{1}$$

$$S_2 = \overline{M_3} \tag{2}$$

$$S_3 = M_2 \tag{3}$$

$$S_4 = \overline{M_2} \times \overline{M_3} \tag{4}$$

$$B_1 = \overline{M_1} \times M_3 \tag{5}$$

Although the controllability of the applied LFM is better than the conventional LFM, it is still not as smooth as the other switching schemes based on sinusoidal pulse width modulation. Therefore, the LSPWM scheme is also utilized for producing the switching signals of the proposed topology. The LSPWM requires three carrier signals and three sinusoidal modulation signals to produce the switching pulses for the switches in the proposed inverter. The carrier signals have a fixed amplitude of V_{cr} and are shifted in level by V_{cr} while the three sinusoidal signals are shifted in phase by 120° and their magnitude can be varied from 0 to $1.5V_{cr}$. Fig. 4 shows the generation process of switching pulses for leg A switches, S_1-S_4 and B_1, in which, three carrier signals CR_1, CR_2 and CR_3 are compared with one sinusoidal reference signal SR_A, producing three controlling signals X_1, X_2 and X_3. Equations (6)-(10) describe the logical operation applied on X_1-X_3 signals to produce the required switching pulses. Also, these pre-described operators in (6)-(10) can be applied on X_4-X_9 signals to generate the switching pulses for switches in legs B and C. The X_4-X_9 are the controlling signals, resulting from the comparison process between three carrier signals and other two phase-shifted sinusoidal signals SR_B and SR_C. The last trace in Fig. 4 shows the pole voltage V_{A0} with four voltage levels of 0, $E/3$, $2E/3$, and E, being marked by the switching states in Table I.

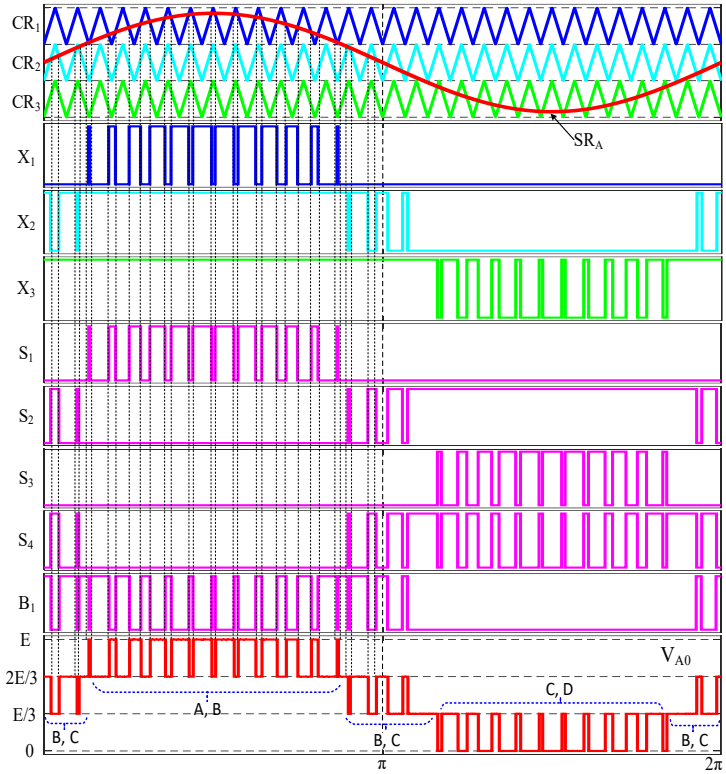


Fig. 4 Switching pattern and pole voltage under the LSPWM scheme (leg A).

$$S_1 = X_1 \tag{6}$$

$$S_2 = \overline{X_2} \tag{7}$$

$$S_3 = \overline{X_3} \tag{8}$$

$$S_4 = \overline{X_2} \times X_3 \tag{9}$$

$$B_1 = \overline{X_1} \times X_2 \tag{10}$$

IV. VOLTAGE BALANCING CONTROL OF THE DC-LINK CAPACITORS

The capacitor voltage imbalance is common in four-level inverter topologies, where three capacitors are connected in series to divide the DC-link voltage into three equal parts as shown in Fig. 1 (b). A generalized mechanism for investigating the capacitor voltage imbalance in the four-level topologies was provided in [27]. The three capacitor currents I_{C1}, I_{C2}, and I_{C3} in the single source configuration (SSC) of the proposed topology are not equal, causing a voltage imbalance. The current of the middle capacitor I_{C2} is larger than the currents of other capacitors I_{C1}, and I_{C3}, which are equal. Consequently, the C_1 and C_3 discharge less energy than C_2. Specifically, C_2 discharges faster to zero while the full DC-link voltage V_{dc} is equally shared between C_1 and C_3. The three capacitor currents can be equalized by either applying a voltage-balance control [23, 27, 31-34] or using voltage-balance circuitry [35, 36]. The variable-carrier scheme (VCS) can effectively control the voltage balance among the three capacitors [27, 34], thus it is chosen to balance the capacitor voltages in this work.

The capacitor voltages are not balanced because of the over-discharge of C_2. Therefore, by regulating the C_2 voltage V_{C2}, the other capacitors C_1 and C_3 can be balanced at V_{C1} and V_{C3}, where $V_{C1}= V_{C3}= (V_{dc}–V_{C2})/2$. Consequently, the three capacitor voltages V_{C1}, V_{C2}, and $V_{C3,}$ could be equated when V_{C2} is regulated at $V_{dc}/3$. Fig. 5 describes the basic principle of the voltage balance control for the proposed topology, consisting of modulation signal generation block, carrier signal block, and the proportional-integral (PI) controller-based voltage loop. These three parts are used to generate modulation signals with a third-harmonic injection, variable and fixed carrier signals, and regulate the C_2 voltage at $V_{dc}/3$. The three carrier signals, CR_1, CR_2, and CR_3, have the same phase shift and frequency, but are different in the amplitude and level shift. CR_1 and CR_3 have a fixed amplitude of 1.5, and are shifted in level of 1.5, but the amplitude of CR_2 is variable. It can be any value from 0 to 1.5β, where β is the PI output. Increasing the amplitudes of CR_1 and CR_3 compared to the LSPWM in Fig. 4 raises the duty cycles of S_1 and S_3 (d_{S1} and d_{S3}) as shown in Fig. 6, discharging more energy from (C_1 and C_2) and (C_2 and C_3), respectively. On the other hand, the duty cycles of B_{12} and S_2 (d_{B12} and d_{S2}) are changing through the PI controller, aiming to regulate the middle capacitor voltage V_{C2} at $V_{dc}/3$. Accordingly, the capacitor voltages are effectively balanced.

V. SIMULATION AND EXPERIMENTAL RESULTS

Several simulations and experimental tests were carried out and presented in this section to verify the operating concept of the proposed four-level inverter topology. It is worthy to clarify that the included results in this section are for both

configurations, SSC and MSC. The MSC is first numerically verified in MATLAB Simulink, and then experimentally validated through the in-house test setup. The SSC results are obtained by using the OPAL-RT real-time simulator OP5707 [37].

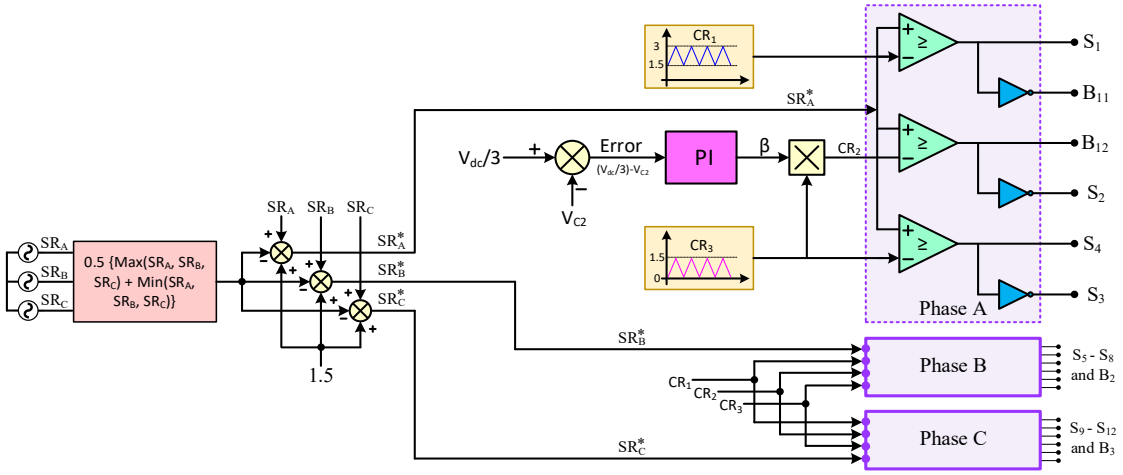


Fig. 5 Overall voltage-balance control of the DC-link capacitors.

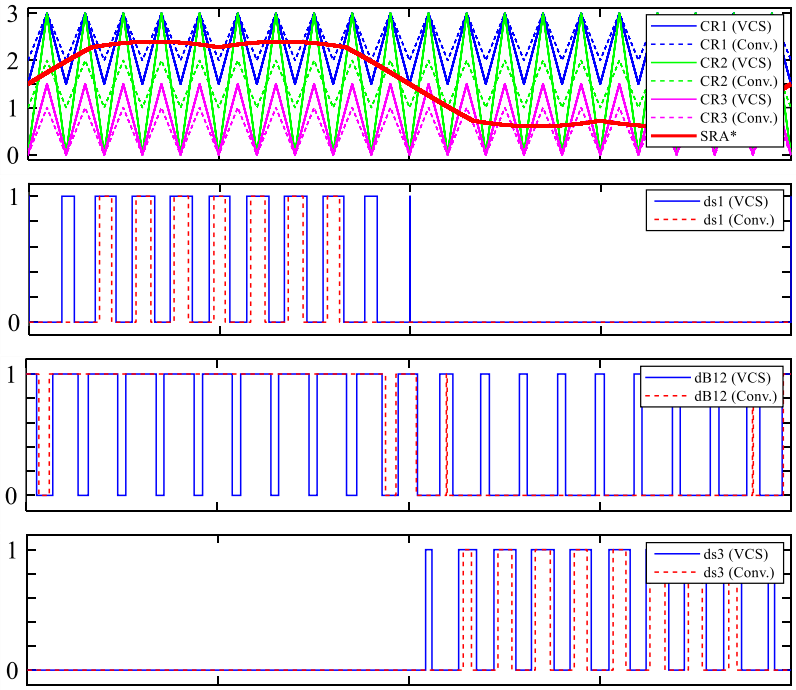


Fig. 6 Switch duty cycles under the variable-carrier scheme (VCS) and the conventional LSPWM scheme.

Table II shows the system specifications of the simulation and experimental validations. Fig. 7 shows the inverter prototype, consisting of three 62024P-100-50 DC voltage sources, eighteen SKM300GA12E4 IGBT modules act as power switches (S_1-S_{12} and B_1-B_3) accompanied by SKHI 10/12 R gate-driver boards, and dSPACE's MicroLabBox digital controller. Further, a low-power DC voltage source for control circuits, and some measurement devices, such as oscilloscope, voltage and current probes, are shown in Fig. 7.

TABLE II
USED COMPONENT AND SYSTEM SPECIFICATIONS

Description	Value/ Part number	Unit
DC-link voltage (V_{dc})	150	V
Load resistor (R)	40	Ω
Load inductor (L)	100	mH
Switching frequency (F_S)	2	kHz
Modulation frequency (F_o)	50	Hz
Modulation index (MI), LSPWM	0.9	–
Modulator signals (H), LFM	±0.35	–
Sampling time (T_S)	15	μs
DC voltage source	62024P-100-50	–
Switching device	SKM300GA12E4	–
Gate-driver board	SKHI 10/12 R	–

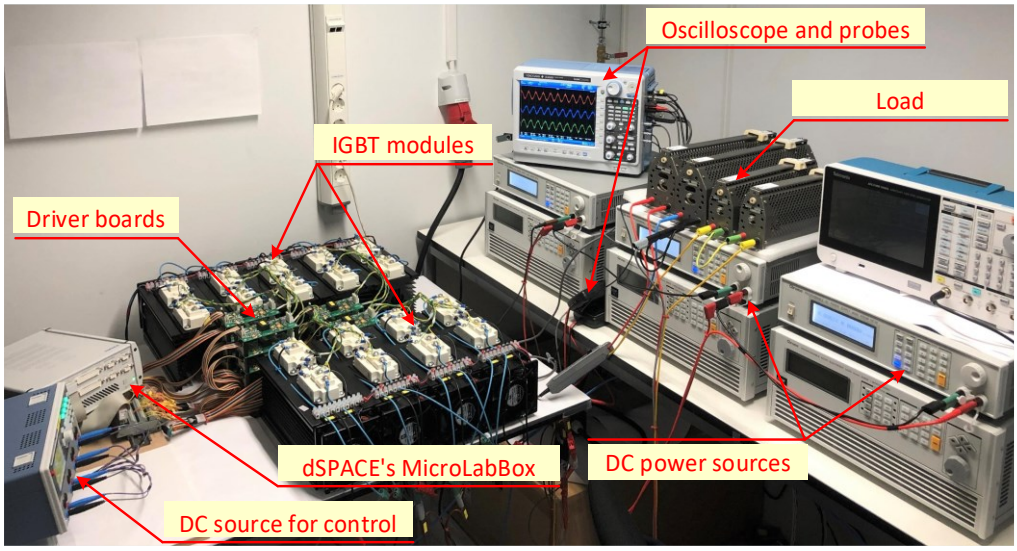
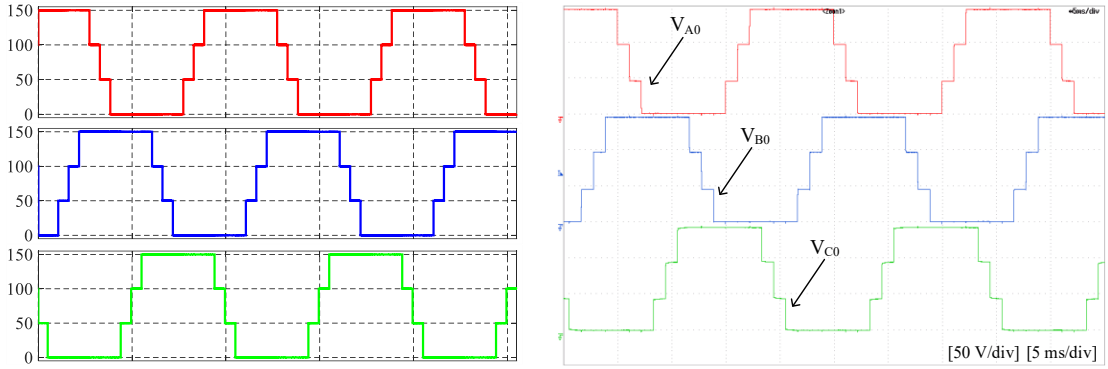


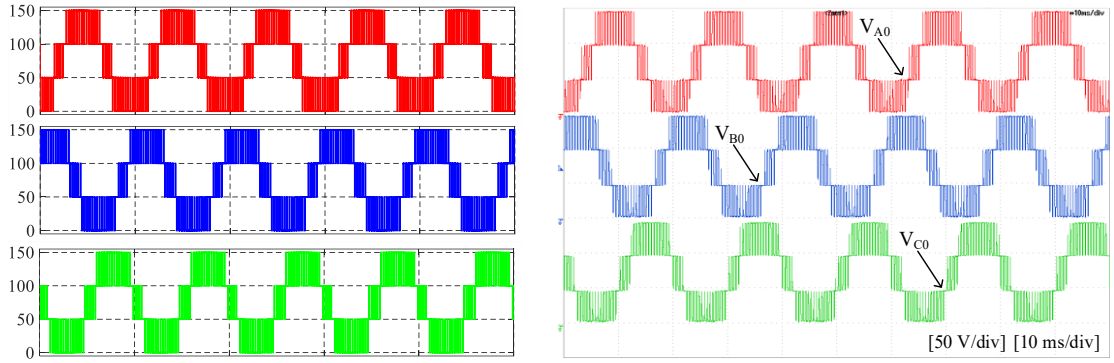
Fig. 7 The in-house experimental setup.

The switching schemes shown in Figs. 3 and 4 are executed using the digital controller, producing the required switching pulses for the different switches in the proposed topology. These switching pulses control the corresponding switches to produce pole voltages with specific phase angles and level counts, as shown in Figs. 8 and 9. Figs. 8(a) and (b) depict the simulation and experimental results for the pole voltages V_{A0}, V_{B0}, and V_{C0} when using the LFM scheme. Each pole voltage has three voltage levels of 50 V and a phase shift of 120° to the adjacent pole voltages. Further, the consistent pole voltage waveforms are shown in Figs. 9(a) and (b) when using LSPWM switching scheme. The three pole-voltage V_{A0}, V_{B0}, and V_{C0}, are the key waveforms for synthesising both line and phase voltages. For example, the line voltage V_{AB} is synthesized by subtracting two poles voltage V_{A0} and V_{B0} while the phase voltage V_{AN} is generated from the three poles voltages by $V_{AN} = (2V_{A0} - V_{B0} - V_{C0})/3$.



(a) (b)

Fig. 8 Pole voltages V_{A0}, V_{B0}, and V_{C0} using LFM (a) Simulation, (b) Experimental.

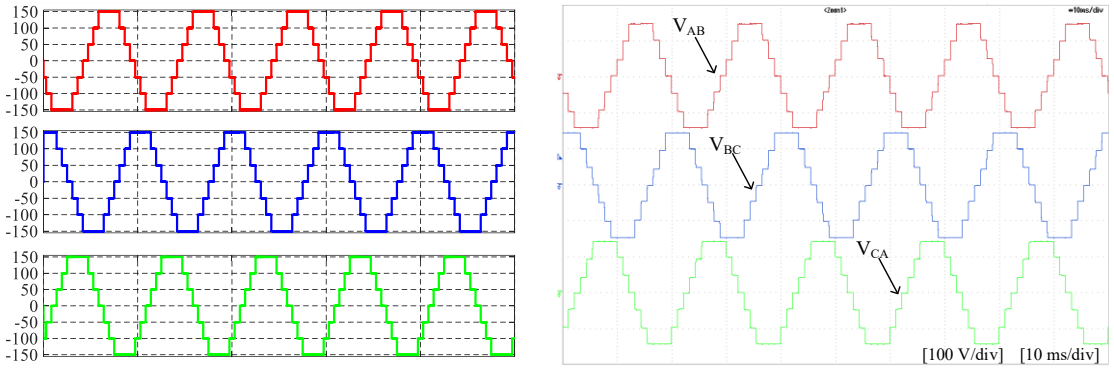


(a) (b)

Fig. 9 Pole voltages V_{A0}, V_{B0}, and V_{C0} using LSPWM (a) Simulation, (b) Experimental.

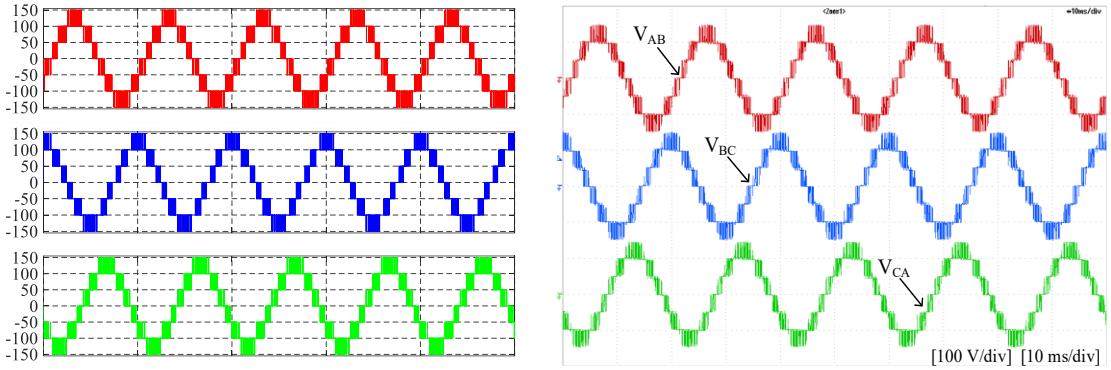
Figs. 10 and 11 show the line voltages V_{AB}, V_{BC}, and V_{CA} when using LFM and LSPWM schemes, respectively. As seen in Figs. 10 and 11, the proposed topology is capable for generating seven-level waveforms: three positive levels of 150, 100, and 50 V, zero-voltage level, and three negative levels of -50, -100, and -150 V. These line voltages are balanced and identical in both simulation and experimental tests. The proposed topology is further tested on resistive and inductive loads, as shown in Figs. 12-14. Fig. 12 illustrates the obtained simulation and experimental results of the line voltage V_{AB}, phase voltage V_{AN} and load current I_{AN} when delivering the power to the resistive loads of 40 Ω. Furthermore, the waveforms under the resistive-inductive loads of 50.86∠42.3° (R= 40 Ω and L= 100 mH) are described in Figs. 13 and 14 for LFM and LSPWM schemes, respectively. As seen from Figs. 12-14, the load current I_{AN} has a phase shift of 0° and 42.3° under the *R* and *R-L* loads, respectively.

The key results for the SSC of the proposed topology are presented hereafter. The DC-link voltage V_{dc} has the same value as in the experimental validation of the MSC, and is divided into three equal parts by using three capacitors of 1000 µF. The control scheme shown in Fig. 5 is used to generate the switching pulses for controlling the voltage of three DC-link capacitors at $V_{dc}/3$.



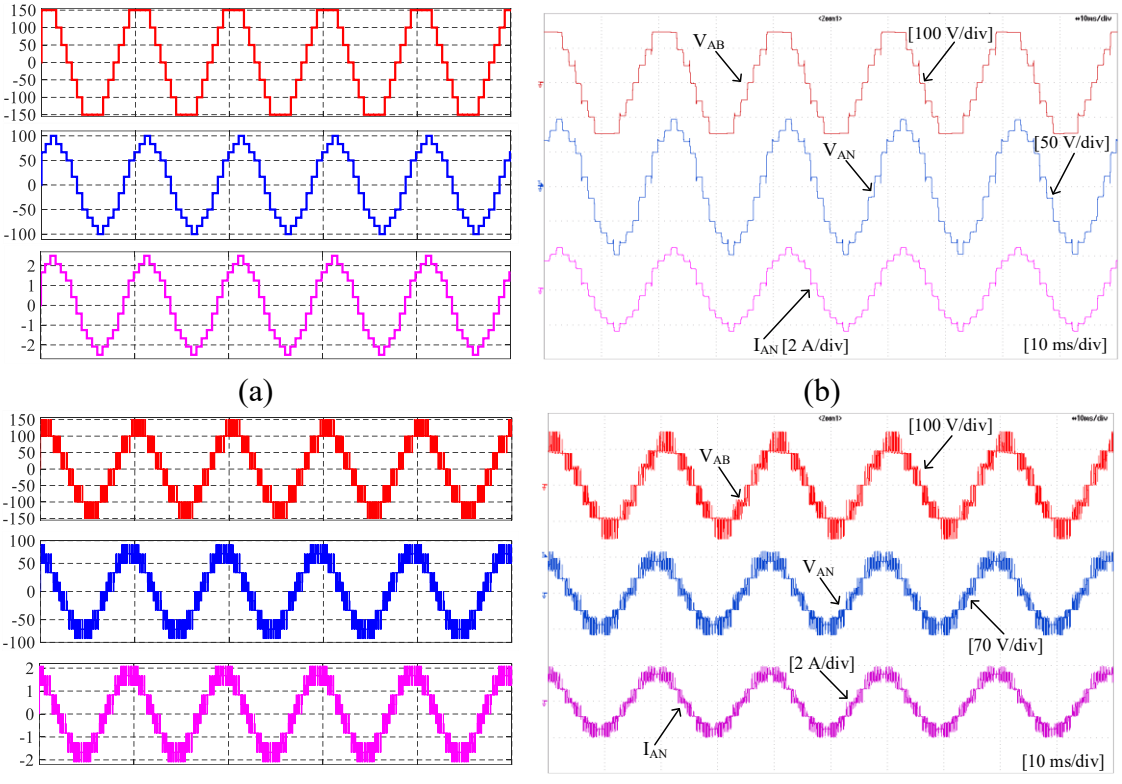
(a) (b)

Fig. 10 Line voltages V_{AB}, V_{BC}, and V_{CA} using LFM (a) Simulation, (b) Experimental.



(a) (b)

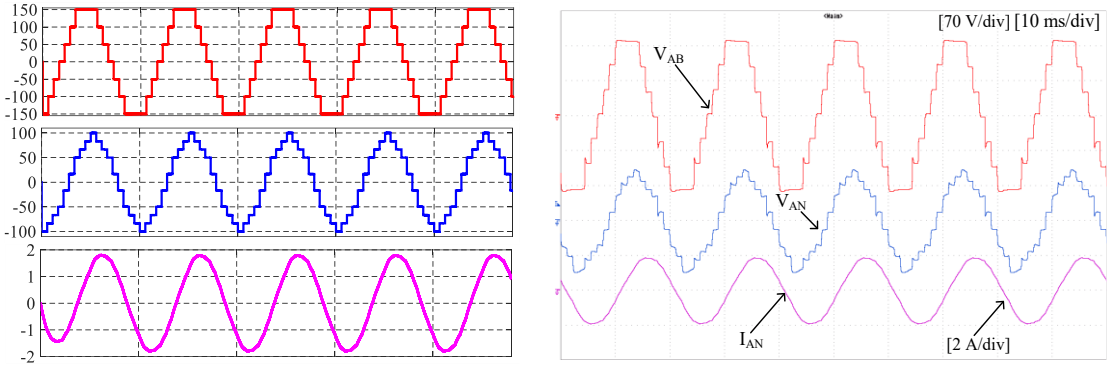
Fig. 11 Line voltages V_{AB}, V_{BC}, and V_{CA} using LSPWM (a) Simulation, (b) Experimental.



(a) (b)

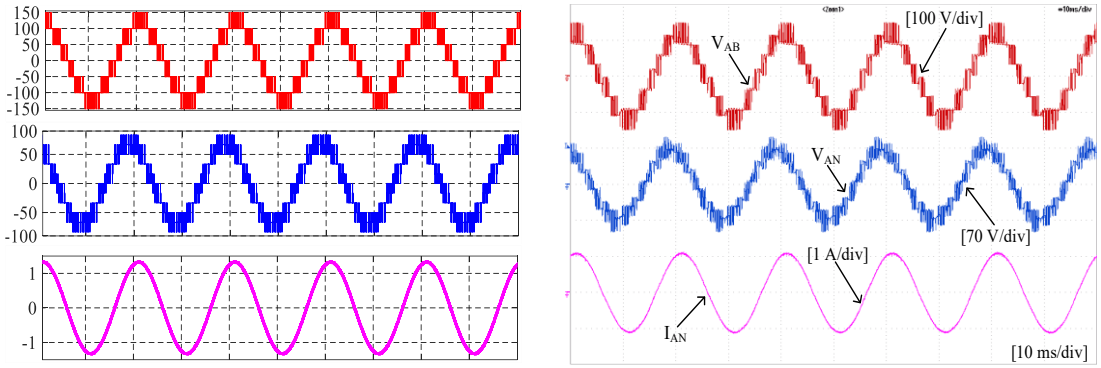
(c) (d)

Fig.12 Obtained V_{AB}, V_{AN}, and I_{AN} when feeding R-load (a) Simulation (LFM), (b) Experimental (LFM), (c) Simulation (LSPWM), (d) Experimental (LSPWM).



(a) (b)

Fig. 13 Obtained V_{AB}, V_{AN}, and I_{AN} for R-L load using LFM (a) Simulation, (b) Experimental.



(a) (b)

Fig. 14 Obtained V_{AB}, V_{AN}, and I_{AN} for R-L load using LSPWM (a) Simulation, (b) Experimental.

Fig. 15 shows the line voltage V_{AB}, phase voltage V_{AN} and the load current I_{AN} when a resistive-inductive load is connected to the proposed topology. Further, Fig. 16 illustrates the effectivity of the applied voltage-balance control of the DC-link capacitors C_1, C_2, and C_3. The three capacitor voltages V_{C1}, and V_{C2}, and V_{C3} are balanced for a wide range of modulation indices (MIs) as shown in Fig. 16(a), in which the MI changes from 0.9 to 0.3, keeping an acceptable tolerance of the capacitor voltages (V_{C1}= 51.21 V, V_{C2}= 50.20 V, and V_{C3}= 49.03 V). Further, Fig. 16(b) shows that the voltage-balance control can balance the capacitor voltages nearby 50 V (V_{C1}= 50.58 V, V_{C2}= 50.48 V, and V_{C3}= 49.37 V), while changing the load value by 100%, from (R = 30 Ω and L= 10 mH) to (R = 15 Ω and L= 5 mH). In Fig. 16, the voltage scale of V_{C1}, V_{C2}, and V_{C3} is 25 V/div, resulting in vague changes in the voltage waveforms when varying loads or modulation index.

VI. Power Losses and Efficiency Analysis

The loss analysis of the proposed topology is presented in this section to illustrate the effects of some salient parameters such as switching frequency (F_s) and load value on the conversion efficiency. The major part of the loss is dissipated in the conversion stage, i.e. in the semiconductor devices, in which the losses have three forms: conduction loss (P_{con}), switching loss (P_{sw}), and OFF-state loss (P_{off}) [38-40].

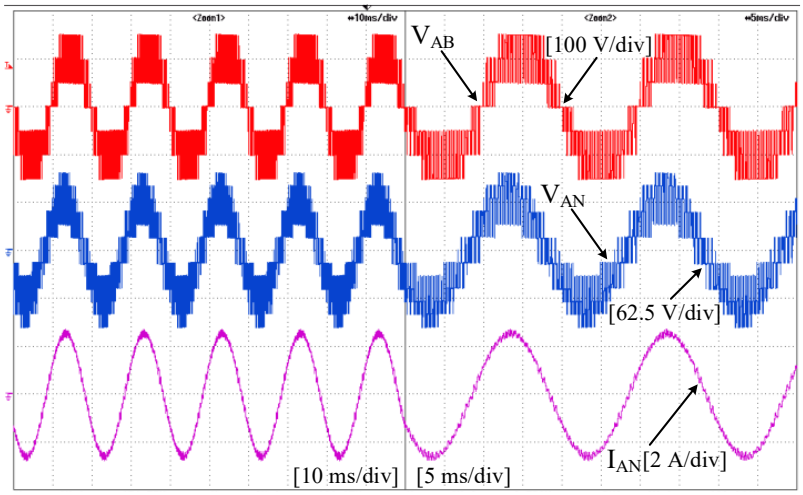
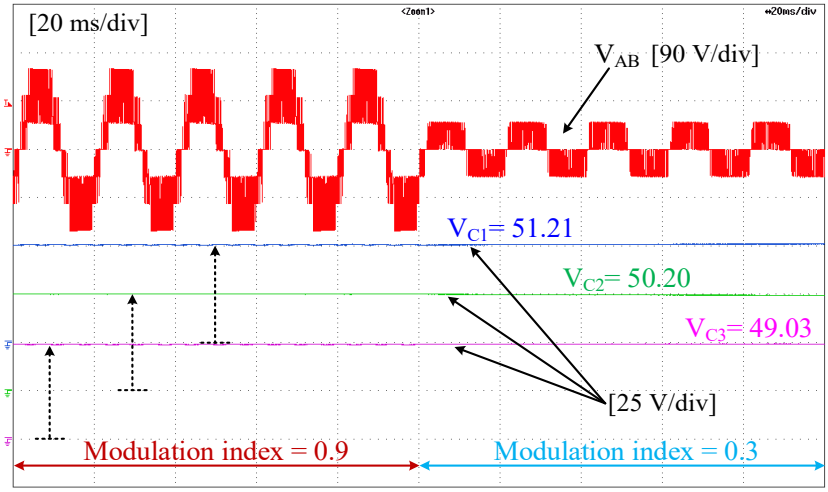
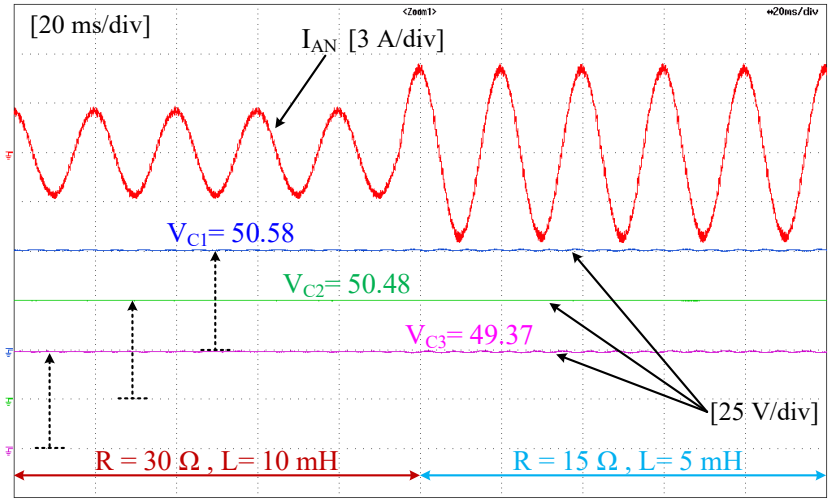


Fig. 15 Obtained V_{AB}, V_{AN}, and I_{AN} for the SSC configuration when feeding R-L load (obtained by using OP5707).



(a)



(b)

Fig. 16 Dynamic results of the SSC configuration (obtained by using OP5707) (a) Changing the MI from 0.9 to 0.3: V_{AB}, V_{C1}, V_{C2}, and V_{C3}, (b) Changing the load value by 100%: I_{AN}, V_{C1}, V_{C2}, and V_{C3}.

The ON-state resistance (R_{on}) and ON-state voltage (V_{on}) in the IGBTs devices cause conduction power loss when the load currents flow through them. The conduction loss depends on the load current and the characteristic of the device (i.e. R_{on}, V_{on}, etc.), while the switching frequency (F_s) does not have direct effects on the conduction loss, but the average value of the conduction loss depends on the duty cycle [40]. However, the switching loss depends on the switching frequency because of slow transitions between the switching states, i.e. transition from ON to OFF, and vice versa. Accordingly, a switching device still conducts a current when a voltage is applied to its terminal, causing a large instantaneous energy loss. For IGBTs, these energies are turn-on energy (E_{on}) and turn-off energy (E_{off}). For diodes, it is termed as reverse recovery energy (E_{rec}). The switching loss is proportional to the blocking voltage of the switching devices as well [38, 39, 41]. Non-zero currents are flowing through the switching devices during their OFF-state periods, causing OFF-state power loss. However, these non-zero currents can be neglectable and are considered as leakage currents [38]. Accordingly, the power loss during the OFF-state periods is ignored in this study. Detailed equations for calculating the power loss in the switching devices are highlighted in [38-41].

A medium-fast trench IGBT module with a part number of SKM300GA12E4 is used to build a model to study the power losses distribution and conversion efficiency of the proposed topology. The used IGBT module has a soft-switching fourth-generation controlled axial lifetime (CAL) freewheeling diode. Table III lists the system specifications and the IGBT module main parameters with an assumption of a 150° C junction temperature. The detailed parameters of the used IGBT module can be found in [42].

TABLE III
SYSTEM SPECIFICATIONS FOR THE LOSS ANALYSIS

Parameter/Specification	Value	Unit
Collector-emitter breakdown voltage (V_{CE})	1200	V
Collector-emitter on-state voltage ($V_{CE,\,on}$)	2.45	V
IGBT on resistance ($R_{CE,\,on}$)	5.5	mΩ
Forward voltage (V_f)	2.42	V
Turn-on delay time ($T_{d,\,on}$)	220	ns
Rise time (T_r)	51	ns
Turn-off delay time ($T_{d,\,off}$)	515	ns
Fall time (T_f)	105	ns
Diode on-resistance (R_{on})	4.4	mΩ
Junction temperature (T_j)	150	°C
Switching frequency (F_s)	2, 5, 8	kHz
Modulation index (MI)	1	-
Power factor (PF)	0.897	-
Input DC sources	350	V
Rated output power (P_{out})	5	kW

The efficiency of the proposed topology is studied under varying the switching frequency and load. The switching frequency is changed from 2 kHz to 8 kHz in the step of 3 kHz, while the load is changed from 0.5 kW to 5 kW in steps of 0.5 kW.

Fig. 17 illustrates the dependency of the efficiency on the switching frequency and load conditions. The efficiency increases when raising the load, and decreases when the switching frequency rises. For example, at the switching frequency of 5 kHz, the efficiency is increased from 96.65% to 99.15% when increasing the load from 0.5 kW to 5 kW. Contrarily, it is decreased from 99.19% to 98.41% when increasing switching frequency from 2 kHz to 8 kHz at 2.5 kW load, matching well power-loss calculations in literature [38-41]. It is emphasized that all switching device parameters and the other system specifications (i.e. input voltage, power factor, modulation index, etc.) are kept constant while studying the effects of the switching frequency or load on the total efficiency.

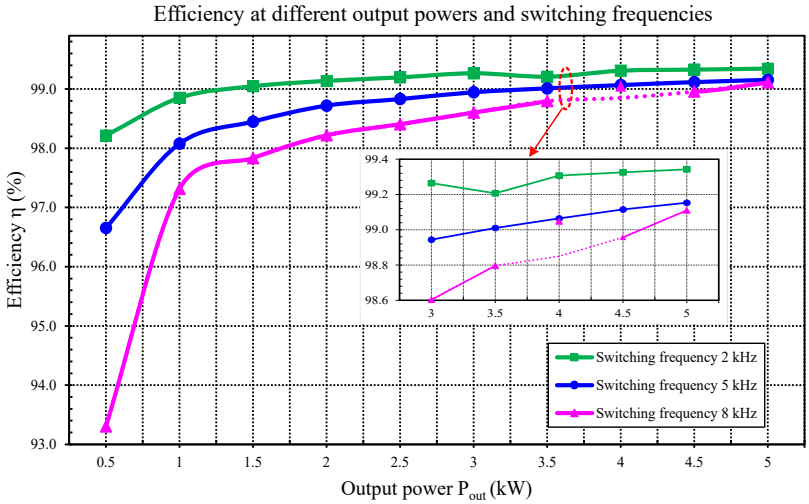


Fig. 17 The dependency of the conversion efficiency on the switching frequency (F_s= 2, 5, and 8 kHz) and output power.

As mentioned above, both switching loss (P_{sw}) and conduction loss (P_{con}) are considered the dominant losses in semiconductor devices. Therefore, the power loss distribution of individual switches is studied and subdivided into switching and conduction losses. Fig. 18 shows the power loss distribution among different switches at the switching frequency of 5 kHz and the output power of 2.5 kW. Since the load and switching frequency are constant, the conduction and switching losses are directly proportional to the conduction period and switching voltage, respectively. For example, the switching losses in switches S_1, S_5, S_9 are higher than those of the remaining switches because they block higher voltages. The switches S_4, S_8, and S_{12} have the lowest conduction loss since their conduction periods are shorter than those of other switches.

The effect of modulation schemes, namely LFM and LSPWM, on the efficiency of the proposed topology is highlighted in this section. The efficiency is obtained when increasing the load power from 10% to 100%, by step of 10%. The system specifications in Table III are kept the same when changing the modulation schemes between LFM and LSPWM. It is noting that the switching frequencies of LFM and LSPWM are 50 Hz and 5 kHz, respectively. Using LFM at only 50 Hz results in the lower switching loss P_{sw} as compared to using LSPWM, increasing the conversion efficiency as shown in Fig. 19. As explained in Section III, LSPWM is required to control the output voltage better.

Among all addressed four-level topologies in this paper, the topology in [28] is considered as the closest circuit to the proposed topology from the structural point of view. Therefore, an efficiency comparison between the two topologies is carried out while keeping system parameters identical as listed in Table III. Fig. 20 shows the efficiency of the two circuits at different loads, proving that the efficiencies of the two topologies have a good agreement with small differences.

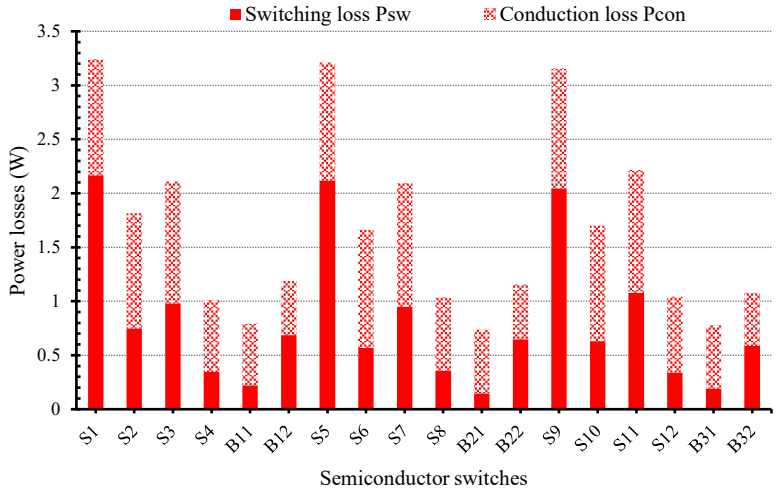


Fig. 18 Power loss distribution in the used switches at 5 kHz switching frequency and 2.5 kW output power.

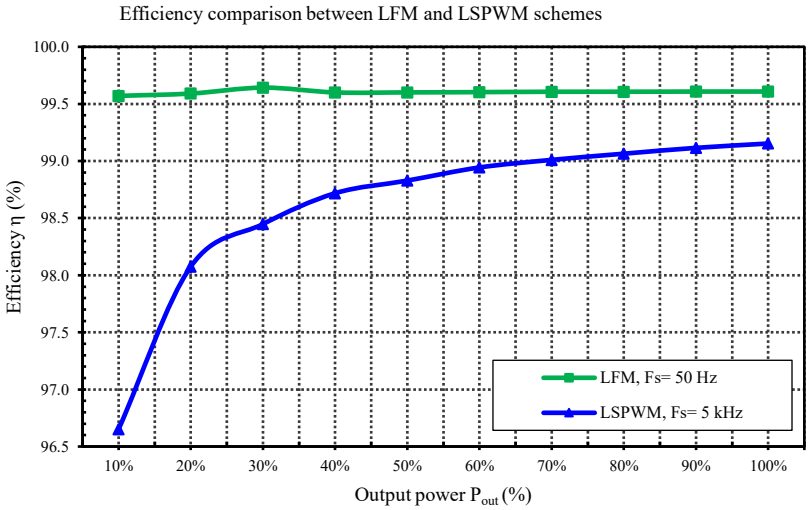


Fig. 19 Efficiency comparison between the low-frequency modulation (LFM) and level-shifted pulse width modulation (LSPWM).

VII. Comparative Study

The SSC of the proposed topology is compared with both the recently published four-level inverters [20-28] and some conventional MLI topologies. A summary of this comparative study is provided in this section, clarifying the salient features of the proposed topology. The counterpart MLI topologies are labelled by T_1 to T_{10} and quantitively compared in term of the counts of DC sources N_{DC}, switches N_{SW}, diodes N_D, and capacitors N_C. Each element in any component group (e.g. the group

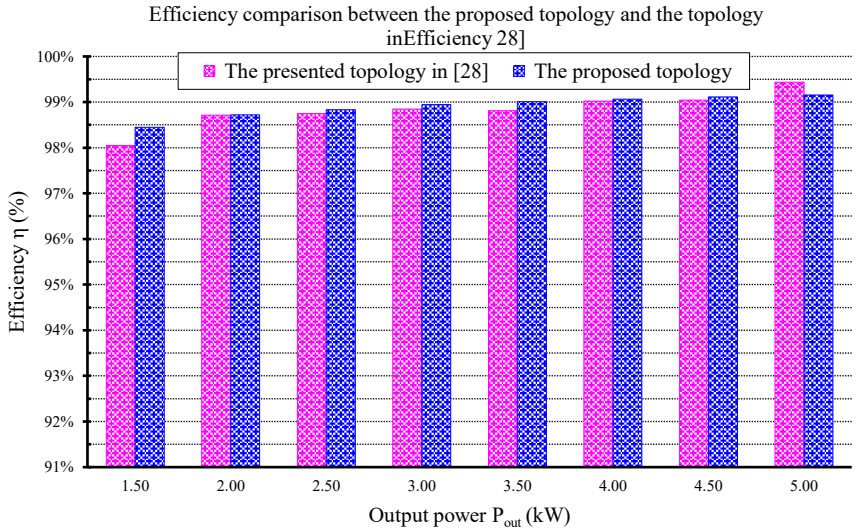


Fig. 20. Efficiency comparison between the proposed topology and the topology in [28].

of switches, diodes, etc.) is accompanied by its voltage rating while the current rating is assumed to be equal to the load current for all components. Some additional conditions are considered for obtaining a fair comparison among the different topologies: A) producing same output line voltages in terms of both the peak and step value, for example, V_{AB} must have seven levels of $E/3$ step and can reach a peak of $\pm E$ (i.e., E, $-2E/3$, $-E/3$, 0, $E/3$, $2E/3$, and E), B) all switching devices are counted based on unidirectional configuration, or any bidirectional switch is disassembled to its primary elements, for example, the proposed topology has three bidirectional switches: each is configured by connecting two unidirectional switches in a common emitter configuration, so they are counted as six unidirectional switches. Table IV summarizes the component counts of three-phase configurations, where the compared topologies are listed in descending order based on the total component count.

According to Table IV, topologies T_1 and T_2 require the highest component count while T_9, T_{10}, and the proposed topology have the lowest one. In terms of switch count, the topology T_1 has the lowest number of switches (i.e. twelve switches), but it needs twenty-four diodes, being the highest count among the compared topologies. However, topologies T_4-T_{10} and the proposed topology do not use clamping diodes. In terms of the capacitor count, T_5 requires nine flying capacitors, being the highest number among the addressed MLIs while the proposed topology and topologies T_1, T_2, T_6, T_7, T_9, and T_{10} do not need flying capacitors.

It is noted that the topologies T_9 and T_{10} have a similar component count like the proposed topology and they do not require any clamping diodes or flying capacitors, making them the possible counterparts of the proposed inverter. Nevertheless, as compared to T_9 and T_{10}, the proposed topology has advantageous features: A) it has a 50% reduction in the high-voltage switches. Only three switches must withstand to E while in the topologies T_9 and T_{10}, six switches must block E. B) the proposed topology has a total standing voltage (TSV) lower than the topology T_{10}. It has a TSV of $10E$ (TSV= $9*E/3+6*2E/3+3*E$) while T_{10} has TSV of $12E$ (TSV= $6*E/3+6*2E/3+6*E$), reducing the total cost of the required

switches. C) Although both the proposed topology and the topology T_9 have a TSV of 10E, the proposed topology has a lower switch count in the conduction paths than the topology T_9. For each inverter leg, it reduces one switch, giving the proposed topology an extra advantage in reducing the conduction loss.

TABLE IV
COMPARISON OF THE PROPOSED TOPOLOGY WITH OTHER FOUR-LEVEL INVERTERS [20-28] IN TERMS OF REQUIRED COMPONENTS AND VOLTAGE RATING

Topology	N_{DC}		N_{sw}			N_D		N_C		
	E/3	E	E/3	2E/3	E	E/3	2E/3	DC-link		Flying
								E/3	E/2	E/3
T_1 [20], EI-MLI	0	1	0	6	6	12	12	3	0	0
T_2, NPC-MLI	0	1	18	0	0	18	0	3	0	0
T_3 [21], NNPC MLI	0	1	18	0	0	6	0	0	2	6
T_4 [22], hybrid π-type MLI	0	1	18	6	0	0	0	3	0	3
T_5, FC-MLI	0	1	18	0	0	0	0	3	0	9
T_6 [23], 4L-ANPC MLI	0	1	24	0	0	0	0	3	0	0
T_7, half-HB MLI	9	0	18	0	0	0	0	0	0	0
T_8 [24-26], NT-type MLI	0	1	12	6	0	0	0	0	0	6
T_9 [27], DT-Type MLI	0	1	12	0	6	0	0	3	0	0
T_{10} [28], π-type MLI	0	1	6	6	6	0	0	3	0	0
The proposed MLI	0	1	9	6	3	0	0	3	0	0

VIII. CONCLUSION

This paper proposes a novel inverter topology with a reduced component count, being attractive in low- and medium-voltage applications. The proposed circuit generates four voltage levels without requiring flying capacitors or clamping diodes, reducing the size, cost, control complexity of the inverter and enhancing its reliability and lifetime. Several simulation and experimental tests were presented to validate the proposed topology performance at resistive and inductive loads. The proposed inverter was compared with the recently developed four-level topologies to highlight its merits. Moreover, its conversion efficiency was analysed when varying the switching frequency, modulation schemes, and loads.

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Paper III:

Novel Three-Phase Multi-Level Inverter with Reduced Components

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Novel Three-Phase Multi-Level Inverter with Reduced Components

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***Abstract*—A new multilevel converter topology is proposed in this paper. Low component count and compact design are the main features of the proposed topology. Furthermore, the proposed converter is a capacitor-, inductor-, and diode-free configuration, allowing reducing the converter footprint, increasing the lifetime and simplifying the control strategy. Further, a comparative study is carried out to highlight the merits of the proposed circuit as compared to existing multilevel topologies. Finally, simulation results for the three-level version using different modulation strategies are presented.**

Index Terms— Fundamental frequency modulation, multilevel inverters, pulse width modulation

I. Introduction

Nowadays, renewable energy generators (REGs) are interconnected to the grid with a higher penetration for the purpose of meeting the increased demand for energy worldwide with keeping CO_2 emissions at low levels. Accordingly, notable improvements to energy conservation and a significant reduction of CO_2 emissions are achieved. Nevertheless, there are constant needs for proposing new technologies in order to increase system reliability and efficiency. Recent developments in those technologies have heightened the need for improving power electronics converters (PECs) that link the original energy source to the grid. PECs play an essential role in power systems containing renewable generators, as they take the responsibility of converting the generated primary power from REGs to be matched with the grid or load standards. Additionally, PECs are used for increasing the overall performance of generating systems because of their ability to integrate different storage technologies allowing doing several essential services such as energy arbitrage, peak shaving, load flowing, spinning reserve, voltage support, black start, and frequency regulation, etc. [1].

The main REGs are photovoltaic (PV), wind power (WP), and hydropower plants (HPPs). In these generating systems, various converter families already have been used for a long time, like traditional voltage source converters (VSCs), matrix converters (MCs), and cyclo-converters (CCVs). However, significant problems with these converters have limited power handling due to limited maximum power rating of available semiconductor devices, high total harmonics distortion (THD) in input and output sides, and negative influence on the power factor of the system by using none-fully-controlled converters such as CCV [2-5]. Several solutions have been presented for the purpose of overcoming the abovementioned

limitations, including using identical converters in parallel configurations for increasing the handled power, using complex, bulky and specially designed filters for improving the THD, and using compensation circuits for controlling the reactive power and improving the power factor in non-fully controlled converters. However, these solutions becoming unattractive today because they increase the weight, volume, complexity, and cost of PECs while decreasing efficiency, reliability and lifetime of the energy system [2, 3, 5]. These drawbacks prevent the use of these converters in high power applications. Unique features of modularity, low dv/dt, low THD, low switching frequency, low electromagnetic interferences, low filtering requirements, and low switching losses of multilevel converters (MLCs) allow them to be used intensively in modern medium- and high-power energy systems [6-8]. In other words, MLCs-based systems produce high-quality outputs with reasonable side effects.

Neutral point clamped converter (NPC) [9, 10], flying capacitors converter (FC) [11, 12], and cascaded H-bridge converter (CHB) [13] are three common topologies of MLCs. High component count, namely DC sources, electrolytic capacitors, transformers, switching devices, and power diodes, increasing the converter footprint, cost, conduction losses, control complexity and decreasing the lifetime is the main drawback of the mentioned topologies [6-8]. To tackle these drawbacks, several topologies were recently presented in [14-20], aiming to improve conventional configurations by proposing new circuits with reduced components count and simplified control algorithms. Towards this aim, a new multilevel converter topology is proposed in this paper. The proposed topology can produce the same number of voltage levels with low component count compared to the existing configurations. Further, the proposed topology has a compact design feature as it does not require either transformers or electrolytic capacitors for operation. This compact feature is important in portable solutions requiring a reduced size of the converter and low cooling system requirements. Besides, the losses in the proposed circuit will be decreased dramatically because of using only switching devices operating at low frequencies instead of using hybrid designs based on switches and diodes.

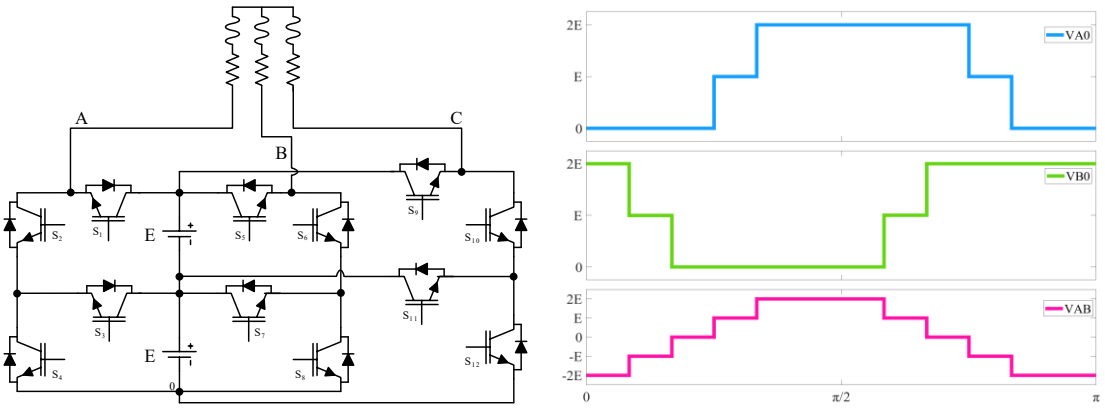
This paper is organized as follows. The operating principles of the proposed topology will be presented for three-level configuration in section II. In section III, a comparison between the proposed circuit and other MLC topologies for generating the same number of voltage levels will be provided. Then, the two applied switching schemes will be explained in section IV, while section V will introduce the simulation results for the two modulation schemes. Finally, conclusions will be withdrawn in section VI.

II. THE PROPOSED MULTI-LEVEL CONVERTER CONFIGURATION

Simplifying the converter structure is the main objective when designing the proposed MLC topology. By this way, a simple control system can be used, and an extra reliability degree can be obtained. To achieve this target, electrolytic capacitors, power transformer, and power diodes should not be used in the design of the proposed topology in order to avoid increasing the size, losses, and decreasing the lifetime of the converter. For wider applications, the input DC ports

should be decreased as well. Consequently, the number of required isolated DC sources will be reduced. One DC source is normally defined by an isolation transformer combined with a six-pulse rectifier. Therefore, saving one DC source means saving six power diodes and one isolation transformer. According to this perspective, the proposed topology is designed to have a fewer number of isolated DC sources while keeping reasonable switching device count. The proposed topology uses only two DC sources and twelve switching devices for producing three-level pole voltages, resulting in five-level line voltages. The two isolated DC sources can be realised for example by using two PV generators. Fig. 1 shows the power circuit and the resulting voltages of the proposed MLC. Although the proposed topology can be extended to N level, only the three-level configuration is studied in this paper.

Throughout this paper, the term -pole voltage- will refer to the voltage difference between point A or B or C and point 0. The pole voltages V_{A0}, V_{B0}, and V_{C0}, are used for synthesising both line and phase voltages. For this reason, both of the two switching strategies are designed for controlling the used switches in a way to produce three-level voltage waveforms having phase shifts of 120°. As a result, five-level line voltages can be produced as shown in Fig. 1(b), where the line voltage V_{AB} is constructed by subtracting V_{A0} from V_{B0}.



(a) (b)

Fig. 1. The proposed three-phase multilevel topology. (a) The power circuit for the proposed topology. (b) Line voltage V_{AB} synthesization using pole voltages V_{A0} and V_{B0}.

III. Comparison of the Proposed Topology with Other MLC Topologies

Conventional multi-level converters, namely CHB, FC, and NPC have several shortcomings in both control and component count as mentioned in section I. To overcome these limitations, new and modified topologies have been reported in [14-20]. These topologies aim to decrease the component count while increasing efficiency and reliability. Although these configurations are widely used in industrial applications, some of them are still in investigation and improvement stages. Table I summarises the results of a comparative strategy regarding the required components for producing an equal number of voltage levels.

The comparative strategy is based on unified constraints as follows: producing three-level pole voltages for each topology, using only symmetrical DC sources, i.e. DC voltage source has a rating 2E was counted as two DC sources each has a rating of E, single-phase topology being converted to a three-phase version before comparison.Table I shows a comparison between the proposed topology and existing circuits in literature in term of the component count at the same voltage levels and the mentioned constraints. The proposed topology can produce the same output voltage levels while using a lower component count as compared to the other three-level configurations. The main advantages of the proposed topology are capacitor-, diode-, and inductor-free, allowing the proposed MLC to have a longer lifetime, lower switching losses, and compact design. The main characteristics and limitations of the compared topologies are highlighted and discussed in the following paragraphs.

TABLE I. COMPARISON BETWEEN THE PROPOSED TOPOLOGY AND THREE-LEVEL MLC TOPOLOGIES

Topology	**DC Sources**	**Switches**	**Diodes**	**Capacitors**	**Inductors**	**Total**	**CLF** [a]
Modified T-type [19]	1	9	12	2	0	24	8.0
Fig. 8 in [16]	3	9	9	0	3	24	8.0
In [18]	1	18	0	3	0	22	7.3
Neutral point clamped (NPC)	1	12	6	2	0	21	7.0
Active T-type converter [14, 17]	1	18	0	2	0	21	7.0
In [20]	1	12	3	4	1	21	7.0
Cascaded half H-Bridge (CHHB)	6	12	0	0	0	18	6.0
Flying capacitors (FCs)	1	12	0	4	0	17	5.7
Cascaded full H-bridge (CHB)	3	12	0	0	0	15	5.0
T-type converter [14, 19]	1	12	0	2	0	15	5.0
Fig. 5 in [15]	3	9	3	0	0	15	5.0
The proposed topology	2	12	0	0	0	14	4.7

[a] Components per level factor [22]

In [20], a three-level topology was presented, which is an extension of the two-level split-source inverter (SSI) in [21]. It can generate a high-quality three-level output voltage with a boosting feature, making a direct connection of low-voltage energy sources, e.g. photovoltaics (PV), more accessible. For generating three-level, it requires one DC source, twelve semiconductor switches, three power diodes, four capacitors, and only one inductor. Although having features like multi-level outputs, boosting capability, and operating with an only single source, this topology suffers from high current and voltage stresses on the used semiconductor components, limited power transfer capability, increasing the system footprint and control-complexity due to capacitors and inductors, besides decreasing the expected lifetime of the converter. Further, the quality of the output voltage is a function of the gain value, i.e. at low voltages values, the THD of the output voltages rises when increasing the input voltage. Additionally, it needs extra efforts in control algorithms for removing the low-frequency components from not only input current but also output voltage caused by oscillations of flying capacitors voltages. Moreover, during starting, special precautions for limiting the

switch voltage stress and controlling the rise up time, like using soft-start-up-resistors is mandatory for grid-connected mode while in stand-alone mode, those issues can be controlled by especially setting of control parameters in control algorithm.

Authors in [18] have highlighted a new MLC using two main switches to change the polarity of the output voltages, and several groups of anti-parallel switches for level-generator stages. For producing three-level three-phase voltage, this topology requires eighteen switches, three capacitors, and one DC source. The main limitations for this circuit are using electrolytic capacitors for splitting one DC source to three equal divisions, requiring a high number of switches and having high voltage stress across switches, which are used for changing the polarity, resulting in different losses and heat distribution inside the converter. As a result, the converter cost, size, losses, and control complexity are increased while decreasing the system lifetime.

A dual-DC-port asymmetrical MLI (DPAMLI) was designed and analyzed in [15]. It requires nine switches, three power diodes, and three DC sources (two having E and one with 2E) in order to generate three-level voltage for three-phase applications. The neutral point clamped (NPC) and T-type three-level cells are used for derivation of the suggested topology. Although the DPMLI can allow a bidirectional power flow between input and output ports, only a unidirectional version was highlighted and validated in [15] for the purpose of reducing the components count. It is a single-stage converter, being able to connect two DC sources, having different ratings and producing multilevel AC output voltages. This makes the connection of different voltage sources to the same converter easier and efficient. It has two different operating modes, which are selected by the controller according to the relationship between the required output voltage and the actual applied voltage across the low DC port terminals. Although it does not have any problem regarding using electrolytic capacitors, it uses power diodes, increasing losses in the converter. Further, at least six switches have high voltage stresses equal to the voltage applied across the high voltage DC port terminals, limiting this topology to be only applicable in low and medium voltage.

For the purpose of decreasing switch count, authors in [19] have presented a modified three-level topology of well-known T-type MLI. The three bidirectional switches between the load points and the clamped neutral point were replaced by a cell consisting of one switch and four diodes. This topology needs two capacitors, one DC source, twelve power diodes, and nine switches for producing the same output voltage levels as a conventional T-type topology. However, using capacitors and a high number of semiconductor components make this topology unattractive for many applications that require high efficiency, reliability, and smaller size.

Most of the voltage source converters (VSCs) are suffering from the shoot-through problem, resulting in decreasing their reliability and adding complexity in both control stage and protection circuits. One of the most common solutions is adding a deadtime between the complementary switches either by using software or hardware solutions. However, this solution renders several drawbacks such as distortion of output waveforms and increasing the power losses, especially when

using body diodes with a poor performance [16, 23, 24]. The shoot-through problem is a critical problem in MLI topologies due to having a higher number of power switches in different configurations. In [16], another solution is presented in the form of new dual-buck multilevel topologies, allowing splitting one switching leg into two legs. Although these configurations enhance the reliability degree and the control simplicity, they require a high component count in the power circuit. For example, the presented topologies require two DC sources, nine switches, nine power diodes, and three inductors for generating only three voltage levels when feeding three-phase load.

IV. MODULATION SCHEMES FOR THE PROPOSED CIRCUIT

Modulation schemes for MLCs are classified according to the switching frequency into two groups: fundamental and low-frequency modulation. All of these switching schemes are used for producing a specified AC voltage waveform across the converter outputs, increasing the magnitude of the output voltage, decreasing the harmonics contents in both output currents and voltages, and performing others services such as balancing of capacitors voltages and common-mode voltage reductions [6].

In this paper, two switching schemes are applied. The first one is based on a fundamental switching frequency, i.e., staircase modulation (SCM), while the other belongs to low frequency modulation, i.e. level-shifted pulse width modulation (LSPWM). The applied modulation schemes are designed for controlling the proposed topology to produce three-level 0, E, and 2E across pole voltage V_{A0}, five-level 2E, E, 0, -E, and -2E across line voltage V_{AB}, and seven-level 4/3 E, E, 2/3 E, 0, -2/3 E, -E, and -4/3 E across phase voltage V_{AN}.

Table II summarises the twelve switching states that are used in SCM. These switching states are selected in a way to minimise the number of active switches at any instant to reduce the converter losses. Furthermore, LSPWM is implemented

Table II. The switching states and the corresponding pole voltages (X : ON, − : OFF)

V_{A0}	E	2E	2E	2E	2E	2E	E	0	0	0	0	0
V_{B0}	0	0	0	0	E	2E	2E	2E	2E	2E	E	0
V_{C0}	2E	2E	E	0	0	0	0	0	E	2E	2E	2E
S_1	−	X	X	X	X	X	−	−	−	−	−	−
S_2	X	−	−	−	−	−	X	X	X	X	X	X
S_3	X	−	−	−	−	−	X	−	−	−	−	−
S_4	−	−	−	−	−	−	−	X	X	X	X	X
S_5	−	−	−	−	−	X	X	X	X	X	−	−
S_6	X	X	X	X	X	−	−	−	−	−	X	X
S_7	−	−	−	−	X	−	−	−	−	−	X	−
S_8	X	X	X	X	−	−	−	−	−	−	−	X
S_9	X	X	−	−	−	−	−	−	−	X	X	X
S_{10}	−	−	X	X	X	X	X	X	X	−	−	−
S_{11}	−	−	X	−	−	−	−	−	X	−	−	−
S_{12}	−	−	−	X	X	X	X	X	−	−	−	−

by using two symmetrical carrier signals C_{R1} and C_{R2}. These signals have the same magnitude of C_{RM} and phase while having a level shift of C_{RM}. The number of carrier signals N_{CR} is related to the output voltage levels across the pole terminals N by (1) [8].

$$N_{CR} = N - 1 \tag{1}$$

The LSPWM scheme uses three sinusoidal modulation signals, having a magnitude of C_{RM} and a phase-shift of 120°. These signals are compared with C_{R1} and C_{R2} for generating two Boolean signals X and Y. Then the switching signals are produced by executing logical operations on X and Y as described in the proposed equations (2)-(5).

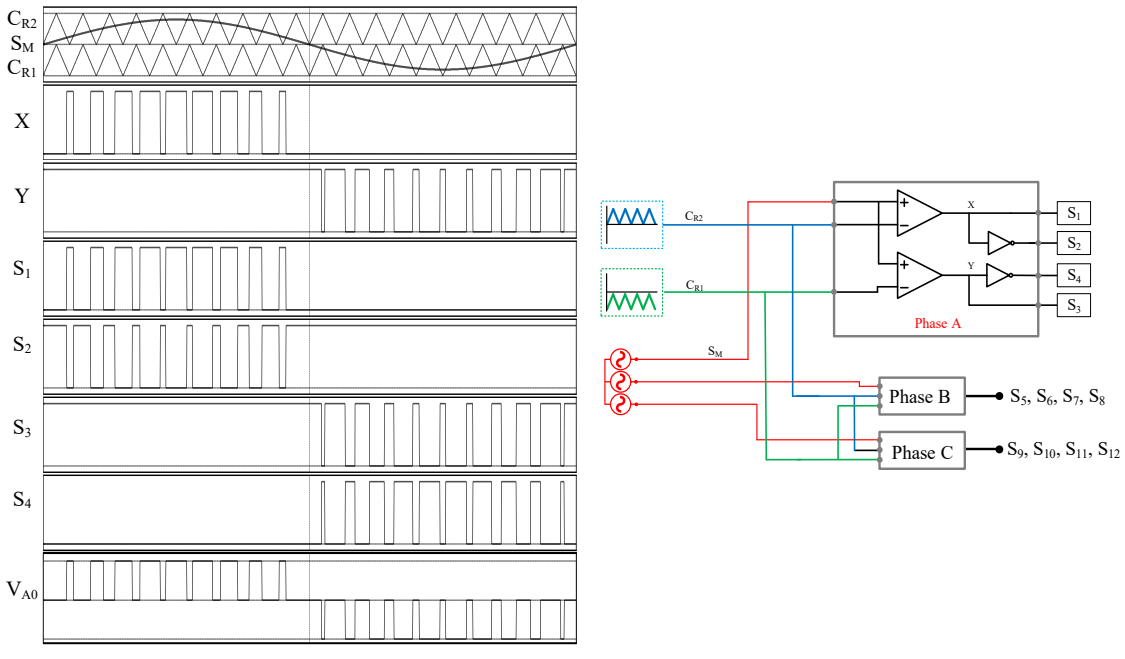
$$S_1 = X \tag{2}$$

$$S_2 = \overline{X} \tag{3}$$

$$S_3 = Y \tag{4}$$

$$S_4 = \overline{Y} \tag{5}$$

Fig. 2 shows the LSPWM switching scheme for phase A, including the pole voltage for phase A - V_{A0}, two carrier signals C_{R1}, C_{R2}, one sinusoidal modulation signal S_M, two Boolean signals X, Y, and four switching signals for phase A, i.e., S_1, S_2, S_3, and S_4.



(a) (b)

Fig. 2. The LSPWM switching scheme for the proposed converter. (a) Switching patterns for phase A. (b) Block diagrams for the Boolean operations.

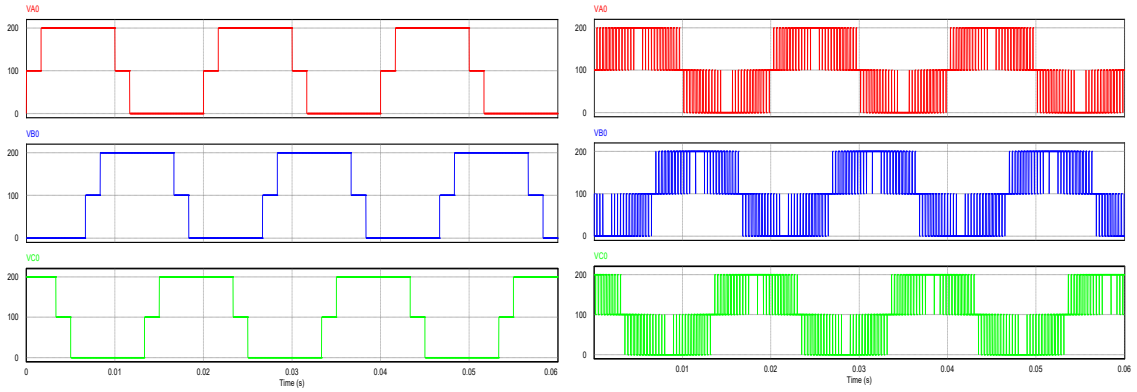
V. Simulation Results and Discussions

To illustrate the working principles of the proposed topology, a three-level model is designed and simulated not only for a fundamental frequency modulation but also for a pulse width modulation technique. The simulated model uses two symmetrical DC voltage sources and twelve switches (nine of E volt and three of 2E volt) to produce a three-level pole voltage. Table III provides the main simulation parameters, while the PSIM software has been used for obtaining the simulation results.

Fig. 3 shows the pole voltages V_{A0}, V_{B0}, and V_{C0} when the proposed converters are modulated by SCM and LSPWM switching schemes. By keeping the voltage across pole terminals have three steps and a phase shift of 120°, five-level balanced three-phase line voltages V_{AB}, V_{BC}, and V_{CA} will be generated at the load terminals as shown in Fig. 4. Fig. 5 shows the simulated results for the proposed topology when supplying power to a resistive-inductive load with a power factor of 0.9.

TABLE III. Simulation System Main Specifications

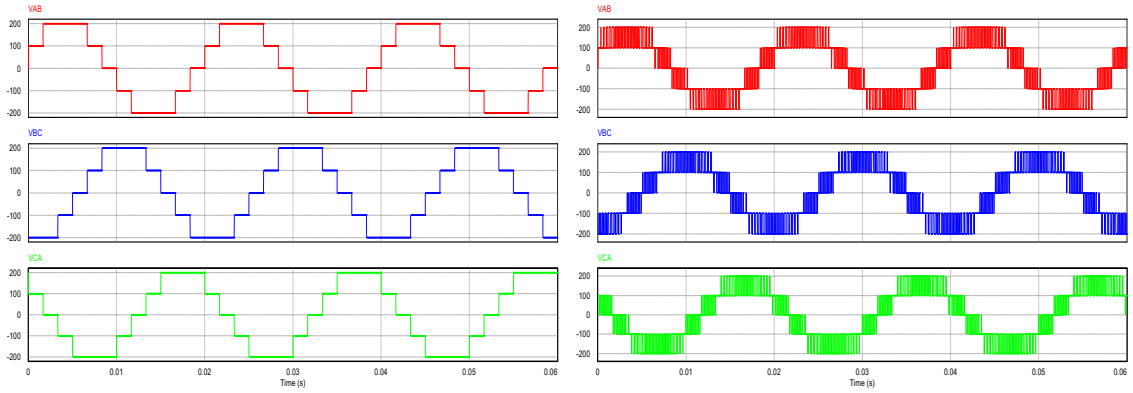
System parameters	**Value**
DC voltage value E	100 V
Load value at 50 Hz	R= 50 Ω, X_L= 23.6 Ω
Switching Frequency F_s	2.5 kHz
Modulation index Mi (= Sin_M / C_{RM})	1



(a) (b)

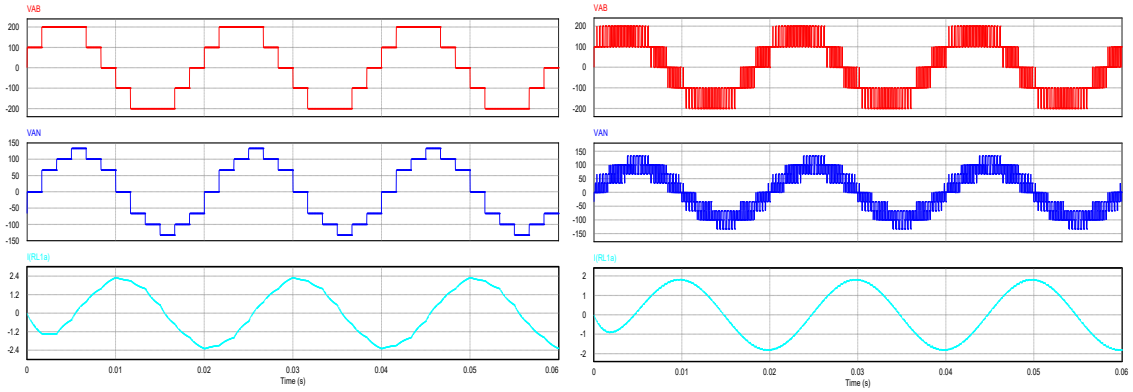
Fig. 3. The pole voltage waveforms: V_{A0}, V_{B0}, and V_{C0}. (a) staircases modulation. (b) Level-shifted PWM.

By comparing the two graphs for V_{AN} in Fig. 5 (a) and (b), it can be seen that the voltage level number is different consistent with the applied switching scheme. V_{AN} has seven levels of -4/3 E, - E, -2/3 E, 0, 2/3 E, E, 4/3 E for SCM and nine levels of -4/3 E, - E, -2/3 E, -1/3 E, 0, 1/3 E, 2/3 E, E, 4/3 E for LSPWM. The two extra voltage levels in V_{AN} ±1/3 E are generated because of two new voltage combinations in the pole voltages when using LSPWM switching scheme. Table IV and (6) [25] provide more clarification regarding the effect of switching schemes on the phase voltage level number.



(a) (b)

Fig. 4. The output line voltage waveforms: V_{AB}, V_{BC}, and V_{CA}. (a) Staircases modulation. (b) Level-shifted PWM.



(a) (b)

Fig. 5. The output waveforms under R-L load: V_{AB}, V_{An}, and I_{An}. (a) Staircases modulation. (b) Level-shifted PWM.

TABLE IV. THE SWITCHING MODULATION EFFECTS ON THE NUMBER OF LEVELS OF THE PHASE VOLTAGE V_{AN}

V_{A0}		V_{B0}		V_{C0}		V_{AN}	
SCM	LSPWM	SCM	LSPWM	SCM	LSPWM	SCM	LSPWM
2E	2E	0	0	0	0	4/3 E	4/3 E
2E	2E	E	E	0	0	E	E
2E	2E	2E	E	0	E	2/3 E	2/3 E
–	E	–	E	–	0	–	1/3 E
E	E	2E	2E	0	0	0	0
–	E	–	2E	–	E	–	-1/3 E
0	0	2E	2E	0	0	-2/3 E	-2/3 E
0	0	2E	2E	E	E	-E	-E
0	0	2E	2E	2E	2E	-4/3 E	-4/3 E

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \times \begin{bmatrix} V_{A0} \\ V_{B0} \\ V_{C0} \end{bmatrix} \quad (6)$$

VI. CONCLUSION

A new three-level multilevel inverter is proposed and analysed in this study. The proposed topology can generate a three-level pole voltage without using any passive component. Further, it requires a low component count as compared to other existing three-level topologies. Two modulation strategies based on fundamental frequency modulation and sinusoidal pulse width modulation are effectively applied for producing three balanced three-phase output voltages. The effectiveness of the proposed topology is verified via a simulation model of the circuit and resistive-inductive load. Moreover, a comparative study is carried out to highlight the advantage of the proposed circuit and provide a view on the design trade-off and selection of suitable multilevel converter topologies.

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Paper IV:

Novel Three-Phase Multilevel Inverter with Reduced Components for Low- and High-Voltage Applications

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Novel Three-Phase Multilevel Inverter with Reduced Components for Low- and High-Voltage Applications

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***Abstract*—This paper presents a novel multilevel topology for three-phase applications, having three-level and hybrid N-level modular configurations, enabling low-, medium-, and high-voltage operations. The proposed topology has several attractive features, namely reduced component count, being capacitor-, inductor-, and diode-free, lowering cost, control-complexity, and size, and can operate in a wide range of voltages and powers. Selected simulation and experimental results are presented to verify the performance of the proposed topology. Further, the overall efficiency of the topology and loss distribution in switches are studied. Finally, the key features of the proposed topology in terms of component count, blocking voltage, and DC-link requirements are highlighted via a comparative study.**

Index Terms—DC-AC power converters, low-frequency modulation, multilevel inverters, pulse width modulation.

I. INTRODUCTION

Multilevel inverters (MLIs) have played a key role in modern DC-AC converters or energy conversion systems due to their attractive features of modularity, high switching redundancy, voltage scalability, low harmonics contents in output waveforms and low dv/dt stress [1-22]. These features make MLI-based DC-AC systems having low total harmonic distortion (THD), low filter requirements, low electromagnetic interference (EMI), high-voltage high-power capacities, fault-tolerant operation, and utilising low-voltage switches for high-voltage applications. However, MLIs suffer from complex control strategies and high component count, resulting in high cost, bulky size, reduced efficiency and reliability. Three conventional MLI topologies, namely cascaded H-bridge (CHB) MLI [23], neutral point clamped (NPC) MLI [24], and flying capacitor (FC) [25] have been a baseline for research and development of MLIs over past decades. Reducing total component count and simplifying the control requirements by reducing active switches and flying capacitor count have been attractive topics to lower required sensors and sophisticated gate drivers or reduce the size and cost of the converters [1-12]. Configurations, advantages, and disadvantages of these recently developed circuits are highlighted hereafter, and more details can be found in [1-12].

The authors in [1] presented a capacitor-based three-level unit, consisting of three switches, two capacitors, and four diodes, being repeated for generating higher voltage levels. In each unit, the DC source is used for charging the two capacitors, and never directly connected to the load. Consequently, the voltage levels across the unit terminals are 0, V_{C1}, and V_{C2}, where V_{C1} and V_{C2} are the voltage across the two capacitors, and each of them is equal to half of the DC source voltage. The main merits of this structure are summarized as low switch count, medium voltage stress across the semiconductor components, symmetrical and asymmetrical operation capabilities, generating both positive and negative voltages without a polarity changer, and low count of switches in the current paths. However, the topology requires four power diodes and two capacitors per each unit, resulting in negative effects on size, cost, and lifetime of the inverter.

To address the problem of using capacitors in [1], the authors in [2] presented a capacitor-free circuit, integrating the conventional half-bridge (HB) with a new two-level structure to construct a three-phase MLI. This design can generate N voltage levels by increasing the number of connected HB cells in cascade. The two-level structure consists of three modified full H-bridge (MFHB) and one main DC source of V_M. The output voltages of this structure are limited by only two levels of 0 and the maximum voltage V_M. Each MFHB has eight semiconductor devices (four diodes and four switches) connected in parallel with the main DC source. The cascaded HB part is used for generating any voltage level between 0 and V_M, in which one HB is needed for each level, i.e. one DC source and two switches. This topology has features of a reduced component count, being inductor-, capacitor-free, and extendable for producing N levels. Further, the DC sources in HB stage can be isolated or non-isolated, simplifying the realisation of these sources. On the other hand, its main disadvantages include using several power diodes and DC sources, resulting in high losses and cost. Further, significant voltage stress across all semiconductor devices in the two-level structure due to extra HB cells. Such drawbacks restrict the topology's voltage level number and reduce its reliability, especially in high-voltage applications.

Hybrid MLIs, requiring multiple DC sources like the presented topologies in [1, 2], were reported and discussed in [3, 4, 6]. The topologies in [3, 4] have similar structures with two stages, high-frequency stage (HFS) and low-frequency stage (LFS). The HFS is responsible for generating both zero- and positive-voltage levels, being called as a level generator (LG), while LFS is used to change the polarity every half cycle to produce bipolar output voltages, being called as a polarity changer (POCH). In these topologies, a full H-bridge is used as a POCH while HB or switched-diodes (SD) cells are used to construct the LG stage. The SD's cell is formed by one DC source, one switch, and one diode, saving one switch as compared to the HB with the same number of DC sources, but it requires one diode for each cell. Many isolated DC sources and twelve high-voltage switches are required in the second stage, i.e. the POCH, in which their voltage rating is a function of the cell number in the LG stage. Accordingly, the presented topologies have a high loss in the second stage, restricting them to be used in low-voltage applications alone, for example, in PV farms, where implementing a high number of isolated DC sources becomes easier. Structure simplicity, capacitor- and

inductor-free features, operating in both symmetrical and asymmetrical modes, and reduced component count are the key advantages of these MLI topologies. To reduce high-voltage switches in [3, 4], the authors in [5] presented a topology using two switches for changing the polarity instead of four switches. Although the topology in [5] requires the same number of DC sources like the topologies in [3, 4], it needs six capacitors, increasing the footprint and control complexity of the converter.

Towards both low- and high-voltage applications, the authors in [6] presented a three-phase hybrid MLI configuration, consisting of three units: two-level three-phase VSI, three single-phase three-level FHB and three two-level HB. The authors suggested that repeating the second unit increases the voltage levels. Generating three levels in the topology would need four DC sources and twelve switches. Modularity is the key feature of this topology, so high voltages can be obtained without increasing the voltage stress across switches, making the topology suitable in high-voltage high-power applications. However, requiring many isolated DC sources and high switch count in the conduction paths are its main drawbacks.

To avoid using multiple DC sources, single-source topologies like T-type and NPC MLIs were proposed to use as three-level inverters [9]. Due to the lower count of power electronics components in the current paths, the T-type MLI has a lower conduction loss than NPC. For example, any positive or negative voltage level in the T-type inverter needs only one switch in the current path while two switches are required in case of NPC regardless of the voltage level. However, the switching loss in NPC is lower than that in T-type because the switch blocking voltages of the NPC are lower than those in the unidirectional switches of T-type MLI [9] as well explained in [26, 27]. The authors in [7-9] presented modified circuits to overcome some drawbacks of both T-type and NPC MLIs. The modified circuit in [7] reduces the switch count to nine instead of twelve in the conventional T-type MLI. However, it requires twelve diodes, two capacitors and one DC source for generating three voltage levels. The designed circuit is only applicable to low-voltage applications as the main six switches block the full DC-link voltage, like conventional T-type inverters. Although the count or number of switches is reduced, the total power electronics components are increased in the current path, resulting in a high conduction loss. A diode-free T-type MLI, using 18 switches, two capacitors, and one DC source, is presented in [8] as a solution of reducing conduction losses of the topology in [7], but it doubles the switch count. The presented topology uses only active switches, removing the power diodes from the bidirectional-switch structures in [7]. Accordingly, zero-vector current paths will not involve any power diode, reducing the conduction losses. As compared to T-type MLIs, NPC inverters have a higher uneven loss distribution among power electronic components or unequal junction temperature rises, reducing the switching frequency and power rating of the converter [9, 28]. To solve the mentioned problems, the authors in [9] presented a hybrid active neutral point (hybrid-ANPC) topology, generating three voltage levels by using three legs of six switches, two capacitors, and one DC source. Despite increasing the power

density, the proposed topology requires a higher count of switches and gate drivers' circuits than those in the conventional NPC MLIs.

The mentioned MLI configurations use complementary switches, causing shoot-through problems or reducing the circuit reliability. Implementing a dead-time through hardware or software is to avoid the shoot-through, but might distort the output waveforms and increase the converter losses due to the poor characteristics of freewheeling diodes [29]. To overcome these issues, a family of dual-buck MLIs (DB-MLIs) is presented in [10], aiming to split each leg into two new legs formed by diodes and switches. These legs are connected through a coupled inductor network for forming phase voltages. Additionally, three diodes are required to link each phase to the DC-link. The presented topology has two DC ports for connecting low- and high-voltage sources at the same time, allowing for using two renewable energy sources (RESs) with different output voltages. In case of using a single low-voltage DC source, a boost converter (BC) is required to implement the high-voltage source. The BC is bypassed based on the instantaneous AC output voltage value. The presented topology requires nine switches, nine diodes, two isolated DC sources, and three coupled inductors, resulting in a converter with a bulky size, high cost, and low efficiency. Other two asymmetrical MLIs with dual DC-ports are presented in [11], which are based on NPC, and T-type configurations. Using the same DC-link structure for the dual-DC port MLI in [10] allows them to feed power to a load from low- and high-voltage DC sources. Both configurations in [11] require extra three switches but do not use any coupled inductor to produce the same number of voltage levels in [10]. Further, the T-type-based configuration does not need any diode while NPC-based configuration needs three additional diodes. Unlike the topology in [10], a dead-time is recommended to be used in [11] for avoiding short-circuit faults.

The above review of the recently developed multilevel inverters proves that the existing MLIs are still bulky due to a high number of components, and restricted by voltage level applications, namely low or high voltage level alone. An initial study of a novel three-level MLI with a reduced component count was presented in [30] based on simulation results. This manuscript details the low-voltage configuration of the previous work and presents a new *N*-level hybrid configuration for high-voltage applications. Further, the switching algorithm for low-frequency modulation (LFM) is modified in order to control the RMS value, level count, and frequency of the output voltage online. Additional simulation results are presented for both configurations. Within this framework, the proposed low-voltage configuration is experimentally validated through an in-house test setup. Finally, the key features of the proposed topology are proven via a comparison with other topologies in [1-12].

II. The Proposed Multilevel Inverter

In this section, the circuit description and switching schemes of the proposed topology are introduced and discussed in detail.

A. CIRCUIT DESCRIPTION

The low-voltage configuration of the proposed topology is shown in Fig. 1, which is a transformerless MLI and does not require any flying capacitor (FC), or power diode or coupled inductor (CI) in its operation, allowing for a high-efficiency and compact design. Each phase consists of only four switches, being distinctively connected for constructing a three-level unit. Further, to reduce the DC source count, the three-phase legs share the same DC-link. The DC-link is formed by connecting two symmetrical DC sources of E in series. However, these DC sources can be replaced by batteries or AC voltage sources followed by rectifiers or different RESs, e.g. PV strings and fuel cells.

Twelve power switches S_1 to S_{12} are used to create different paths from the two DC sources to the load. Therefore, the DC sources can be arranged in different ways for producing five levels $2E$, E, 0, $-E$, and $-2E$ in the line voltage. For example, when S_1, S_6, S_8, and S_9 are in ON-state, and the remaining switches are in OFF-state, the line voltages V_{AB}, V_{BC}, and V_{CA} are equal to $2E$, $-2E$ and 0, respectively. Fig. 2 shows the switching modes for the proposed circuit when producing five voltage levels in the line voltage V_{AB}, along with the conduction paths for the forward and reverse currents in red and blue lines, respectively. These switching modes have been selected in a way to prevent any appearance of a positive voltage across built-in diodes of the switches. As a result, the DC sources are protected from short-circuit faults. Further, for the same reason, some selected switching states are removed from the control algorithms of the inverter. For example, in phase A, (S_1-S_3), (S_1, S_2, S_4) and (S_3, S_4) cannot be in ON-state at the same instance.

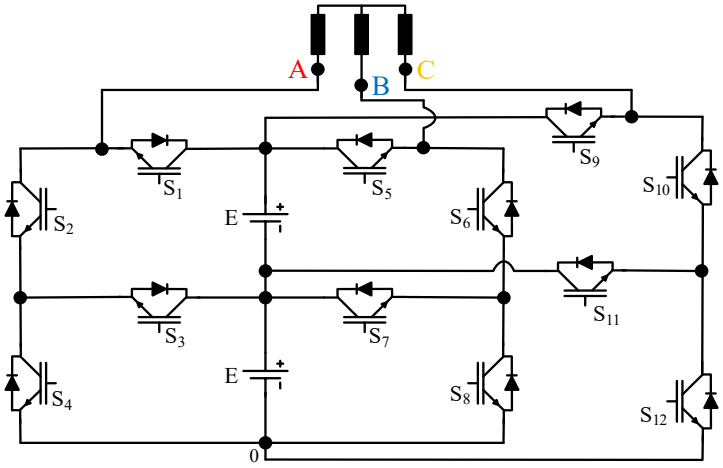

Fig. 1. Low-voltage three-level configuration of the proposed topology.

In addition to the low-voltage configuration of the proposed inverter, the N-level hybrid configuration for high-voltage applications is proposed as shown in Fig. 3, using the three-level configuration as a fixed stage and a new three-phase module as a repeated stage. Each module has three basic cells or one cell for each phase. Each basic cell requires eight switches and two DC sources. It can produce five voltage and seven voltage levels for symmetrical and asymmetrical DC sources, respectively. As shown in Fig. 1, the basic cell is formed by using the DC-link and either (leg A + leg B) or (leg B + leg C) or (leg C + leg A), this is the two-phase

version of the fixed stage. The basic cell is formed in a way to allow it to be used in the two proposed configurations, reducing manufacturing, maintenance, voltage upgrading cost and time.

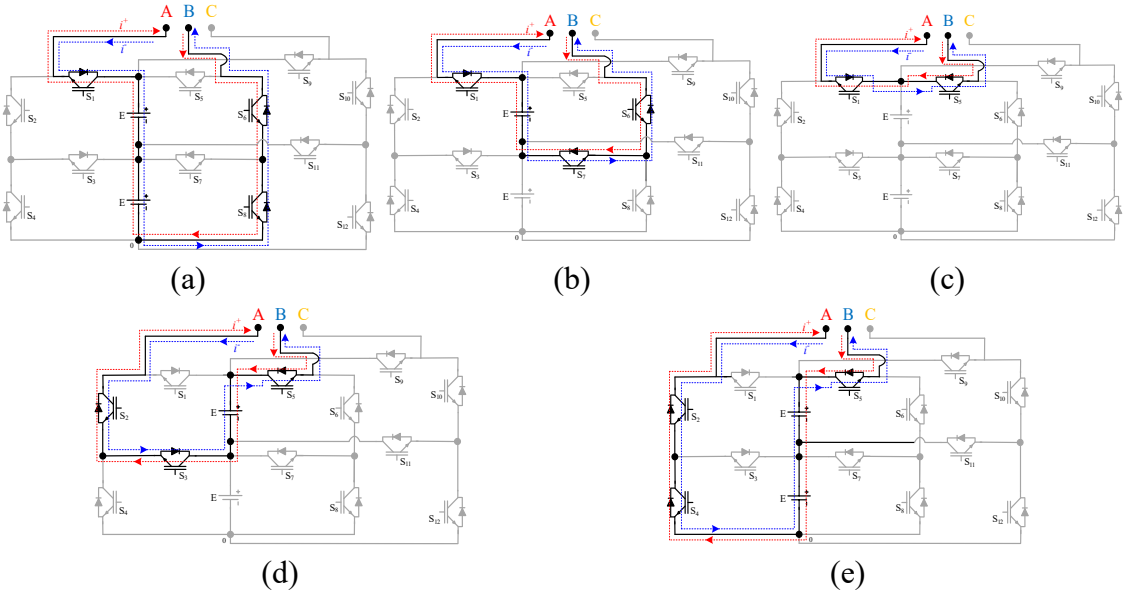

Fig. 2. The switching modes for the low-voltage configuration. (a) $V_{AB} = 2E$. (b) $V_{AB} = E$. (c) $V_{AB} = 0$.(d) $V_{AB} = -E$. (e) $V_{AB} = -2E$.

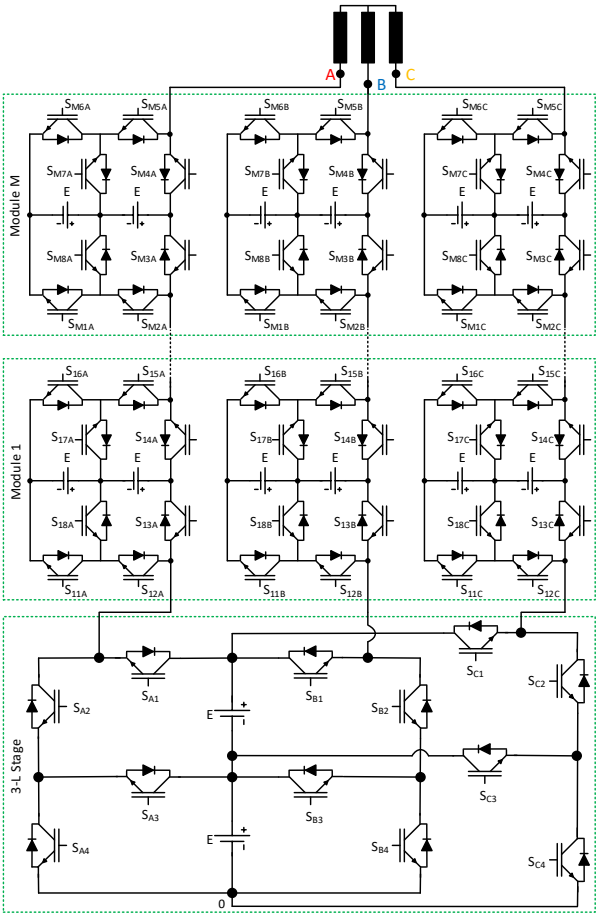

Fig. 3. *N*-level high-voltage configuration of the proposed topology.

In the hybrid configuration of the proposed topology, the voltage levels can be enlarged to N levels without increasing the voltage stress across the switches due to the modularity feature. The counts of the three-phase modules M, switches N_{SW}, and DC sources N_{DC} in term of voltage levels N, are presented in (1) - (3). For producing seven levels in the pole voltage, only one module is needed as calculated in (1). Consequently, eight symmetrical DC sources and thirty-six switches are required according to (2) and (3), respectively.

$$M = 0.25N - 0.75 \tag{1}$$

$$N_{DC} = 1.5N - 2.5 \tag{2}$$

$$N_{SW} = 6N - 6 \tag{3}$$

It is worth mentioning that the switch count for each module can be reduced to eighteen instead of twenty-four switches. This can be obtained by merging the three switches S_{M5A}, S_{M6A}, and S_{M7A} in each basic cell to be one switch and changing the switching algorithm a little bit. For example, in the first module (i.e. $M = 1$), S_{15A}, S_{16A}, and S_{17A} can be merged to be one switching device with a higher blocking voltage ($2E$ instead of E). Accordingly, the total number of required switches could be reduced, as calculated in (4) for symmetrical operation.

$$N_{SW} = 4.5N - 1.5 \tag{4}$$

B. MODULATION STRATEGIES

The low-voltage configuration as shown in Fig. 1 has 64 switching states, but only twelve states are required and summarized in Table I, being used in the switching algorithms for two modulation techniques. These twelve switching states are selected in a way to prevent any switching paths to form a closed loop for the DC sources. Further, to reduce the conduction losses, reducing the count of ON-switches in the conducting path for each level was taken into consideration when selecting these switching states. Table I shows that the switching states of S_3 and S_4 are labelled with 'X' letter for producing $2E$ in pole A. 'X' letter means these switches can be either in ON- or OFF-state, but the switching cycles are minimised to reduce the switching loss. For this reason, the switching algorithms were designed to keep the same previous states of S_3 and S_4 to be their new switching states, i.e. X-state will be ON if the previous state was ON, and vice versa. For example, in S_4, the previous switching state was OFF, so the new state is selected to be OFF.

Fig. 4 shows the switching patterns for the LFM and highlights the three-pole voltage waveforms V_{A0}, V_{B0}, and V_{C0}. The LFM uses three rectified sinusoidal waveforms with amplitudes of 1. These waveforms are compared to two signals, 'Zero-reference' and a proposed modulator signal (called as H), to generate L_1-L_6. The value of the modulator signal H can be varied from 0 to 1 for obtaining different numbers of voltage levels. Therefore, the proposed modulator H adds more flexibility for the online control of both level number and root mean square (RMS) value of the output voltages. Implementing Boolean operations on L_1 and

L_2, as described in (5)-(6), results in the switching signals for phase A. For phases B and C, the procedures are similar except a phase-shift of 120°.

TABLE I
SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGE OF PHASE A (X: ON OR OFF)

V_{A0}	S_1	S_2	S_3	S_4
	Pole A			
E	OFF	ON	ON	OFF
2*E*	ON	OFF	X	X
2*E*	ON	OFF	X	X
2*E*	ON	OFF	X	X
2*E*	ON	OFF	X	X
2*E*	ON	OFF	X	X
E	OFF	ON	ON	OFF
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON

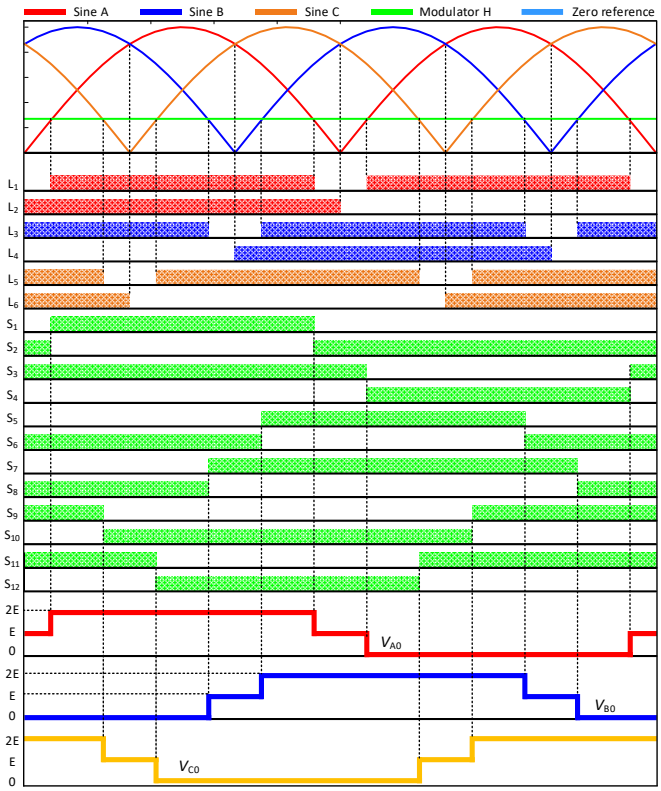

Fig. 4. LFM switching scheme for the proposed inverter.

$$\overline{S_1},\ S_2=\overline{L_1\times L_2} \tag{5}$$

$$\overline{S_3},\ S_4=L_1\times\overline{L_2} \tag{6}$$

Switching signals of the high-voltage configuration can be generated based on Table II, listing the full switching states for producing seven voltage levels. It shows twenty-seven states, seven primary states (written in blue) and twenty redundant states, providing some flexibility in the switching algorithms, balancing power losses of switches and increasing the reliability. The reason for selecting the seven primary states is to minimise the count of ON-switch in conduction paths and reduce the conduction losses. For example, six possible switching states can be used to produce a $2E$ level, but the second state with three ON-switches is selected and marked as a primary state, reducing the conduction losses by at least 40% when producing $2E$ since the other five states use either five or six ON-switches.

TABLE II
SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGE FOR SEVEN-LEVEL CONFIGURATION OF THE PROPOSED TOPOLOGY

V_{A0}	S_{A1}	S_{A2}	S_{A3}	S_{A4}	S_{11A}	S_{12A}	S_{13A}	S_{14A}	S_{15A}	S_{16A}	S_{17A}	S_{18A}
	Phase A, fixed stage				**Phase A in the first module**							
4*E*	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
3*E*	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF
	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
	OFF	ON	OFF	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
2*E*	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON
	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON
	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
E	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF
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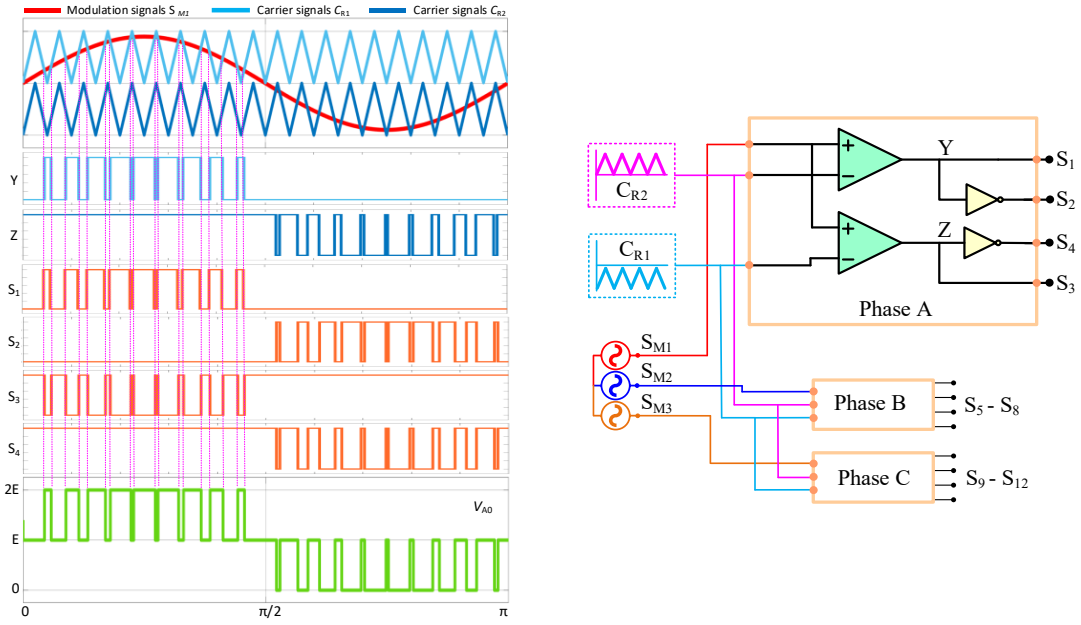
	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
E	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON
	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
-2*E*	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF

In addition to LFM, the LS-PWM scheme was implemented as shown in Fig. 5. Using two carrier signals C_{R1} and C_{R2} and three sinusoidal waveforms S_{M1}, S_{M2},

and S_{M3} generates the required switching pulses for the switches in the low-voltage configuration. The signals of S_{M1}-S_{M3} have the same magnitude and shape with a phase-shift of 120° among them. Fig. 5(a) shows the generation process of switching pulses for the four switches in phase A. The Y and Z signals are generated by comparing the S_{M1} with the two carrier signals. Afterwards, different Boolean operators are used for extracting the correct switching signals from Y and Z, as seen in Fig. 5(b). Similarly, the switching pulses for the high-voltage configuration can be generated based on Fig. 5, but the number of carrier signals is increased to six instead of two. Accordingly, six controlling signals labelled by X_1 to X_6 from top to down are generated by comparing the sinusoidal modulation signals with six carrier signals. The switching pulses of phase A are obtained by implementing the Boolean operations on the six controlling signals as summarised in (7)-(15).



(a) (b)

Fig. 5. LS-PWM switching scheme for the low-voltage configuration. (a) Key waveforms. (b) Switching logic.

$$S_{A1},\ \overline{S_{A2}}=X_3 \tag{7}$$

$$S_{A3}=\overline{X_3}\times X_4 \tag{8}$$

$$S_{A4}=\overline{X_4} \tag{9}$$

$$S_{11A}=X_1 \tag{10}$$

$$S_{12A},\ \overline{S_{13A}}=X_2 \tag{11}$$

$$S_{14A},\ \overline{S_{15A}}=X_5 \tag{12}$$

$$S_{16A} = \overline{X_6} \tag{13}$$

$$S_{17A} = \overline{X_5} \times X_6 \tag{14}$$

$$S_{18A} = \overline{X_1} \times X_2 \tag{15}$$

III. Simulation and Experimental Results

To verify the operating principles of the proposed circuit, both switching schemes are simulated in Matlab/Simulink and experimentally validated on a laboratory prototype. For building the low-voltage prototype, twelve insulated-gate bipolar transistors (IGBT) modules with built-in freewheeling diodes are used, in addition to two DC voltage sources. The complete in-house setup is captured and showed in Fig. 6. The digital controller -dSPACE MicroLabBox is used to implement the switching algorithms for both LFM and LS-PWM. Two primary DC sources are used for supplying the electrical power to the three-phase load through twelve IGBT modules SKM300GA12E4, in which each IGBT is controlled through a SKHI 10/12 R gate-driver board and attached to a heatsink for reducing the temperature of the IGBT's internal junction. Further, the test setup includes secondary devices such as low-power DC source for driver boards, oscilloscope, voltage- and current-probe. Table III lists specifications of the studied cases in simulations and experimental tests.

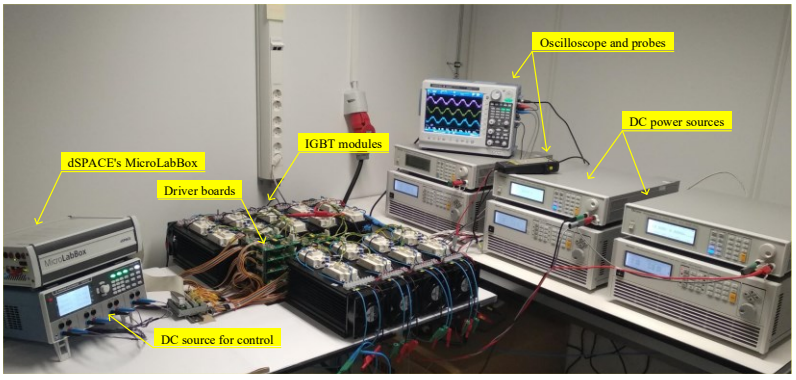
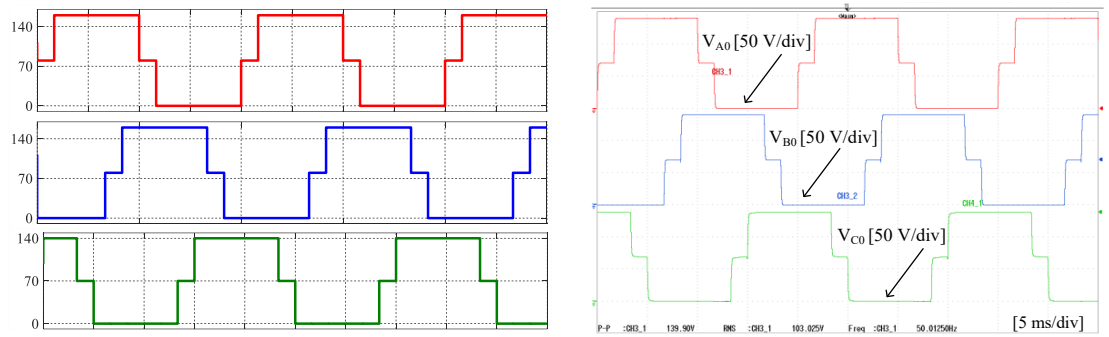


Fig. 6. The in-house experimental setup.

TABLE III
System Specifications and Used Components

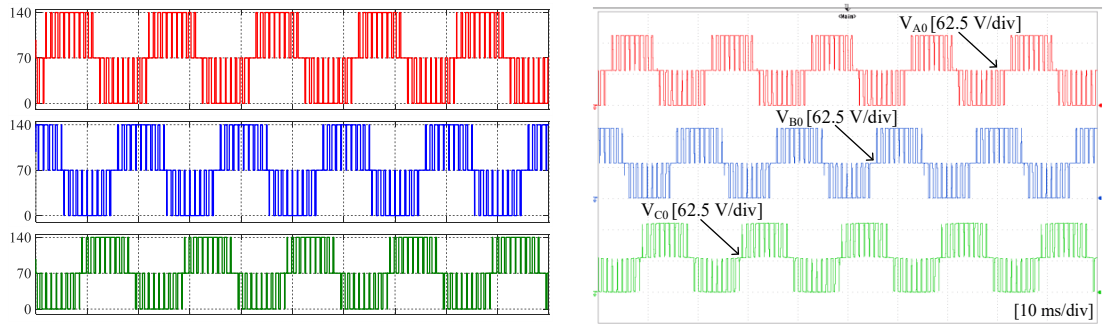
Description	Value/ Part number	Unit
DC voltage source (E)	70	V
Load R, X_L	30, 31.41	Ω
Carrier frequency (F_S)	1000	Hz
Modulation signal frequency (F)	50	Hz
Modulation index (M_I), LS-PWM	0.9	–
Modulator signal (H), LFM	0.27	–
Sampling time (T_S)	15	µs
Switching device	SKM300GA12E4	–
Gate-driver board	SKHI 10/12 R	–
DC voltage source	62024P-100-50	–

Figs. 7(a) and 8(a) show the simulation waveforms of the pole voltages V_{A0}, V_{B0}, and V_{C0} for LFM and LS-PWM, respectively. Each waveform has three voltage levels of 0, E, and $2E$, in addition to a phase-shift of 120° for the two other pole voltages. The waveforms of experimental tests are presented in Figs. 7(b) and 8(b), matching well the obtained simulation results in Figs. 7(a) and 8(a). In the experimental results, the 'voltage-per-division' setting was changed from standard values into flexible ones to make sure that the obtained results fit the oscilloscope screen. Figs. 9 and 10 depict the balanced three-phase line voltages V_{AB}, V_{BC}, and V_{CA}, where five voltage levels of $2E$, E, 0, $-E$, and $-2E$ were produced by maintaining the pole voltages in the same conditions as shown in Figs. 7 and 8, (i.e. three levels and phase-shift of 120°). A resistive-inductive (R-L) load is used to verify the performance of the proposed inverter under loading conditions. Figs. 11 and 12 illustrate the obtained results when using a load with a lagging power factor of 0.7. Further, Figs. 11 and 12 show the five-level line voltage V_{AB} in the first trace while the phase voltage V_{AN} and load current I_{AN} are shown in the second and third traces, respectively.



(a) (b)

Fig. 7. Pole voltages V_{A0}, V_{B0}, and V_{C0} for LFM. (a) Simulation. (b) Experimental.



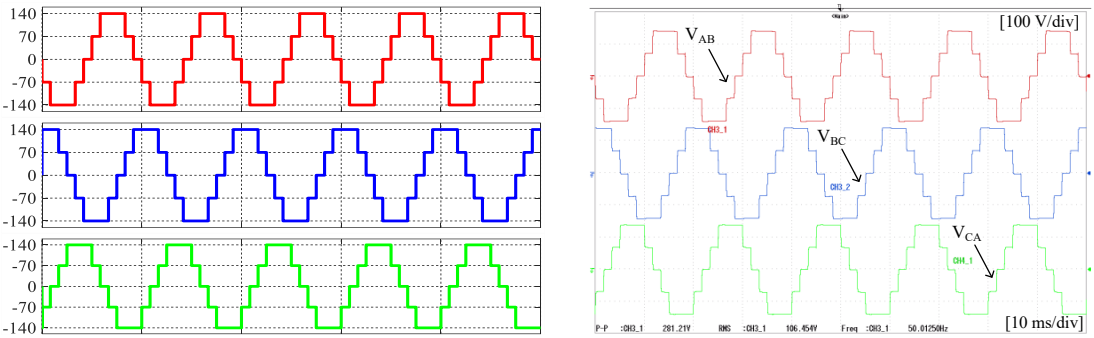
(a) (b)

Fig. 8. Pole voltages V_{A0}, V_{B0}, and V_{C0} for LS-PWM. (a) Simulation. (b) Experimental.

As observed from the second trace in Figs. 11 and 12, the phase-load voltage has seven levels of $-4/3E$, $-E$, $-2/3E$, 0, $2/3\ E$, E, and $4/3E$ under LFM, while nine levels of $4/3E$, $-E$, $-2/3\ E$, $-1/3E$, 0, $1/3E$, $2/3E$, E, and $4/3E$ are obtained under the LS-PWM control. The two extra levels come from the different pole voltage combinations for the two modulation schemes. Table IV shows a list of different combinations of voltage values across the poles of the proposed topology. In case of generating the switching pulses by using the LFM scheme, only seven voltage

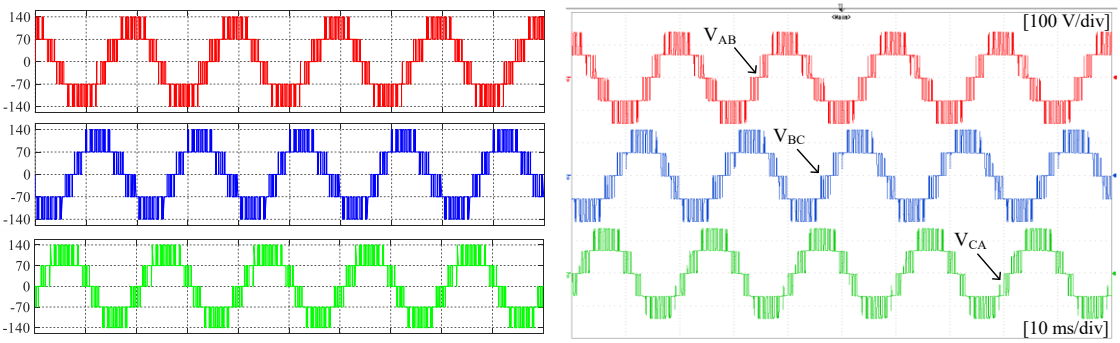
combinations can be achieved (*A*1-*A*3), *A*5, and (*A*7-*A*9), while nine voltage combinations (*A*1-*A*9) are obtained by using the LS-PWM scheme.

Although the LFM scheme uses lower frequency signals for generating the switching pulses, the LS-PWM switching scheme has a higher degree of flexibility. In the LS-PWM, the output voltage frequency, RMS value, and the number of levels can be controlled online by changing the frequency and magnitude of the modulation signal. In the LFM scheme, the proposed modulator *H* is integrated into the switching algorithm to add a degree of freedom for changing the output level count and RMS value while the frequency of the output voltage is changed in the traditional way using the sinusoidal modulation signals.



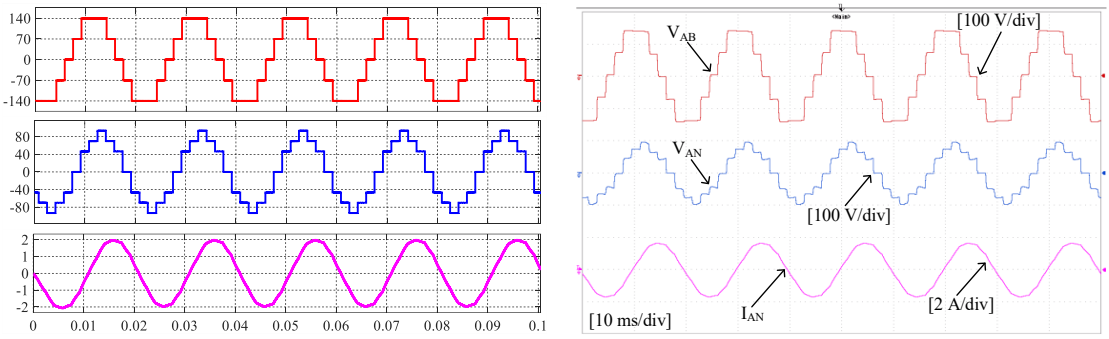
(a) (b)

Fig. 9. Line voltages V_{AB}, V_{BC}, and V_{CA} for LFM. (a) Simulation. (b) Experimental.



(a) (b)

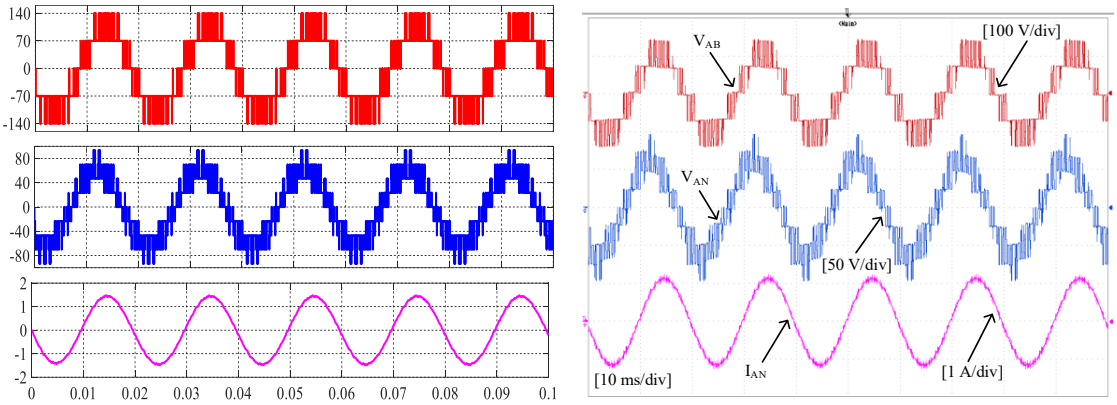
Fig. 10. Line voltages V_{AB}, V_{BC}, and V_{CA} for LS-PWM. (a) Simulation. (b) Experimental.



(a) (b)

Fig. 11. Obtained V_{AB}, V_{AN}, and I_{AN} for LFM. (a) Simulation. (b) Experimental.

Figs. 13(a) and (b) show the simulation and experimental output line voltage waveforms at different values of the modulator H. By changing H from 1 to 0, the RMS value of the line voltage is varied from 0% to 81.6% of the DC-link voltage. Further, the line voltage has zero-, three-, and five levels when H is 1, 0.9, and 0.2, respectively. Therefore, the proposed topology can produce the output voltage with variable magnitudes, frequency, and level counts for both the LS-PWM and LFM.

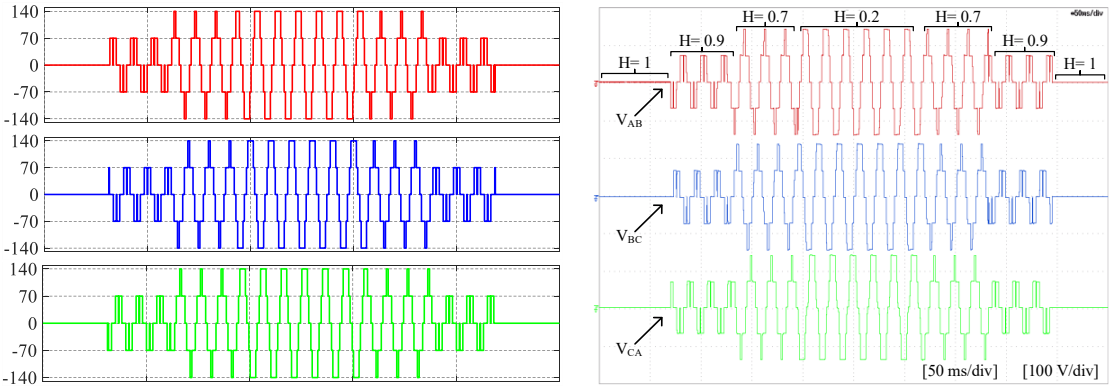


(a) (b)

Fig. 12. Obtained V_{AB}, V_{AN}, and I_{AN} for LS-PWM. (a) Simulation. (b) Experimental.

TABLE IV
POLE VOLTAGE COMBINATIONS FOR THE USED SWITCHING SCHEMES

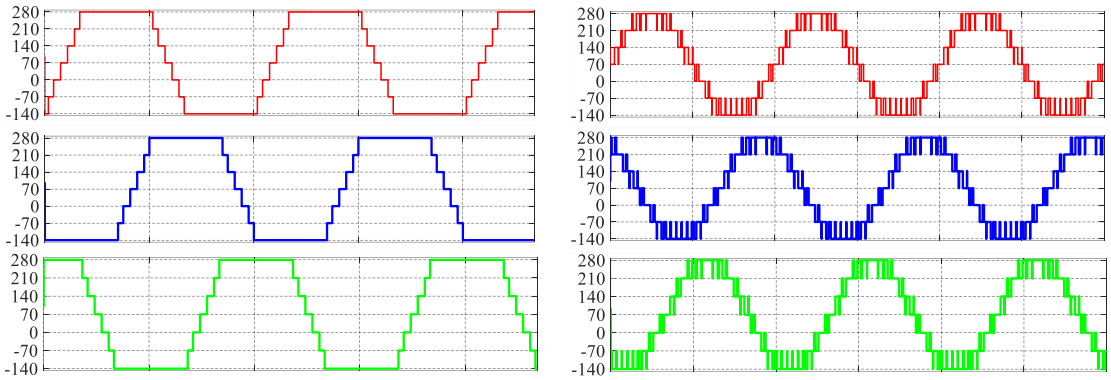
	LFM			LS-PWM			Phase voltage	
	V_{A0}	V_{B0}	V_{C0}	V_{A0}	V_{B0}	V_{C0}	LFM	LS-PWM
***A*1**	2*E*	0	0	2*E*	0	0	4/3*E*	4/3*E*
***A*2**	2*E*	*E*	0	2*E*	*E*	0	*E*	*E*
***A*3**	2*E*	2*E*	0	2*E*	2*E*	0	2/3*E*	2/3*E*
***A*4**	–	–	–	*E*	*E*	0	–	1/3*E*
***A*5**	*E*	2*E*	0	*E*	2*E*	0	0	0
***A*6**	–	–	–	*E*	2*E*	*E*	–	-1/3*E*
***A*7**	0	2*E*	0	0	2*E*	0	-2/3*E*	-2/3*E*
***A*8**	0	2*E*	*E*	0	2*E*	*E*	-*E*	-*E*
***A*9**	0	2*E*	2*E*	0	2*E*	2*E*	-4/3*E*	-4/3*E*



(a) (b)

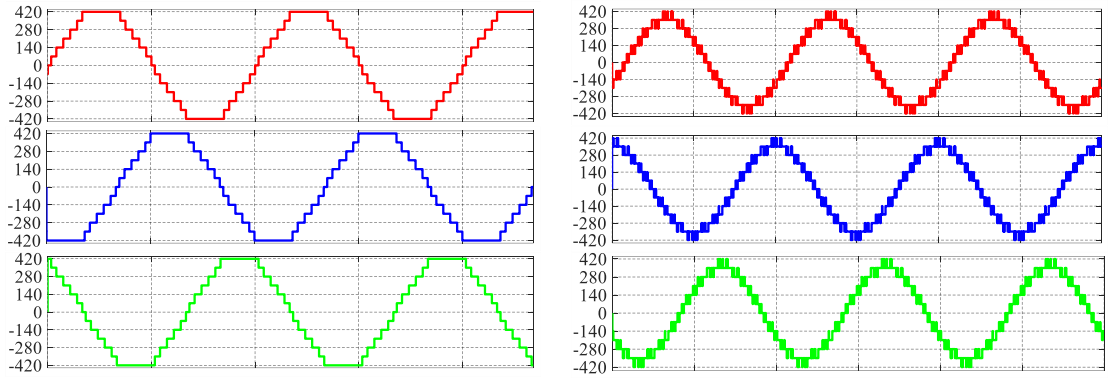
Fig. 13. Line voltages V_{AB}, V_{BC}, and V_{CA} for different values of H. (a) Simulation. (b) Experimental.

Some selected results for the hybrid configuration of the proposed topology depicted in Fig. 3 are shown in Figs. 14, 15 and 16 when the fixed stage and one repeated module are used for feeding power to an R-L load (R=50 Ω, L=100 mH) under LFM and LS-PWM, respectively. By using one module cascaded with the fixed stage, seven levels of -2E, -E, 0, E, 2E, 3E, and 4E can be produced in the pole voltage V_{A0} while thirteen levels of -6E, -5E, -4E, -3E, -2E, -E, 0, E, 2E, 3E, 4E, 5E, and 6E are generated in the line voltage V_{AB}.



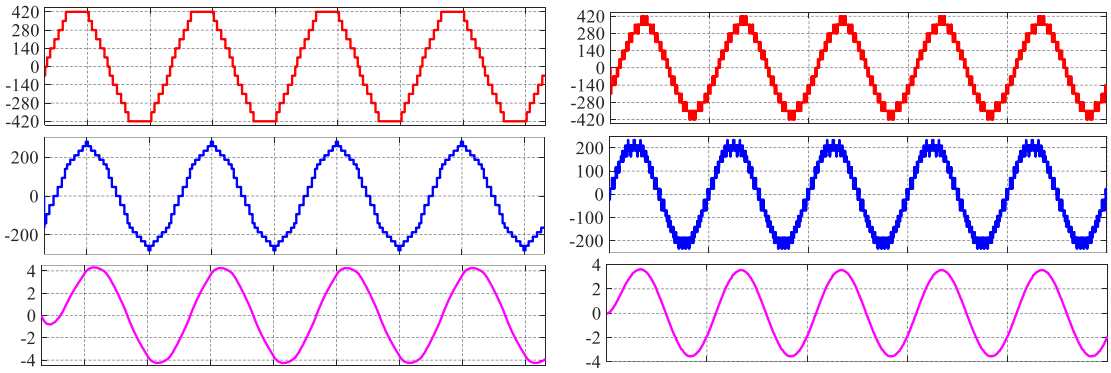
(a) (b)

Fig. 14. Pole voltages V_{A0}, V_{B0}, and V_{C0}. (a) LFM. (b) LS-PWM.



(a) (b)

Fig. 15. Line voltages V_{AB}, V_{BC}, and V_{CA}. (a) LFM. (b) LS-PWM.



(a) (b)

Fig. 16. Obtained waveforms of V_{AB}, V_{AN}, and $I_{A.}$ (a) LFM. (b) LS-PWM.

IV. Power Losses and Efficiency Analysis

The power losses in semiconductor devices are classified into three categories according to the operating state of the device: A) OFF-state losses, B) ON-state or conduction losses, and C) changing-state or switching losses [31-33]. Due to the nonideality characteristics of switches, a leakage current is following through switches during OFF-state, causing OFF-state power losses. The OFF-state losses can be neglected in most cases since leakage currents are insignificant during OFF-state [31]. During the ON-state, the switches have non-zero ON-state voltage (V_{on}) and ON-state resistance (R_{on}), causing power losses. The ON-state losses depend on V_{on}, R_{on}, load current and the switch duty cycle [33]. The transitions, from OFF- to ON states and vice versa, cannot occur instantaneously. In those transition periods, the flowing current and voltage across the device result in a large instantaneous loss or dissipated energies, which are termed as turn-on energy (E_{on}) and turn-off energy (E_{off}) for IGBTs, and reverse recovery energy (E_{rec}) for diodes. The switching losses are directly proportional to the switching frequency and blocking voltage of the devices [31, 32, 34]. More details on calculating the switching and conduction losses can be found in [31-34].

The efficiency of the proposed topology and the losses distribution in the switches are analysed based on a PSIM software model, considering the actual working condition of the IGBT modules. The required parameters of IGBTs are obtained from data sheets provided by component manufacturers. The IGBT modules are assumed to be working at a junction temperature of 150° C. Table V shows the system specifications and the parameters of used IGBT modules. The IGBT module has a part number of SKM300GA12E4, which is medium-fast trench IGBT in conjunction with a soft-switching controlled axial lifetime (CAL) freewheeling diode.

The loss distribution of different switches is shown in Fig. 17, where the losses are divided into conduction losses (P_{con}) and switching losses (P_{sw}). The conduction period and blocking voltage of the switch have the main effects on the conduction losses and switching losses when the switching frequency and load are kept constant (Fs =5 kHz and P_{out} = 4 kW). For example, S_1, S_5, and S_9 have voltage stresses of 2E, so their switching losses are higher than the other switches. On the other hand, S_2, S_6, and S_{10} have the highest conduction losses because their conduction durations are the longest among switches. Fig. 18 shows that the switching frequency significantly affects switching losses, but it has a small impact on the conduction losses.

The performance of the proposed topology is investigated by changing the switching frequency and load while keeping all other variables constant. Fig. 19 shows the efficiency variation when increasing the load from 10% to a full load of 4 kW in steps of 10% at the switching frequency of 5 kHz. The efficiency increases from 95.89% to 99.06% when the load is increased from 10% to 100% of the rated power. On the other hand, Fig. 19 also shows the effect of increasing the switching frequency from 1 kHz to 10 kHz on the converter efficiency at full load. The efficiency decreases from 99.35% at 1 kHz to 98.71% at 10 kHz.

TABLE V
SYSTEM SPECIFICATIONS FOR THE LOSS ANALYSIS

Parameter/Specification	Value	Unit
Collector-emitter breakdown voltage (V_{CE})	1200	V
Collector-emitter on-state voltage ($V_{CE,\ on}$)	2.45	V
Collector-emitter voltage at zero current ($V_{CE,\ I=0}$)	0.8	V
IGBT on resistance ($R_{CE,\ on}$)	5.5	mΩ
Input capacitance (C_{ies})	17.6	nF
Output capacitance (C_{oes})	1.16	nF
Reverse transfer capacitance (C_{res})	0.94	nF
Turn-on delay time ($T_{d,\ on}$)	220	ns
Rise time (T_r)	51	ns
Turn-off delay time ($T_{d,\ off}$)	515	ns
Fall time (T_f)	105	ns
Turn-on switching energy (E_{on})	23.4	mJ
Turn-off switching energy (E_{off})	35	mJ
Reverse recovery energy (E_{rec})	22.2	mJ
Forward voltage (V_f)	2.42	V
Forward voltage at zero current (V_{f0})	1.1	V
Diode on-resistance (R_{on})	4.4	mΩ
Junction temperature (T_j)	150	°C
Switching frequency (F_s)	5	kHz
Modulation index (M_I)	0.9	-
Power factor (PF)	0.877	-
Input DC sources (E)	500	V
Rated output power (P_{out})	4	kW

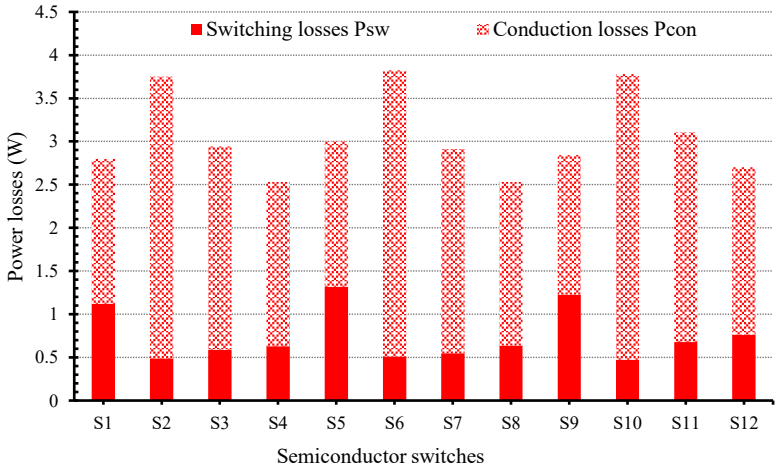


Fig. 17. Loss distribution in various switches at the rated power and switching frequency of 5 kHz.

V. THE COMPARATIVE STUDY

In this section, a comparison between the proposed topology and the recently reported multilevel topologies in [1-12] is carried out to highlight the key features of the proposed circuit. The compared topologies are labelled with T_A to T_S, which

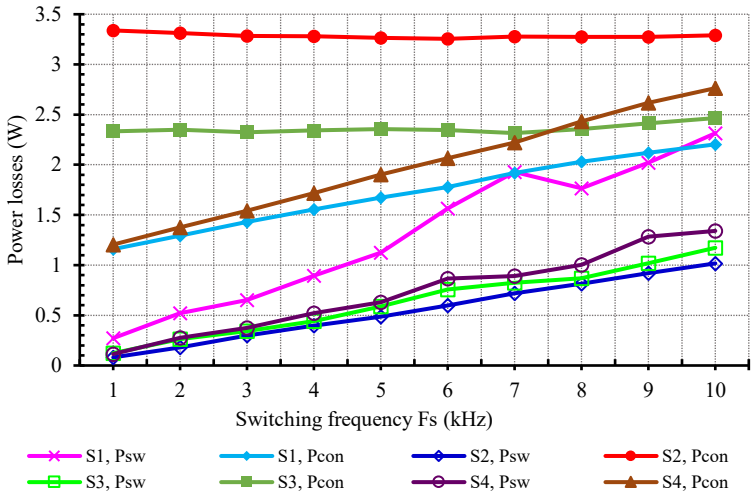


Fig. 18. Effects of switching frequency on the power losses of switches (phase A) at the rated power.

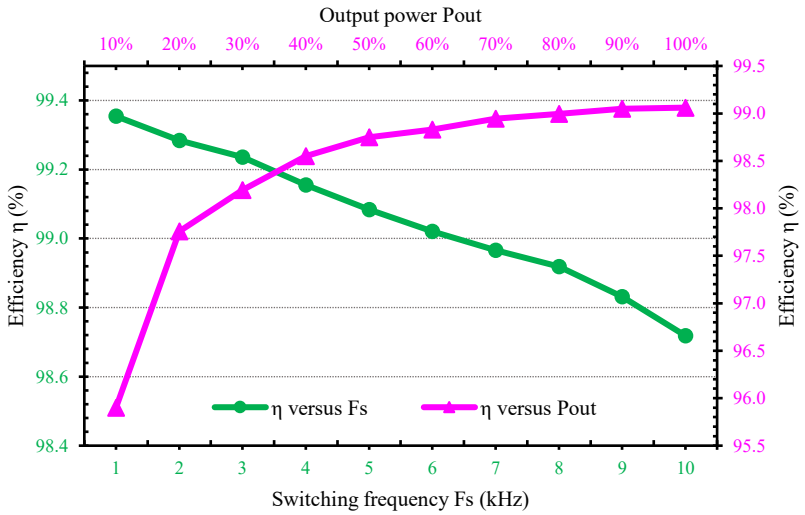


Fig. 19. Efficiency at different loads and switching frequencies.

are ordered in a descending manner in terms of the required number of components. Merits and demerits of each topology were discussed in Section I. Table VI lists the component counts for three-phase configuration of the addressed topologies, including DC source count N_{DC}, switch count N_{SW}, power diode count N_D, inductor count N_L, and capacitors count N_C. Further, 'component per level factor (CLF)' is used to calculate the required components for producing one voltage level [35].

Some assumptions are used in the comparison study: A) the number of levels N is equal to three for the pole voltage and five for the line voltage, B) all mentioned topologies are set to be in three-phase configurations, C) the unidirectional switch is the counting unit for switching devices, i.e. each bidirectional switch was disassembled into its primary parts, D) the built-in/freewheeling diodes are not included for calculating the diode count N_D, E) the coupled-inductor is counted as one inductor, F) the capacitor count N_C includes only the flying capacitors, while the DC-link capacitors for single-source MLIs are replaced by DC sources (i.e. the

DC-link structures are unified for all single-source MLI, in the form of two DC sources in series instead of one DC source divided by two capacitors into two equal parts).

TABLE VI
SUMMARY OF THE COMPARISON STUDY AMONG THE PROPOSED TOPOLOGY, THE MLIS IN [1-12] AND THE CONVENTIONAL MLIS IN TERMS OF COMPONENT COUNT AND DC-LINK VOLTAGE REQUIREMENTS

Topology	N_{DC}		N_{SW}				N_D		N_L	N_C	**CLF**
	E	***2E***	***0.5E***	***E***	***1.5E***	***2E***	***E***	***2E***		***E***	
T_A In [1]	0	3	0	3	0	6	12	0	0	6	10.0
T_B In [2]	1	1	4	1	3	6	12	0	0	0	9.3
T_C In [3]	3	0	0	18	0	0	3	0	0	0	8.0
T_D In [7]	2	0	0	3	0	6	12	0	0	0	7.7
T_E In [10]	1	1	0	6	0	3	3	6	3	0	7.7
T_F In [4]	3	0	0	18	0	0	0	0	0	0	7.0
T_G In [3]	3	0	0	18	0	0	0	0	0	0	7.0
T_H In [3]	3	0	0	15	0	0	3	0	0	0	7.0
T_I In [9]	2	0	0	18	0	0	0	0	0	0	6.7
T_J In [8]	2	0	0	12	0	6	0	0	0	0	6.7
T_K, NPC	2	0	0	12	0	0	6	0	0	0	6.7
T_L, CHHB	6	0	0	12	0	0	0	0	0	0	6.0
T_M In [5]	6	0	0	6	0	6	0	0	0	0	6.0
T_N, FCs	2	0	0	12	0	0	0	0	0	3	5.7
T_O In [6]	4	0	0	12	0	0	0	0	0	0	5.3
T_P, CHB	3	0	0	12	0	0	0	0	0	0	5.0
T_Q, T-type	2	0	0	6	0	6	0	0	0	0	4.7
T_R In [12]	2	0	0	9	0	3	0	0	0	0	4.7
T_S In [11]	1	1	0	6	0	6	0	0	0	0	4.7
The proposed topology	2	0	0	9	0	3	0	0	0	0	4.7

To make the comparison as fair as possible, the transferred power to the load must be equal in all compared topologies. This can be accomplished by generating the same voltage values across the connected load of each topology. The five voltage levels must have the same values for all circuits. For Example , -2*E*, *E*, 0, *E*, and 2*E* are selected to be the values of the five levels in the output voltage. Therefore, the values of the DC sources in the DC-link of some topologies are changed to generate the same output voltages.

According to Table VI, topologies T_Q-T_S are considered as the counterparts to the proposed topology in terms of component count. All of them require fourteen components to produce three voltage levels. However, the proposed topology has advantages of A) simpler DC-link requirements and lower high-voltage switches compared to topology T_S, B) higher count of low-voltage switches (9 instead of 6) and a 50% reduction of high voltage switches (3 instead of 6) compared to topology T_Q. Although the proposed topology and the topology T_R have the same advantages and disadvantages for three-level operations, the proposed topology is more advantageous for level counts more than three due to its merits of eliminating

flying capacitors, reaching to high voltages without output transformer, and simplifying control requirements (there is no need for voltage balancing algorithms or voltage sensors for controlling the voltages of the flying capacitors). From application point of view, the proposed topology is more advantageous in renewable energy systems, e.g. PV farms, or for low and high voltage applications, where several isolated DC sources are available. For example, when one module is used with the three-level fixed stage (i.e. six switches and DC sources more while saving three flying capacitors compared to T_R), the proposed topology generates seven, nine, eleven, and fifteen voltage levels for symmetrical and asymmetrical operation (DC voltage ratios are 1:1, 2:1, 1:2, and 1:3) while T_R generates five, seven, seven, and nine voltage levels with same DC voltage ratios.

VI. Conclusion

This paper presents and analyses a new three-phase multilevel topology, being applicable for both low-voltage and high-voltage applications. The key features of the proposed topology are numerically verified by simulation results and experimentally validated through an in-house laboratory prototype. The proposed topology is tested using a resistive-inductive load under low-frequency modulation and level-shifted pulse width modulation techniques. Further, the LFM is modified by integrating the proposed modulator *H*, enabling online control of the output voltage in terms of RMS value, frequency, and level count. Using similar building blocks in both configurations allows for reducing the time and cost of manufacturing, troubleshooting, voltage-level upgrading. A detailed comparison between the proposed topology and other recently developed MLIs in terms of component count and voltage ratings proves that the proposed topology avoids using of power diodes, inductors, and capacitors, resulting in a more compact design with a higher life-time, efficiency and simpler control algorithms.

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Paper V:

New Multilevel Inverter Topology with Reduced Component Count

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New Multilevel Inverter Topology with Reduced Component Count

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***Abstract*—This paper introduces a new topology of modular multilevel inverters, being suitable in medium and high voltage applications. As compared to the existing circuits, the proposed topology has advantages of high 'levels/components' ratio, increasing the output voltage levels without increasing the voltage stress across the used switches, structure simplicity, isolation features, and modularity. These merits allow it to fit well in high-reliability medium-power applications, which require fast troubleshooting and maintenance flexibility. Operating principles of the proposed scheme are detailed in low frequency and pulse width modulation. Simulation and experimental results validate the effectiveness of the circuit under different modulation and load conditions. Further, a comparative study between the proposed topology and other existing multilevel topologies was conducted and summarized in this paper.**

Index Terms— Converter control, multilevel converters, pulse-width modulation, staircases modulation, voltage source inverters.

I. Introduction

Modular multilevel inverters (MMLIs) have got great attention in both academia and industry due to their advantages such as high modularity, dynamics, power quality, low total harmonic distortion (THD), and low *dv/dt*. Such merits make MMLIs more suitable for an efficient and reliable power converter in renewable energy (RE) than counterparts, i.e. two-level, Quasi-Z-Source and matrix converters [1, 2]. Neutral point diode clamped (NPDC), flying capacitors (FC), and cascades H-bridge (CHB) converters have been developed for years to increase voltage levels, but increasing the voltage levels results in a higher number of components, typically switching devices, electrolytic capacitors, power diodes, and DC power supplies. Further, control complexity, fault-detection difficulty, short lifetime, and low efficiency have been the main drawbacks in the existing solutions. Producing new high-power switching devices and developing new multilevel inverters (MLIs) have been solutions to overcome the mentioned demerits [3-5]. Several topologies for MLIs have been intensively developed and reported in literature [6-13]. However, the existing circuits face certain challenges such as high component count, using electrolytic capacitors, limited output voltage levels, and control complexity.

In this paper, a new topology for modular multi-level converters is proposed to reduce component count and control complexity. The proposed circuit can galvanically isolate the source and the load by using a transformer bank. Although

the proposed circuit can operate in both symmetrical or asymmetrical modes, an only symmetrical configuration is studied in this paper. The proposed topology is compared to transformer-based and existing similar multilevel topologies. The comparative study shows that the proposed converter can further reduce the required components for producing the same output voltage levels as compared to the counterpart. Performance of the proposed topology under different load conditions using low-frequency modulation (LFM) and pulse width modulation (PWM) is verified via simulations and experimentally validated.

II. THE PROPOSED MULTILEVEL TOPOLOGY

A. GENERALIZED CONFIGURATION

The proposed topology consists of two stages: the main stage and repeated one. A N-level configuration is depicted in Fig. 1. The main stage comprises two DC power supplies and eighteen power switching devices connected to a medium frequency transformer bank. The medium frequency transformer provides isolating and stepping-up features, increasing the applicability for the proposed circuit.

The main stage operates as a base platform for generating five voltage levels while the repeated stage works as a level-generator stage, which can be repeated to increase the output levels. The relationship between the output voltage level number N and the utilized components can be defined by using the proposed equations (1)-(3).

$$N_{\text{Total}} = 3.5N + 5.5 \tag{1}$$

$$N_{\text{DC}} = 1.5N - 5.5 \tag{2}$$

$$N_{\text{SW}} = 2N + 8 \tag{3}$$

where N_{Total}, N_{DC}, and N_{SW} are the total component count, DC power supplies count and switching device count, respectively. For example, if only five voltage levels are required, the total number of the components will be twenty-three (two DC power supplies, eighteen switching devices, and three medium frequency transformers).

B. FIVE-LEVEL CONFIGURATION

The scaled-down circuit described in Fig. 2 is considered as a study case in this paper. The circuit uses only the main stage without any repeated stages, producing five voltage levels across the pole terminals AA, or BB, or CC and nine levels across the load terminals.

III. MODULATION STRATEGIES FOR THE PROPOSED TOPOLOGY

Modulation techniques for multi-level converters are usually classified based on many aspects. One of these aspects is the frequency of the switching signals that are produced by the modulation techniques. The switching algorithms can be implemented by using low-frequency modulation (LFM) strategies, i.e. selective

harmonic elimination (SHE) and staircases modulation (SCM) or based on high-frequency modulation (HFM) strategies, e.g. level-shifted, phase-shifted pulse width modulation schemes. The proposed topology is modulated by LFM and level-shifted PWM [1, 12].

A. LOW-FREQUENCY MODULATION

To control the proposed MLI in a way to produce high-quality sinusoidal output voltage a switching scheme based on LFM is designed according to Table I. This table has 28 switching states, and it shows the switching patterns for the used switches. By following these low-frequency patterns, multilevel voltage waveforms can be produced across the pole and load terminals.

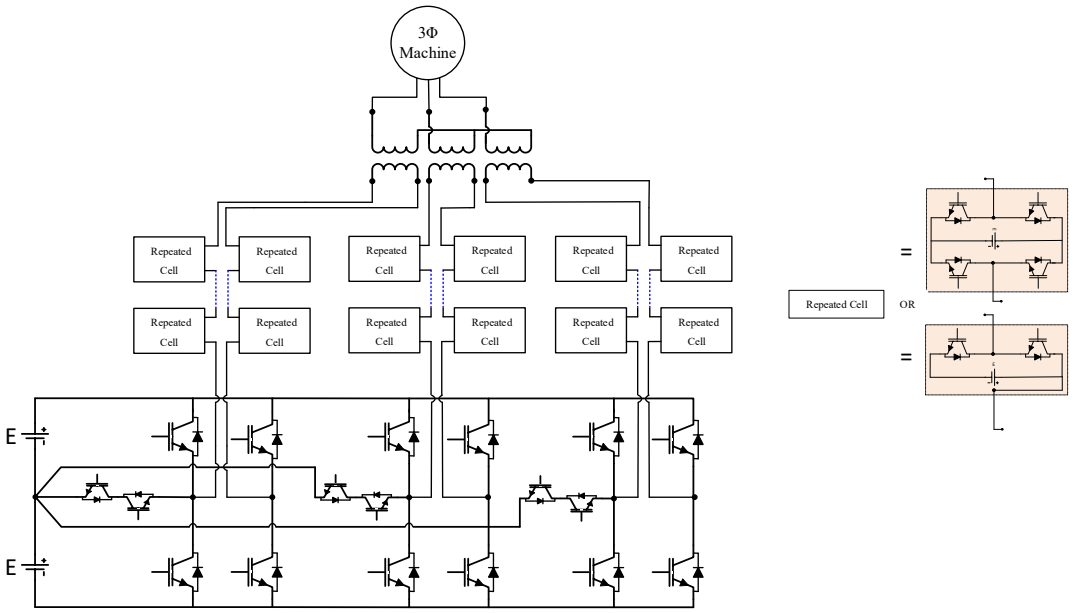


Fig. 1: The generalized configuration of the proposed topology.

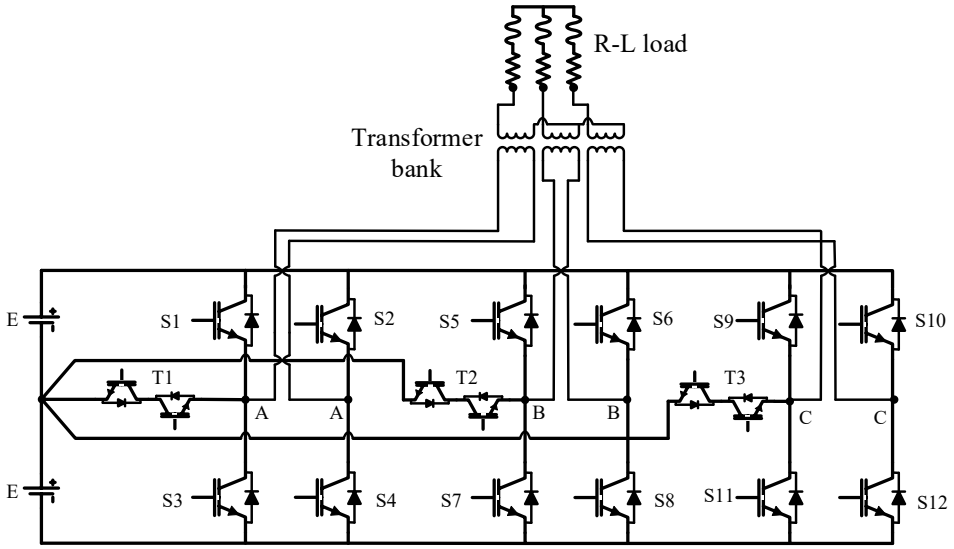


Fig. 2: The scaled-down configuration of the proposed topology.

TABLE I: THE SWITCHING STATES AND THE CORRESPONDING POLE VOLTAGES
(■ ON, □ OFF)

V_{AA}	2E	2E	2E	2E	2E	2E	E	0	-E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-E	0	E	2E	2E	2E	2E	2E
V_{BB}	-2E	-E	0	E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	E	0	-E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E
V_{CC}	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-2E	-E	0	E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	2E	E	0	-E	-2E
T_1							■		■													■		■					
S_1	■	■	■	■	■	■																			■	■	■	■	■
S_2									■	■	■	■	■	■	■	■	■	■	■	■	■								
S_3								■		■	■	■	■	■	■	■	■	■	■		■								
S_4	■	■	■	■	■	■	■	■														■	■	■	■	■	■	■	■
T_2		■		■												■		■											
S_5					■	■	■	■	■	■	■	■	■	■	■														
S_6	■	■															■	■	■	■	■	■	■	■	■	■	■	■	■
S_7	■		■													■		■	■	■	■	■	■	■	■	■	■	■	■
S_8			■	■	■	■	■	■	■	■	■	■	■	■	■	■													
T_3											■		■													■		■	
S_9														■	■	■	■	■	■	■	■	■	■	■	■				
S_{10}	■	■	■	■	■	■	■	■	■	■	■																	■	■
S_{11}	■	■	■	■	■	■	■	■	■	■		■															■		■
S_{12}												■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■		

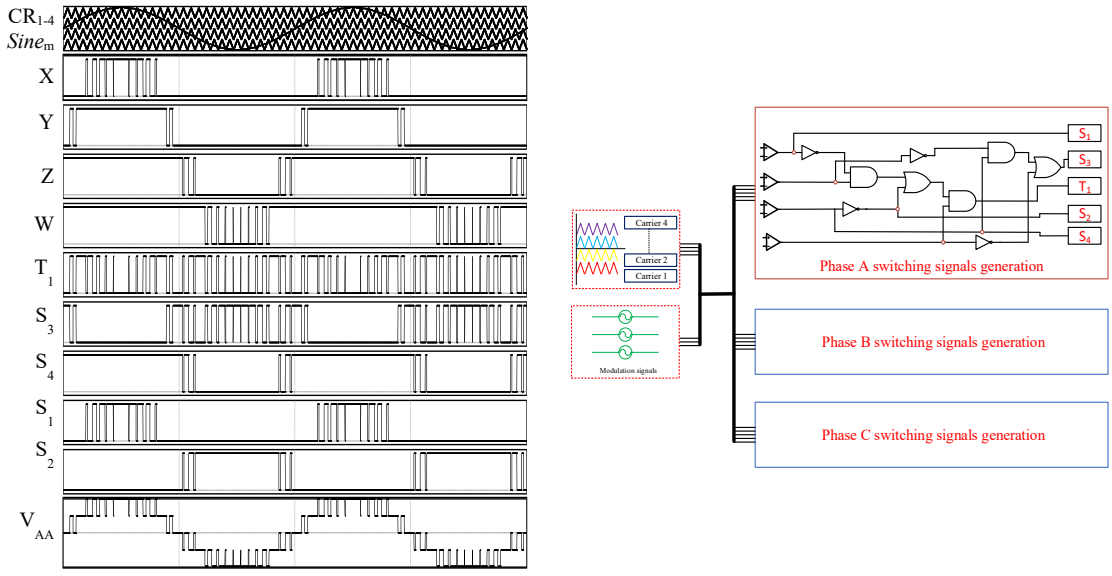
B. LEVEL-SHIFTED PULSE WIDTH MODULATION

Fig. 3 shows a switching scheme based on level-shifted pulse width modulation (LSPWM) and the key signals for phase A in the proposed circuit. For the purpose of producing five voltage levels using LSPWM, four carrier signals CR_1, CR_2, CR_3, and CR_4 are required as (4) [12]. These four carrier signals are equal in the magnitude, frequency, and phase angle.

$$N_{\text{carrier}} = N - 1 \tag{4}$$

The carrier signals are compared with three-phase modulation signals $Sine_{\text{m}}$, which are sinusoidal and have a phase shift of 120°. This is mandatory to produce three-phase balanced output sinusoidal voltages. Four control signals, *X*, *Y*, *Z*, and *W* are formed in the comparison process in the switching procedure. The switching pulses are formed by different logical operations on these four Boolean signals to make sure that switched multi-level sinusoidal signals are obtained on the output terminals.

Fig. 3 (a) shows only waveforms of phase A, while waveforms for phase B and C are the same with a phase shift of 120°. The switching scheme implementation is described in the proposed equations (5)-(9) and graphically shown in Fig. 3 (b).



(a) (b)

Fig. 3: The switching scheme for the proposed configuration. (a) Switching patterns and the resulted voltage V_{AA}. (b) Switching scheme implementation.

$$S_1 = X \tag{5}$$

$$S_2 = \overline{Z} \tag{6}$$

$$S_3 = \left(\overline{Y} \cdot Z\right) + \overline{W} \tag{7}$$

$$S_4 = Z \tag{8}$$

$$T_1 = \left(\left(\overline{X} \cdot Y\right) + \overline{Z}\right) \cdot W \tag{9}$$

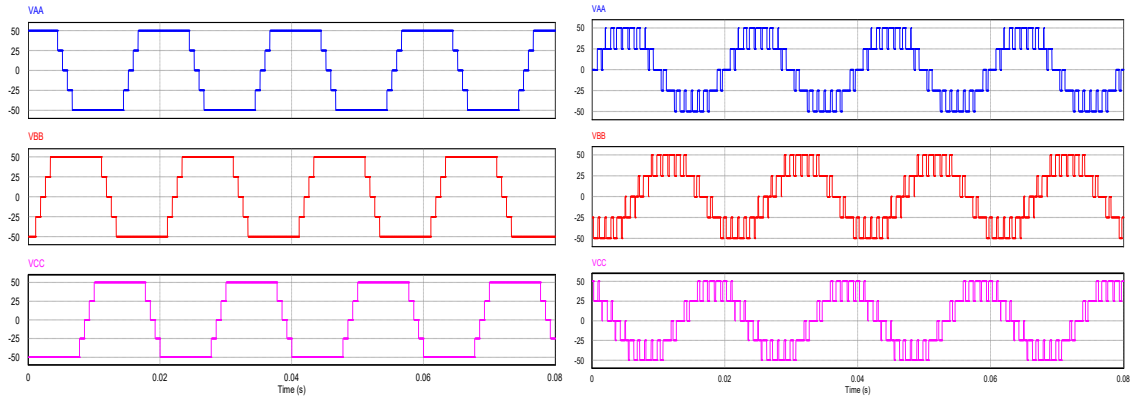
IV. Results and Discussions

A. Simulation Results

The proposed topology is simulated to verify its operating principle and to demonstrate the key waveforms. The simulation model based on the five-level case study in Fig. 2. It uses two symmetrical DC power supplies of 25 V. By controlling the proposed inverter using LFM and LSPWM, a nine-level voltage will be generated across the output terminals, the converter feeds power to an inductive load of 0.9 lagging power factor, R = 10 Ω, L = 75 mH. In LSPWM, the carrier frequency is equal to 1 kHz, and the modulation index (MI) is set to one (MI= 2*|$sine_m$|/|(CR_1+CR_2+CR_3+CR_4) |).

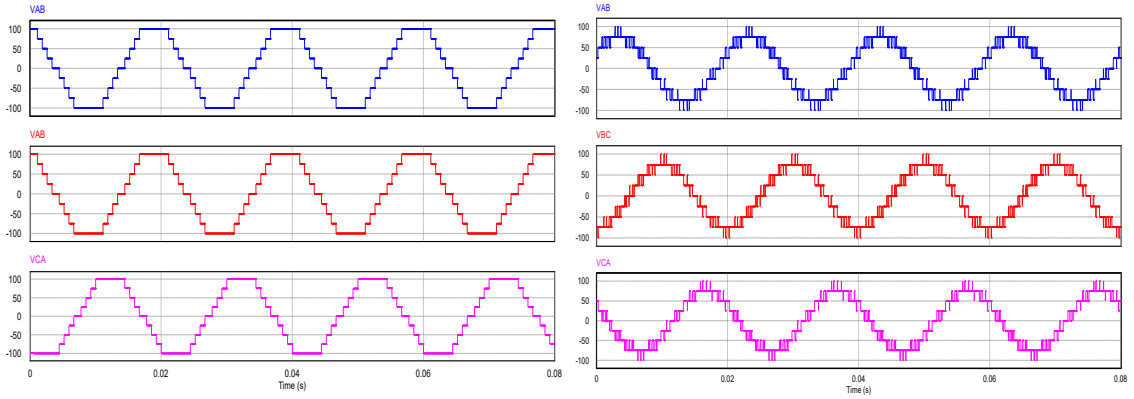
The operating principle is based on generating three five-level voltage waveforms V_{AA}, V_{BB}, and V_{CC} across terminals AA, BB, and CC, respectively. These waveforms must be shifted in phase to produce balanced three-phase voltages V_{AB}, V_{BC}, and V_{CA}, (e.g. $V_{AB} = V_{AA} - V_{BB}$). By using this technique there is no need for an end-side H-bridge that is commonly used for producing bipolar

voltages waveforms, so the voltage stress and switches are reduced. The pole-voltage waveforms are depicted in Fig. 4, including five voltage levels: *2E* ,*E*, *0*, *-E*, and *-2E* where *E*=25 V. By subtracting these three voltages waveforms from each other, three-phase balanced nine-level voltages are produced across the load terminals as described in Fig. 5, including three waveforms with nine steps



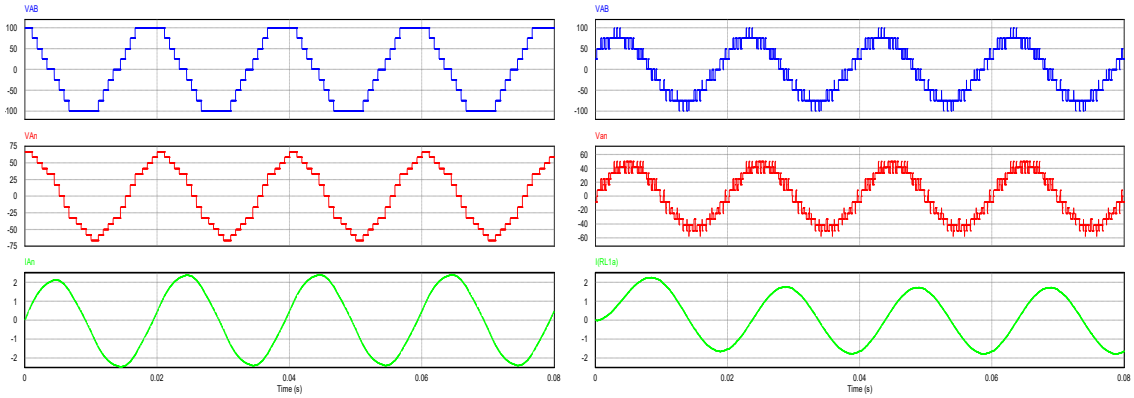
(a) (b)

Fig. 4: Pole voltages waveforms V_{AA}, V_{BB}, and V_{CC}. (a) Low-frequency modulation. (b) Level-shifted PWM.



(a) (b)

Fig. 5: Output voltages waveforms V_{AB}, V_{BC}, and V_{CA}. (a) Low-frequency modulation. (b) Level-shifted PWM.



(a) (b)

Fig. 6: Output waveforms under R-L load V_{AB}, V_{An}, and I_{An}. (a) Low-frequency modulation. (b) Level-shifted PWM.

4E ,3*E*, *2E* ,*E, 0*, *-E*, *2E* ,-3*E*, and *-4E*. Moreover, Fig. 6 not only shows the output voltages and load current but also shows the phase voltage V_{AN} having thirteen levels of $\frac{8}{3}E$, $\frac{7}{3}E$, $\frac{6}{3}E$, $\frac{5}{3}E$, $\frac{4}{3}E$, $\frac{2}{3}E$, 0, $\frac{-2}{3}E$, $\frac{-4}{3}E$, $\frac{-5}{3}E$, $\frac{-6}{3}E$, $\frac{-7}{3}E$, and $\frac{-8}{3}E$.

B. EXPERIMENTAL RESULTS

To validate the performance of the proposed topology, a laboratory setup was built and implemented to confirm the simulation results. Fig. 7 shows the in-house experimental setup, containing the proposed MLI, DC sources, three transformers, dSPACE's MicroLabBox controller, measurement tools and probes. Twelve IGBT modules - SKM300GA12E4 with built-in freewheeling diodes were used to produce a five-level MLI. These IGBT modules were controlled through twelve SKHI 10/12 R driver boards. The specifications of the simulation system are modified in order to match the currently available equipment in the laboratory. The experimental system parameters are listed in Table II. Figs. 8, 9 and 10 show the key waveforms at each stage of the proposed converter. The obtained waveforms show that the proposed MLI can produce five voltage levels under control of both low frequency and PWM switching schemes. Further, the effect of transformers on the output line voltages was indicated in Figs. 9 and 10.

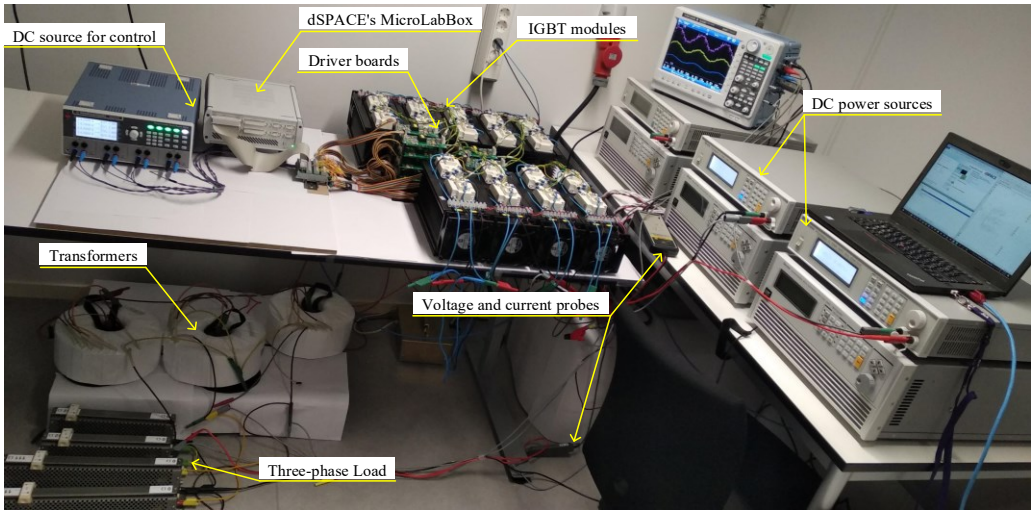
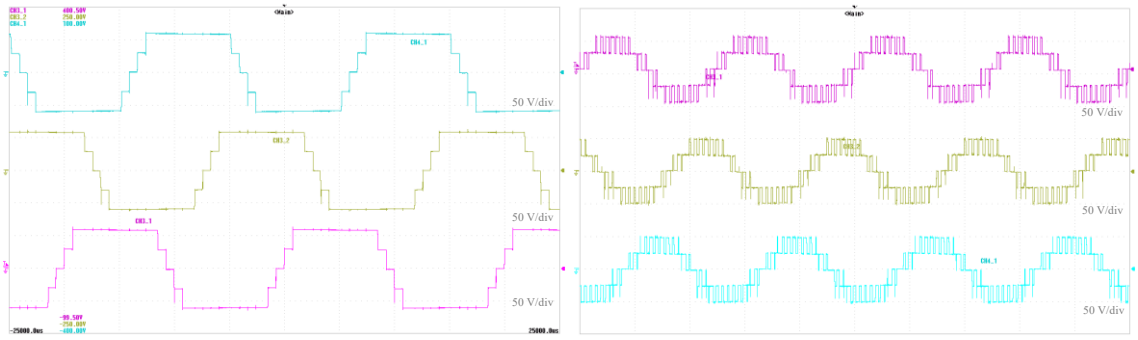


Fig. 7: Laboratory prototype of the proposed topology

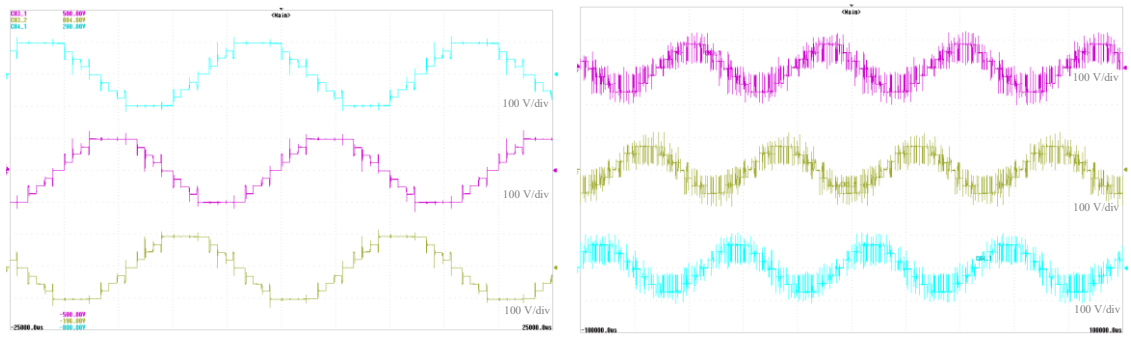
TABLE II: SPECIFICATIONS FOR EXPERIMENTAL SETUP

Parameter	Value	Unit
DC voltage source E	25	V
Load R	100	Ω
Switching Frequency F_s	1000	Hz
Sampling Time T_s	30	µs
Modulation Index MI	0.85	–
1-phase transformer (5 KVA)	240/240	V



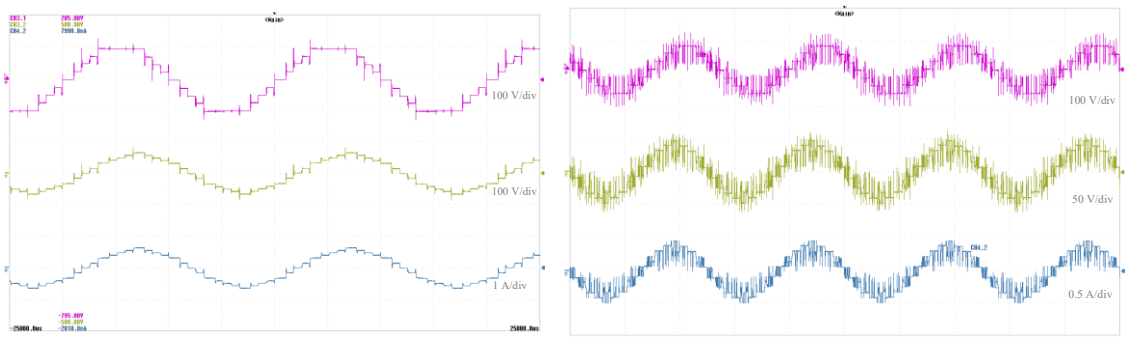
(a) (b)

Fig. 8: Pole voltages V_{AA}, V_{BB}, and V_{CC}. (a) Low-frequency modulation. (b) Level-shifted PWM



(a) (b)

Fig. 9: Output line voltages waveforms V_{AB}, V_{BC}, and V_{CA}. (a) Low-frequency modulation. (b) Level-shifted PWM.



(a) (b)

Fig. 10: Output waveforms under resistive load V_{AB}, V_{AN}, and I_{AN}. (a) Low-frequency modulation. (b) Level-shifted PWM.

V. Comparison of Five-Level Configurations

Recently, several MLI topologies have been introduced in [6-13] to reduce the total number of the used components. A comparison between the proposed topology and the existing ones with the same output voltage levels are summarized in Table III to illustrate the merits of the proposed configuration. The comparative study shows that the proposed structure has various significant merits: low component count, without using electrolytic capacitors for its operation or additional circuit for balancing process, resulting in higher reliability and lifetime, lower control complexity. Moreover, the proposed configuration is a diode-free

topology, enhancing efficiency, since power diodes consume higher energy than other semiconductor devices. From the applications point of view, the proposed MLI has a modular structure feature, allowing the output voltage levels to increase without increasing voltage stress across the switching devices. Further, both complete isolation and flexible output voltage value are guaranteed by using transformers bank, which is very useful in upgrading existing systems. To sum up, the proposed topology is an attractive solution in applications that require a high-reliability degree, simple control and multi-level output voltages with isolation features.

TABLE III: COMPONENTS REQUIREMENT FOR FIVE-LEVEL THREE-PHASE CONVERTERS

Topology	DC Sources	Switches	Diodes	Capacitors	Transformers	Total	CLF* Factor
[10] 5L-Topolgy 4	1	68	0	3	0	72	14.4
[10] 5L-Topolgy 3	1	62	0	1	2**	66	13.2
Neutral point Clamped	1	24	36	4	0	65	13.0
[10] 5L-Topolgy 1	1	50	2	0	0	53	10.6
[6] 5-level topology	6	24	12	6	0	48	9.6
[10] 5L-Topolgy 2	1	44	0	2	0	47	9.4
[9]	1	36	0	8	0	45	9.0
[10] Stacked multicell converter (SMC)	2	36	0	6	0	44	8.8
[8]	1	24	6	5	0	36	7.2
Half H-Bridge	12	24	0	0	0	36	7.2
[13]	10	24	0	0	0	34	6.8
[12]	4	27	0	0	0	31	6.2
[7]	1	24	0	2	3	30	6.0
[6]	9	18	3	0	0	30	6.0
Full H-Bridge	6	24	0	0	0	30	6.0
Proposed Topology	2	18	0	0	3	23	4.6

*components per level factor [13], ** power inductors, not transformer

VI. CONCLUSION

In this study, a new modular multilevel topology suitable for high-voltage medium power applications was proposed. Although the proposed topology can produce N-level, only five-level version was studied and validated in this paper. For the purpose of illustrating operating principles of the proposed topology, both pulse width and low-frequency modulation strategies are successfully developed and implemented. Further, the simulation results were experimentally validated by using an in-house lab setup. Moreover, a comparative study between the proposed circuit and other multilevel inverter topologies was conducted and summarized. Compared to the existing five-level topologies, the proposed topology has the merits of using low component count for producing the same number of output voltage level. Finally, several significant limitations due to using transformers such as size, noise, and presence of leakage or parasitic inductance, etc. need to be considered in certain applications.

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