How gettering affects the temperature sensitivity of the implied open circuit voltage of multicrystalline silicon wafers

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Abstract **— The temperature sensitivity of the open circuit voltage of a solar cell is mainly driven by changes in the intrinsic carrier concentration, but also by the temperature dependence of the limiting recombination mechanisms in the cell. This paper investigates the influence of recombination through metallic impurities on the temperature sensitivity of multicrystalline silicon wafers. Spatially resolved temperature dependent analysis is performed to evaluate the temperature sensitivity of wafers from different brick positions before and after being subjected to phosphorus diffusion gettering. Local spatial analysis is performed on intra-grain areas, dislocation clusters and grain boundaries. Large variations in temperature sensitivity is observed across the wafers both before and after gettering. The spatially resolved γ parameter is found to change with gettering, indicating that the gettering process alters the balance between different recombination mechanisms in the material. Features with low temperature sensitivity are observed across the wafers and correlated with dislocation clusters. The locations of these areas remain unchanged by the gettering process, suggesting that the cause for the low temperature sen-**

sitivity is not removed. Gettering is observed to have a complex effect on the temperature sensitivity of the dislocation clusters depending on the wafer position in the brick, with dislocations from the top wafer exhibiting lowest temperature sensitivity both before and after gettering.

E.I. Introduction

Silicon solar cells are usually characterized and optimized under standard test conditions (STC), defined as a global standard solar spectrum AM1.5G, an irradiance of 1000 W/m^2 and a cell temperature of 25 °C [1]. However, real operating temperatures can differ considerably from STC [2]. Temperature significantly affects the characteristics of photovoltaic (PV) devices, as has been known for decades [2–5]. Understanding the thermal behavior of a PV device under non-STC is therefore essential to accurately estimate the production of PV power plants and to optimize PV devices for different climatic conditions.

The thermal behavior of a solar cell is primarily determined by the temperature sensitivity of the open circuit voltage (V_{oc}) which accounts for approximately $80 - 90\,\%$ of the total temperature sensitivity of a reasonably good solar cell [6]. The V_{oc} generally decreases with increasing temperature due to a reduction of the band gap energy (E_{g}) which consequently increases the intrinsic carrier concentration (n_i) and the internal carrier recombination [6–8]. The temperature sensitivity of V_{oc} is usually quantified using the temperature coefficient ($\beta_{V_{\mathrm{oc}}}$). To the first-order approximation, and in absolute form, it is given as [9]

$$\beta_{V_{\mathrm{oc}}} = \frac{dV_{\mathrm{oc}}}{dT_{\mathrm{c}}} = -\frac{E_{\mathrm{g0}}/q - V_{\mathrm{oc}} + \gamma k T_{\mathrm{c}}/q}{T_{\mathrm{c}}}, \tag{E.1}$$

where E_{g0} denotes the semiconductor bandgap energy extrapolated to 0 K, q is the elementary charge, k is the Boltzmann constant, and T_{c} is the cell temperature. The parameter γ includes the temperature dependence of several parameters determining the dark saturation current, J_0, and therefore contains information about the dominant recombination mechanism in the material. According to Ref. [4], γ usually takes values between 1 and 4.

Eq. (E.1) predicts an approximately linear relationship between $\beta_{V_{\mathrm{oc}}}$ and the V_{oc} of the cell, implying that a cell with a high V_{oc} will have the inherent advantage of reduced temperature sensitivity. In addition, $\beta_{V_{\mathrm{oc}}}$ can be significantly influenced by the last term in Eq. (E.1) containing the parameter γ [2].

Previously, Berthod *et al.* studied the relationship between global $\beta_{V_{\mathrm{oc}}}$ values and brick height of compensated multicrystalline silicon (mc-Si) solar cells [10]. The authors found lower temperature sensitivity for cells from the top of the bricks despite low V_{oc} values observed for these cells. They suggested that it could be caused by an increased concen-

tration of different crystal defects, typically found in the top of mc-Si ingots as a result of the directional solidification process. Recently, Eberle *et al.* reported increased temperature sensitivity of V_{oc} in contaminated regions of mc-Si cells but reduced temperature sensitivity for areas containing dislocation clusters [11]. This was further investigated by Eberle *et al.* in Ref. [12], reporting reduced temperature sensitivity of dislocation clusters of mc-Si wafers and cells. The authors suggested that it could be caused by the presence of impurities in the dislocation areas and thus Shockley-Read-Hall (SRH) recombination. These findings illustrate the impact of crystallographic defects on the temperature sensitivity of V_{oc} of mc-Si wafers and cells and highlight the importance of further studies to evaluate the varying influence of different defect types. Moreover, it shows the necessity of spatially resolved analysis for detailed investigation of the temperature sensitivity.

This work examines the influence of metallic impurities on the thermal behavior of V_{oc} of mc-Si wafers. Metallic impurities are detrimental limiting defects in *p*-type mc-Si in addition to dislocation clusters [13–15] and knowledge about their impact on the temperature sensitivity is therefore important. This is investigated by spatially evaluating the temperature sensitivity of mc-Si wafers before and after being subjected to phosphorus diffusion gettering (PDG), serving the purpose of altering the concentration of metallic impurities across the wafers [16].

E.II. Experimental Method

A. Sample Preparation

Wafers were cut from a high-performance compensated *p*-type mc-Si ingot tri-doped with boron, gallium and phosphorus. The ingot was made from a blend of compensated silicon [Elkem Solar Silicon® (ESS®)] and polysilicon with a blend-in-ratio of 70 % ESS® and resistivity of 0.9 Ω·cm. Eight 6" wafers were chosen from different positions in a central brick.

The wafers were processed in two steps: Step 1 (referred to as *ungettered*): The as-sawn wafers received saw damage etching, cleaning [17], and passivation with 75 nm silicon nitride (SiN_x) using an industrial plasma-enhanced chemical vapor deposition (PECVD) system (MAiA, Meyer Burger) at a deposition temperature of 400 °C [18]. Step 2 (referred to as *gettered*): The passivation from Step 1 was removed using hydrofluoric (HF) acid followed by a second clean. A conventional PDG [16] was performed by subjecting the wafers to a 45 min $POCl_3$ diffusion treatment with peak temperature of 850 °C resulting in a sheet resistance of 40 Ω·cm [19, 20]. The surface gettering layer was then removed by alkali etching and the wafers were re-passivated using an identical SiN_x process as in Step 1. The wafers were fully characterized after Step 1 and after Step 2.

B. Characterization and Analysis

The wafers were characterized using our novel temperature dependent photoluminescence (PL) imaging system [21], where PL images were acquired at 25 °C and 70 °C enabling mapping of the effective carrier lifetime (τ_{eff}), implied open circuit voltage (iV_{oc}), the temperature coefficient of iV_{oc} ($\beta_{iV_{\text{oc}}}$), and γ. The PL images were obtained at a photon flux of $1.2 \cdot 10^{17}\,\text{cm}^{-2}\text{s}^{-1}$, corresponding to an illumination intensity of approximately 0.5 Sun.

The PL images of the ungettered wafers were calibrated based on a temperature dependent photo-conductance (PC) signal measured on a region of the wafer during PL image acquisition. A detailed description of the calibration procedure can be found in Ref. [21]. The PL images of the gettered wafers were calibrated using a temperature dependent front detection PL-based system [22] to account for trapping observed for these wafers at relevant injection levels. The calibration was performed using a temperature and injection dependent τ_{eff} curve obtained by simultaneously measuring a PC signal on the wafer and collecting a PL signal emitted from the wafer. The τ_{eff} curve obtained from the quasi-steady-state (QSS) PL signal was then matched with the PC-based τ_{eff} curve at high injection. The wafers before and after gettering were therefore both calibrated using PC-based measurements.

From the calibrated PL images, absolute $\beta_{iV_{\text{oc}}}$ maps were obtained by applying to each pixel the following operation:

$$\beta_{iV_{\text{oc,abs},xy}} = \frac{iV_{\text{oc},T2,xy} - iV_{\text{oc},T1,xy}}{T_2 - T_1}. \tag{E.2}$$

Relative $\beta_{iV_{\text{oc}}}$ maps were obtained by normalizing each pixel with the local iV_{oc} at 25 °C. Finally, maps of the γ parameter were created by applying Eq. (E.1) to each pixel. Note that a circular heat stage (Sinton WCT-120TS) was used for imaging, causing an inhomogeneous wafer temperature outside of the heat stage [a circular feature can be observed in Fig. E.1(c)]. Therefore, only the area of the wafers with uniform temperature was used for further analysis.

E.III. Results and Discussion

A. Effect of Gettering on the Temperature Sensitivity

A wafer from the top of the brick is chosen for in-depth analysis since it typically contains a higher impurity concentration compared to wafers from the middle of the brick and thus may be more effectively gettered [23, 24]. Figs. E.1(a) and (e) show images of iV_{oc} at 25 °C of a wafer from the top of the brick before and after gettering, respectively. Dislocations can be identified as dark clusters in the images where recombination active

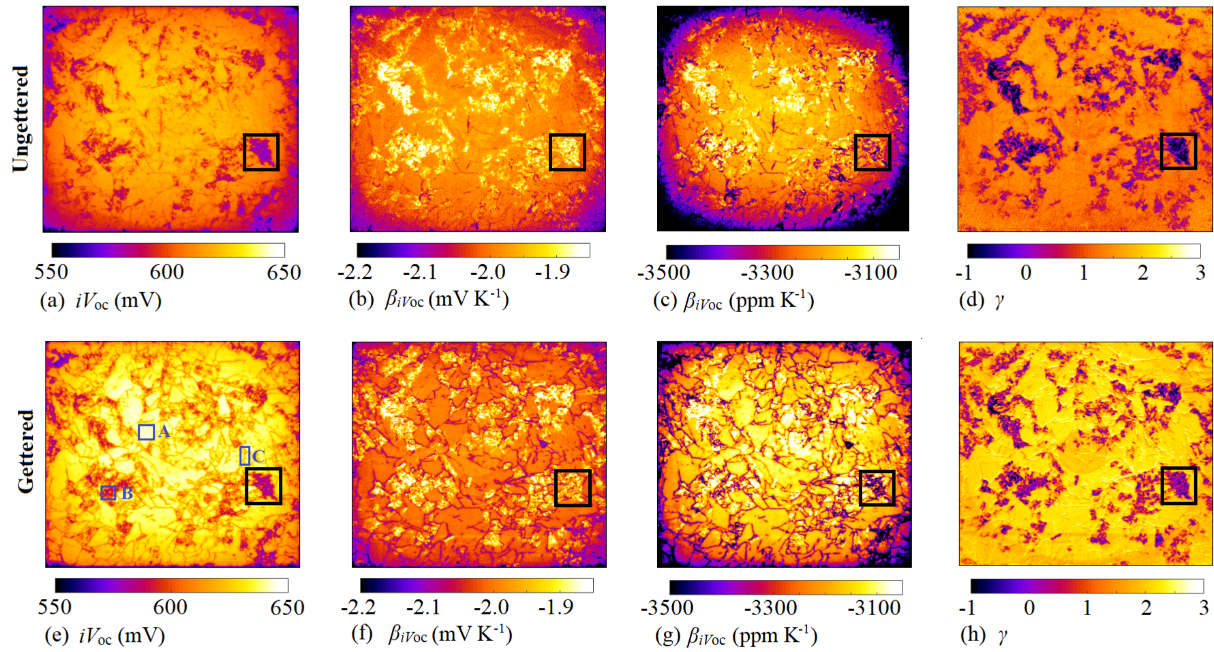

Figure E.1: Images of iV_{oc} at 25 °C, absolute and relative $\beta_{iV_{oc}}$ and γ of a wafer from the top of the brick before (a-d) and after (e-h) gettering. The black square marks a dislocation cluster of special interest. The letters A-C mark areas on the wafer of different crystal quality: (A) An intra-grain area, (B) a dislocation cluster, and (C) a grain boundary.

grain boundaries appear as dark lines. Comparing the two images, the gettering process is found to improve the quality of the intra-grain areas but to increase the recombination activity of the grain boundaries, consistent with results previously reported [23, 25]. The improvement of the intra-grain areas results from the ability of the gettering process to reduce the concentration of detrimental metallic impurities in these areas [16]. The activation of the grain boundaries has been suggested to result from metal decoration of the structures during the gettering process causing a change in recombination behavior [26–29]. It seems that the dislocation clusters are recombination active both before and after gettering.

Figs. E.1(b) and (f) show images of the absolute $\beta_{iV_{oc}}$ before and after gettering, respectively. Large variations are found across the wafer both before and after PDG highlighting the importance of spatially resolved analysis. The temperature sensitivity of intra-grain areas does not seem to be significantly affected by the gettering process for this wafer. In contrast, the grain boundaries show a clear increase in temperature sensitivity after gettering, consistent with the expected correlation between material quality and $\beta_{iV_{oc}}$ as predicted from Eq. (E.1). One interesting observation is that the areas across the wafer exhibiting low temperature sensitivity remain unchanged by the gettering process. Comparing Figs. E.1(b) and (f) to Figs. E.1(a) and (e), the low temperature sensitivity

regions seem to be correlated with dislocation clusters: An unexpected observation since Eq. (E.1) predicts high temperature sensitivity when the iV_{oc} is low. This finding is in correlation with results reported by other recent studies [11, 12, 21, 30] and has been suggested to result from the presence of impurity atoms [12]. It should be noted that some dislocation clusters of wafers from other brick positions were observed to exhibit high absolute temperature sensitivity, however, all features with low temperature sensitivity could be correlated with dislocation clusters.

Similar trends can be found in Figs. E.1(c) and (g) showing images of the relative $\beta_{iV_{\text{oc}}}$ before and after gettering, respectively. However, because the relative $\beta_{iV_{\text{oc}}}$ is more strongly dependent on iV_{oc} compared to the absolute $\beta_{iV_{\text{oc}}}$, intra-grain areas show a relatively larger improvement in temperature sensitivity after gettering compared to Fig. E.1(f). This effect also causes the grain boundaries to exhibit a more negative relative $\beta_{iV_{\text{oc}}}$ after gettering. A region of interest (ROI) is identified on the wafer (black square), containing a dislocation cluster that shows low absolute temperature sensitivity (less negative absolute $\beta_{iV_{\text{oc}}}$) but high relative temperature sensitivity (more negative relative $\beta_{iV_{\text{oc}}}$). This illustrates the importance of the chosen representation of the temperature coefficient and how it can affect the conclusion drawn from the data if proper care is not taken.

Figs. E.1(d) and (h) show images of γ before and after gettering. Large variations are found across the wafer both before and after gettering, indicating that different recombination mechanisms dominate different regions of the wafer. Features with low (and in some cases even negative) γ values can be observed across the wafer and seem to be correlated with dislocation clusters by comparing with Figs. E.1(a) and (e). The locations of these features on the wafer remain the same before and after gettering. The gettering process is found to increase γ in most areas across the wafer.

To investigate the correlation between temperature sensitivity and crystal quality, Figs. E.2(a) and (b) show the absolute $\beta_{iV_{\text{oc}}}$ and iV_{oc} of each pixel on the PL image of the wafer before and after gettering, respectively. Comparing the two figures, gettering is found to broaden the distribution towards higher iV_{oc} and more negative $\beta_{iV_{\text{oc}}}$ suggesting that the gettering process generally improves the quality of parts of the wafer but increases the temperature sensitivity. Note that the medium quality regions exhibit both the lowest and the highest temperature sensitivity.

B. Temperature Sensitivity of Intra-grain Areas, Dislocations, and Grain Boundaries

To further investigate how gettering affects the temperature sensitivity of areas of different crystal quality, local spatial analysis is performed. Three different regions of the wafer

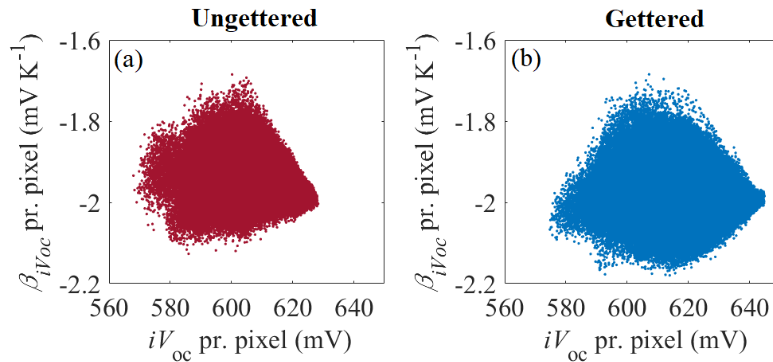

Figure E.2: Absolute $\beta_{iV_{oc}}$ as a function of iV_{oc} for each pixel before and after gettering of a wafer from the top of the brick.

Table E.1: Crystal quality and average absolute $\beta_{iV_{oc}}$ and γ before and after gettering for different regions on a top wafer.

Region	Crystal quality	$\beta_{iV_{oc}}$(unget.) (mV K^{-1})	γ (unget.)	$\beta_{iV_{oc}}$(gettered) (mV K^{-1})	γ (gettered)
A	Intra-grain	-1.98	1.50	-2.00	2.26
B	Dislocation	-1.91	-0.243	-1.95	0.313
C	Grain boundary	-1.98	1.29	-2.02	2.18
-	Global value	-1.96	0.840	-1.98	1.40

are examined, marked in Fig. E.1(e) with the letters A-C, indicating (A) an intra-grain area, (B) a dislocation cluster, and (C) an area containing grain boundaries.

Figs. E.3(a), (d) and (g), show the absolute $\beta_{iV_{oc}}$ as a function of iV_{oc} for each pixel before and after gettering for Regions A-C. Corresponding histograms of absolute $\beta_{iV_{oc}}$ are presented in Figs. E.3(b), (e) and (h), illustrating more clearly the distribution of the temperature sensitivity. Straight lines are inserted in the histograms indicating the average values of the distributions. An overview of the average values can be found in Tab. E.1.

From Fig. E.3(a), the intra-grain region is found to shift towards higher values of iV_{oc} after gettering, indicating a successful gettering of impurities from this region. Note that a similar behavior was observed for most intra-grain regions. The distribution of $\beta_{iV_{oc}}$ [Figs. E.3(a) and (b)] is narrow and show a slight shift towards more negative $\beta_{iV_{oc}}$ values, from an average value of $-1.98\,\mathrm{mV\,K^{-1}}$ to $-2.00\,\mathrm{mV\,K^{-1}}$. This suggests that removal of impurities initially present in this area did not have a significant effect on the temperature sensitivity.

From Figs. E.3(d) and (e), the dislocation cluster exhibits a broad distribution of $\beta_{iV_{oc}}$ both before and after gettering and the gettering process is found to shift the distribution

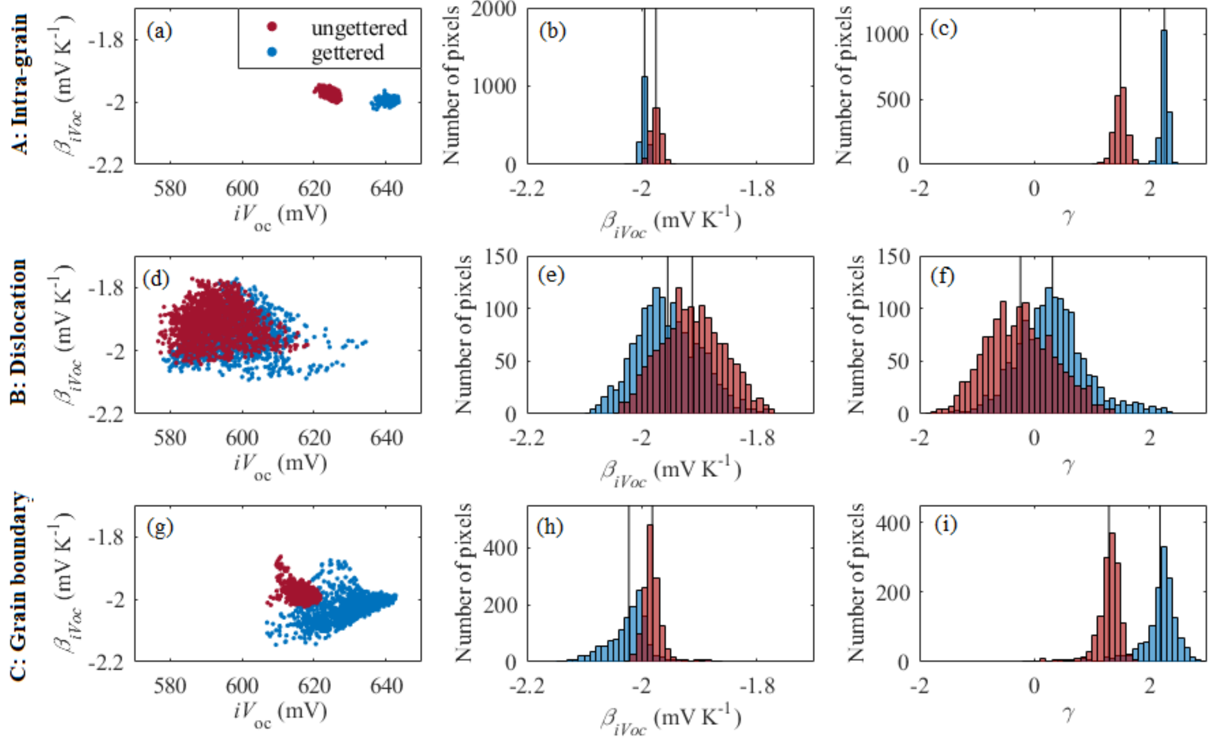

Figure E.3: Absolute $\beta_{iV_{oc}}$ as a function of iV_{oc} for each pixel; and distribution of absolute $\beta_{iV_{oc}}$, and γ in (A) an intra-grain area (a)-(c), (B) dislocation cluster (d)-(f), and (C) grain boundaries (g)-(i) before and after gettering. Straight lines indicate the average values of the $\beta_{iV_{oc}}$ and γ distributions. The locations on the wafer are defined in Fig. E.1(e). Note that the number of pixels differ for the different regions.

to more negative $\beta_{iV_{oc}}$ values. Note the tail of pixels in Fig. E.3(d) which is shifted towards higher iV_{oc} values after gettering. This is likely to be caused by intra-grain areas that were included in this ROI. The dislocation cluster exhibits a wide range of $\beta_{iV_{oc}}$ including regions with the lowest $\beta_{iV_{oc}}$. On average, the temperature sensitivity of this area is found to be the lowest compared to the other two ROIs both before and after gettering (see Tab. E.1).

Turning our attention to the grain boundary area, Figs. E.3(g) and (h) illustrate that the gettering process broadens the distribution of both iV_{oc} and $\beta_{iV_{oc}}$. Furthermore, gettering is found to shift most of the pixels towards more negative $\beta_{iV_{oc}}$ values. The large spread in pixel behavior is likely to arise from the combination of the actual grain boundary and near grain boundary areas which are included in the analyzed region. A long tail appears towards negative $\beta_{iV_{oc}}$ values after gettering, likely to represent the actual grain boundary region. This is consistent with the observations made from the PL images [see Figs. E.1(b) and (f)].

When comparing the average $\beta_{iV_{oc}}$ values of the Regions A-C (see Tab. E.1), the intra-

grain area and grain boundary are found to exhibit very similar behavior. However, when investigating the corresponding distributions in these areas, large differences are found. The grain boundaries are found to exhibit a significantly broader peak towards negative $\beta_{iV_{\mathrm{oc}}}$ values, and the dislocation cluster consists of a tail both with low and high temperature sensitivity. The dislocation clusters are found to exhibit the lowest temperature sensitivity of the three areas both before and after gettering, indicating that the cause for the low temperature sensitivity is not removed by the gettering process. Several other regions of intra-grain areas, dislocations, and grain boundaries were examined on this wafer and were found to show similar distributions and changes in $\beta_{iV_{\mathrm{oc}}}$ with gettering, demonstrating that the selected regions can be considered representative of the different crystal areas across this wafer.

The distributions of γ parameters before and after gettering for the Regions A-C are presented in Figs. E.3(c), (f) and (i). Gettering is observed to shift the distributions to higher γ values for all areas indicating that the gettering process alters the balance between different recombination mechanisms in the material. A relatively large number of pixels in the dislocation cluster display negative γ values. The physical interpretation of this has not yet been determined but has been observed elsewhere in the literature [11, 31].

C. Influence of Brick Position

Multicrystalline silicon ingots typically contain large variations in concentration and composition of crystallographic defects along the ingot as a consequence of the quality of the feedstock and the directional solidification process [24, 32]. This can have a significant impact on the recombination activity of different crystal defects in the as-grown state and how they respond to gettering (see Refs. [23, 26]). It is therefore natural to investigate if this has an impact on the temperature sensitivity of different crystal defects, depending on the original position of the wafer in the brick. An example of this is given in Figs. E.4(a)-(d) which show the distribution of $\beta_{iV_{\mathrm{oc}}}$ of dislocation clusters of four wafers from different relative brick heights of 0.05, 0.34, 0.47, and 0.89, respectively. Average values of the distributions are marked on the figures. Broad distributions are observed for all dislocation clusters, and all distributions are found to shift towards more negative $\beta_{iV_{\mathrm{oc}}}$ values after gettering except for the bottom wafer (relative height 0.05) which exhibits an opposite behavior. This illustrates how brick position can influence the temperature sensitivity and gettering response of different crystal defects.

Comparing the dislocation clusters from the bottom and the top wafers (relative heights 0.05 and 0.89, respectively), the iV_{oc} improves significantly more with gettering for the bottom wafer (from 586 mV to 604 mV) compared to the top wafer (from 597 mV

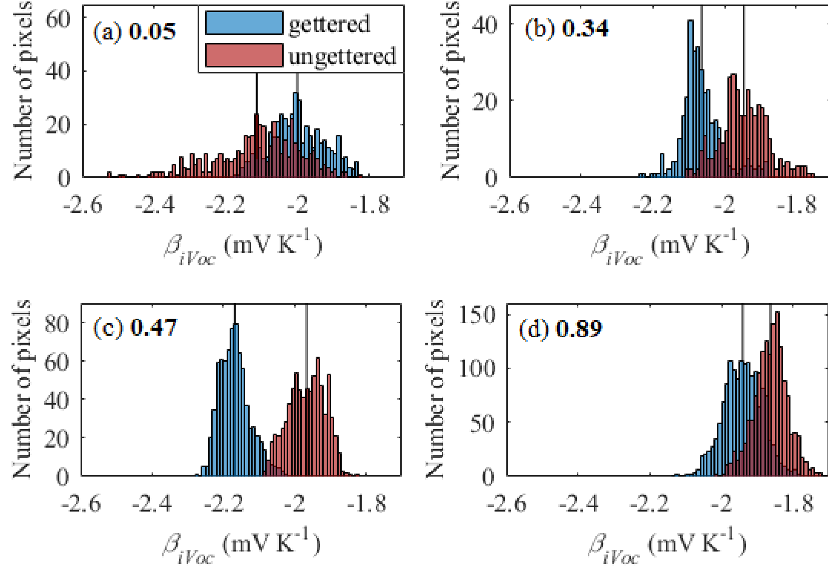

Figure E.4: Distribution of $\beta_{iV_{oc}}$ values of dislocation clusters before and after gettering from four wafers from different brick positions corresponding to 0.05 (a), 0.34 (b), 0.47 (c), and 0.89 (d) of the full brick height. Average values of the distributions are marked with a straight line.

to 601 mV). This indicates that the gettering process was more successful in removing impurities from the dislocation cluster from the bottom wafer, improving the overall performance and therefore the temperature sensitivity. However, despite of comparable iV_{oc} values after gettering, the dislocation in the top wafer still shows the lowest temperature sensitivity compared to the other wafers. Other dislocations on the top wafer were examined and found to show similar behavior. This suggests that dislocation clusters on wafers from the top of a brick might have different properties which could be beneficial at elevated temperatures.

E.IV. Summary

In this study, the temperature sensitivity of the iV_{oc} of mc-Si wafers was investigated and the influence of gettering was evaluated. Large variations in $\beta_{iV_{oc}}$ was observed across the wafers both before and after gettering. Gettering was found to change the γ parameter across the wafer, indicating that the process alters the balance between different recombination mechanisms in the material.

Local spatial analysis was performed to assess the temperature sensitivity of intra-grain areas, dislocation clusters, and grain boundaries. We observed that the gettering process increases the absolute temperature sensitivity of grain boundaries but does not significantly affect the intra-grain areas. Features with low absolute temperature sensi-

tivity were identified across the wafers and could be correlated with dislocation clusters. The location of these areas remained unchanged by the gettering process, indicating that the cause for the low temperature sensitivity was not removed by the gettering process.

Gettering was observed to have a complex effect on the temperature sensitivity of the dislocation clusters depending on the wafer position in the brick. Dislocations from the top wafer exhibited the lowest temperature sensitivity both before and after gettering, suggesting that these dislocation clusters might have different properties which could be beneficial at elevated temperatures.

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