Temperature coefficients and crystal defects in multicrystalline silicon solar cells

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Doctoral Dissertations at
the University of Agder 300

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Doctoral Dissertation for the Degree *Philosophiae Doctor (PhD)* at
the Faculty of Engineering and Science, Specialisation in Renewable Energy

University of Agder
Faculty of Engineering and Science
2020

Doctoral Dissertation at the University of Agder 300
ISSN: 1504-9272
ISBN: 978-82-8427-002-9

Printed by Wittusen & Jensen
Oslo

Crystals are like people, it is the defects in them which tend to make them interesting.

- C. J. Humphreys

Abstract

The conversion efficiency of a photovoltaic device is strongly dependent on the operating temperature. For most devices, the efficiency, and hence the power production, decreases with increasing temperature due to fundamental, material, and process-related factors. Therefore, understanding the thermal behavior of photovoltaic devices is essential to accurately forecast the power production of photovoltaic installations and to optimize devices for different climatic conditions. The thermal behavior of crystalline silicon-based devices is of special interest because of the importance of the technology for industrial applications. This thesis expands the knowledge about temperature dependent performance by investigating how crystal defects influence the thermal behavior of multicrystalline silicon solar cells. Two parameters are given special attention: The temperature coefficient of the open-circuit voltage, which provides information about the temperature sensitivity of the device performance, and the so-called recombination parameter γ, containing information about the underlying physical mechanisms.

In this thesis, temperature dependent performance is studied locally across multicrystalline silicon wafers and solar cells. The temperature sensitivity of grain boundaries, dislocations, and intra-grain regions is investigated at various processing steps, using a novel temperature dependent photoluminescence imaging tool developed during the PhD project. Significant variations in temperature sensitivity is observed for the various crystal defects. Dislocation clusters exhibit an especially interesting thermal behavior, which is discussed in detail. Brick position is found to significantly affect the average temperature sensitivity of wafers and cells, with reduced temperature sensitivity generally observed towards the top of the brick. This is found to arise mainly from the presence of dislocation clusters, because of associated low γ values, and a typically increasing density towards the top of a multicrystalline silicon brick. Finally, the influence of impurity atoms is investigated using a temperature and injection dependent numerical model, relating the recombination parameter γ to impurity recombination in crystalline silicon. The model is used to predict γ for various impurity atoms. Additionally, the temperature coefficient of the open-circuit voltage is predicted without a temperature dependent measurement, enabling more accurate temperature coefficient modeling.

Acknowledgments

Many people have contributed in different ways to the work that comprises this thesis, and made the journey of my PhD absolutely thrilling, wonderful, and challenging - an adventure rich in experiences.

First and foremost, I wish to thank Rune Strandberg for providing great supervision throughout my PhD and for valuable theoretical inputs on problems and experimental observations. Thanks for always being very helpful, for supporting my sometimes impulsive ideas, and for reminding me of the value of "letting things mature". Thanks also go to my co-supervisor, Tor Oskar Sætre, for being supportive and encouraging.

I wish to express my gratitude to Ziv Hameiri for giving me the privilege of doing a research exchange under his supervision. Thanks for being inspiringly humble and friendly, for asking the tough questions, and for the many motivational "Let's save the World". My time at UNSW SPREE really shaped me as a researcher and sparked my motivation.

I would like to thank Jan Ove Odden from REC Solar Norway for providing most of the material used in this work, and for always being very encouraging and helpful with whatever inquiry I had. Thanks to Anders Hope Amundsen for training me on the equipment at REC Solar Norway. Huge thanks also go to Halvard Haug, Marie Syre Wiig, and Rune Søndenå from IFE for fruitful collaboration, for letting me borrow your equipment, and for always being very helpful.

Thanks to the Energy Materials Group at UiA for providing an enjoyable work environment and for valuable feedback on my research. A special thank you goes to Charly Berthod for training me on the PV lab equipment and many engaging conversations about research, food, and ethical dilemmas. Alfredo Sanchez also deserves thanks for blessing me with a lot of dry humor and for many exciting and equation-heavy discussions the past year.

I also wish to thank all the inspiring researchers I met during my research exchange at UNSW SPREE, who generously shared their time and knowledge with me and made me feel welcome. Thanks to the PL Group and the Defect Group for invaluable discussions and suggestions, and SIRF for providing samples for the studies. Shuai Nie deserves a

special thank you for being my temperature dependent PL partner-in-crime, for countless discussions and Skype calls, and for introducing me to the Chinese cuisine. Huge thanks also go to the wonderful friends I made at UNSW SPREE - you made my time in Australia very special.

I wish to thank Antoine and Lorenzo for being the best office mates that one could have. Thanks for many interesting conversations about culture and life in general, and for memorable gatherings outside of work often involving beer. Thanks also go to the "morning crew", Johan Olav and Lorenzo, for sharing the early mornings at H4. Thanks to all the other amazing co-workers and friends who made my time at UiA absolutely unforgettable. Grimstad is an extremely small but special place with high cultural diversity, and I really enjoyed living and working in this environment. Thanks to everyone for hiking and skiing trips, whisky sessions, for keeping my limited Farsi and Nepali skills up to date, and for always making sure that Grimstad had something nice to offer. The list of people is long, so I will simply say, "you know who you are".

Thanks to family and friends at home for accepting and encouraging my decision to move to another country, and for making the effort to stay in touch and support each other from a distance. I love you all very much. Last but not least, thanks to my incredible husband Rasmus, for encouraging me to pursue my dreams, even when it meant living in separate countries. I cannot thank you enough for your love and support, and for filling my life with adventure.

Publications

The following papers have been published or submitted for publication in peer-reviewed international conference proceedings and journals.

A. **S. T. Søndergaard**, J. O. Odden, and R. Strandberg, "Minority carrier lifetime variations in multicrystalline silicon wafers with temperature and ingot position", in: *Proceedings of the 44th IEEE Photovoltaic Specialists Conference*, pp. 2651-2655, 2017. doi: 10.1109/PVSC.2017.8366683.

B. **S. T. Søndergaard**, J. O. Odden, and R. Strandberg, "Temperature dependent suns-V_{oc} of multicrystalline silicon solar cells from different ingot positions", in: *Proceedings of the 7th World Conference on Photovoltaic Energy Conversion*, pp. 2244-2247, 2018. doi: 10.1109/PVSC.2018.8547273.

C. **S. T. Kristensen**, S. Nie, M. S. Wiig, H. Haug, C. Berthod, R. Strandberg, and Z. Hameiri, "A high-accuracy calibration method for temperature dependent photoluminescence imaging", *AIP Conference Proceedings*, vol. 2147, p. 020007, 2019. doi: 10.1063/1.5123812.

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E. **S. T. Kristensen**, S. Nie, C. Berthod, R. Strandberg, J. O. Odden, and Z. Hameiri, "How gettering affects the temperature sensitivity of the implied open circuit voltage of multicrystalline silicon wafers", in: *Proceedings of the 46th IEEE Photovoltaic Specialists Conference*, pp. 0061-0067, 2019. doi: 10.1109/PVSC40753.2019.8980880.

F. S. Nie, **S. T. Kristensen**, A. Gu, R. L. Chin, T. Trupke, and Z. Hameiri, "Photoluminescence-based spatially resolved temperature coefficient maps of silicon wafers and solar cells", *IEEE Journal of Photovoltaics*, vol. 10, no. 2, pp. 585-594, 2019. doi: 10.1109/JPHOTOV.2019.2956261.

G. **S. T. Kristensen**, S. Nie, C. Berthod, R. Strandberg, J. O. Odden, and Z. Hameiri, "Temperature coefficients of crystal defects in multicrystalline silicon wafers", *IEEE Journal of Photovoltaics* , vol. 10, no. 2, pp. 449-457, 2020. doi: 10.1109/JPHOTOV.2020.2968111.

H. **S. T. Kristensen**, A. S. Garcia, S. Nie, Z. Hameiri, and R. Strandberg, "Improved temperature coefficient modeling through the recombination parameter γ", in: *Proceedings of the 47th IEEE Photovoltaic Specialists Conference*, *in press*, 2020.

The following papers were published or submitted for publication during the PhD project but are not included in the thesis.

- C. Berthod, **S. T. Søndergaard**, and J. O. Odden, "Experimental investigation of the optimal ingot resistivity for both the cell performances and the temperature coefficients for different cell architectures", in: *Proceedings of the 7th World Conference on Photovoltaic Energy Conversion*, pp. 293-297, 2018. doi: 10.1109/PVSC.2018.8547804.
- S. Nie, **S. T. Kristensen**, A. Gu, T. Trupke, and Z. Hameiri, "A novel method for characterizating temperature sensitivity of silicon wafers and cells", in: *Proceedings of the 46th IEEE Photovoltaic Specialists Conference*, pp. 0813-0816, 2019. doi: 10.1109/PVSC40753.2019.8980725.
- A. S. Garcia, **S. T. Kristensen**, S. Christiansen, and R. Strandberg, "Temperature coefficients of solar cell parameters at maximum power point", in: *Proceedings of the 47th IEEE Photovoltaic Specialists Conference*, *in press*, 2020.

Contents

Abbreviations

μ-PCD	microwave-induced photoconductive decay
Al_2O_3	aluminum oxide
Al-BSF	aluminum back surface field
AM1.5G	air mass 1.5G
a-Si	amorphous silicon
CCD	charge-coupled device
CdTe	cadmium telluride
CIGC	copper indium gallium selenide
c-Si	crystalline silicon
CSL	coincidence site lattice
CVD	chemical vapor deposition
ESS®	Elkem Solar Silicon®
FBR	fluidized bed reactor
GaAs	gallium arsenide
HP	high performance
IEA	International Energy Agency
LCOE	levelized cost of electricity
mc-Si	multicrystalline silicon
MG-Si	metallurgical-grade silicon
mono-Si	monocrystalline silicon
PC	photoconductance
PERC	passivated emitter and rear cell
PERCT	passivated emitter and rear totally diffused cell
PL	photoluminescence
poly-Si	polycrystalline silicon
PV	photovoltaics
QSS	quasi-steady-state
RAGB	random angle grain boundaries
SAGB	small-angle grain boundaries
SHJ	silicon hetero-junction
SiO_2	quartz
SQ	Shockley-Queisser
SRH	Shockley-Read-Hall
STC	standard test conditions
TC	temperature coefficient
UMG-Si	upgraded metallurgical-grade silicon

Symbols

A_{cal}	conductance calibration constant
A_i	photoluminescence calibration parameter dependent on sample and system
B	radiative recombination coefficient
B_{cal}	conductance calibration constant
C	level of compensation
C_0	element concentration in the melt before solidification
C_{F}	concentration factor
C_{cal}	conductance calibration constant
C_{s}	impurity concentration in the solid phase
D_{l}	diffusion coefficient in the melt
E	energy
E_{C}	energy of conduction band edge
E_{V}	energy of valence band edge
E_{g0}	band gap energy extrapolated to 0 K
E_{g}	band gap energy
E_{t}	defect energy level
G	generation rate
I	current
IV	current-voltage
I_{PL}	intensity of emitted photoluminescence
I_{mpp}	maximum power point current
I_{sc}	short-circuit current
$I_{\mathrm{PL},xy}$	local photoluminescence intensity
J	current density
J_0	diode saturation current density
J_{ph}	photogenerated current density
J_{sc}	short-circuit current density
$J_{0,\mathrm{rad}}$	pre-factor of the dark current density in the radiative limit
$J_{\mathrm{sc,1sun}}$	short-circuit current density at 1 Sun
L	minority carrier diffusion length
N_{A}	acceptor concentration
N_{A}^-	ionized acceptor concentration
N_{C}	effective density of states in the conduction band
N_{D}	donor concentration
N_{D}^+	ionized donor concentration
N_{V}	effective density of states in the valence band
N_{dop}	doping concentration
N_{eff}	effective doping concentration
N_{t}	defect concentration
P_{in}	incoming power
P_{mpp}	maximum power point power
$R_{\mathrm{f,808\,nm}}$	front surface reflection at 808 nm
S_{n0}	surface recombination velocity of electrons
S_{p0}	surface recombination velocity of holes
T_{c}	cell temperature
U_{eff}	effective recombination rate
V	voltage
V_{dark}	sample voltage in the dark
V_{ill}	sample voltage during illumination
V_{mpp}	maximum power point voltage

$V_{\mathrm{oc,1sun}}$	open-circuit voltage at 1 Sun
V_{oc}	open-circuit voltage
W	sample thickness
$\Delta\sigma$	photoconductance
Δn_{xy}	local excess carrier concentration
Ω_{emit}	solid angle of emission
Σ	coincidence index
β_Y	temperature coefficient of the device parameter Y
β_{FF}	temperature coefficient of the fill factor
$\beta_{J_{\mathrm{sc}}}$	temperature coefficient of the short-circuit current density
$\beta_{P_{\mathrm{mpp}}}$	temperature coefficient of the maximum power point power
$\beta_{V_{\mathrm{oc}}}$	temperature coefficient of the open-circuit voltage
$\beta_{iV_{\mathrm{oc}}}$	temperature coefficient of the implied open-circuit voltage
δ	boundary layer thickness
η	conversion efficiency
γ	recombination parameter
γ_{xy}	local recombination parameter
μ_n	electron mobility
μ_p	hole mobility
ν	growth rate
$\nu_{\mathrm{th},n}$	thermal velocity of electrons
$\nu_{\mathrm{th},p}$	thermal velocity of holes
ϕ	photon flux
σ	conductance
σ_{dark}	conductance in the dark
σ_{ill}	conductance during illumination
σ_n	electron capture cross section
σ_p	hole capture cross section
τ_{Auger}	Auger lifetime
τ_{SRH}	Shockley-Read-Hall lifetime
τ_{bulk}	bulk lifetime
$\tau_{\mathrm{eff},xy}$	local effective lifetime
τ_{eff}	effective lifetime
τ_{rad}	radiative lifetime
τ_{surface}	surface lifetime
τ_{n0}	capture time constant of electrons
τ_{p0}	capture time constant of holes
c	speed of light in vacuum
f_{s}	solidified fraction
h	Planck constant
iV_{oc}	implied open-circuit voltage
$iV_{\mathrm{oc},xy}$	local implied open-circuit voltage
k	Boltzmann constant
k_0	equilibrium segregation coefficient
k_{eff}	effective segregation coefficient
n	total electron concentration
n_0	electron concentration in thermal equilibrium
n_1	Shockley-Read-Hall density of electrons
n_{maj}	majority carrier concentration
n_i	intrinsic carrier concentration
p	total hole concentration
p_0	hole concentration in thermal equilibrium
p_1	Shockley-Read-Hall density of holes
q	elementary charge
Δn	excess electron concentration
Δn_{PC}	excess carrier concentration in inductive coil area
Δp	excess hole concentration
ERE	external radiative efficiency
ERE_{oc}	external radiative efficiency at open-circuit conditions
FF	fill factor

Chapter 1

Introduction

1.1 Solar photovoltaics in perspective

The modern world is strongly dependent on the exploitation of energy. With a continuously growing world population and the aim of energy access for all, our appetite for energy does not seem to decrease any time soon. Up until now, our needs have mainly been satisfied using fossil fuels. However, the detrimental environmental, climatic, and social impacts of conventional fossil fuel-based energy production are becoming increasingly apparent. This led most nations of the world to sign the Paris Agreement in 2016, which marked a joined pledge to combat climate change by limiting the global temperature rise to well below 2 °C compared to pre-industrial levels [1]. The transition to sustainable and renewable energy production using a range of energy technologies is a central element for this goal to be successful.

Despite the importance of sustainable and renewable energy sources, global energy and power production is still dominated by fossil fuels [2]. By the end of 2018, renewable sources accounted for an estimated 26.2 % of the global power production [3]. However, the share of renewable energy is increasing, with net capacity additions surpassing fossil fuels for the past four consecutive years [3]. Additionally, according to the International Energy Agency (IEA), global renewable power capacity is expected to expand by 50 % between 2019 and 2024 [2].

Solar photovoltaics (PV) constitutes an important part of the transition to renewable and sustainable energy production. With a globally installed capacity of 505 GW in 2018 [3], the technology accounted for 21 % of the total renewable power capacity including hydropower, and 41 % excluding hydropower. With an impressive growth rate, solar PV is expected to lead the expansion of the global renewable power capacity in the coming years due to increasing economical feasibility [2]. This is a result of technological improvements and increased market competition mainly facilitated by China, which accounted for 45 %

of the global PV capacity additions in 2018 [3]. In 2018, module prices of crystalline silicon (c-Si), the dominant industrial PV technology, fell by up to 32 % compared to 2017 [3]. Additionally, in some countries, the levelized cost of electricity (LCOE) of operating PV plants was close to or below retail electricity prices, and in some cases even below wholesale electricity prices [3]. The continuous global implementation of solar PV is based on further reductions in the LCOE to ensure cost-competitiveness, which relies on continuous research and technological improvements of both existing and new PV technologies.

1.2 Motivation

The power production from PV modules is strongly affected by the operating conditions, such as the incoming irradiance, module temperature, humidity, and wind speed [4, 5]. Since the climate can vary significantly depending on the location of the module [4–6], knowledge about the influence of operating conditions is essential to make accurate power predictions, as well as to optimize PV devices for different climatic conditions.

The performance of a solar cell generally decreases with increasing temperature [7–11], with the exact temperature sensitivity depending on various factors such as the semiconductor material, the recombination processes[1] in the device, and other physical parameters [6, 12–14]. Most important are the mechanisms that affect the temperature sensitivity of the voltage of the cell, since it accounts for approximately 80-90 % of the total thermal behavior [14]. The temperature sensitivity of the voltage is mainly determined by the cell quality but also by the dominant recombination mechanisms in the cell [11].

Temperature dependent PV performance has generally been studied for various cell technologies (see Refs. [7, 8, 10–12, 15–20] for examples). Special attention has been given to c-Si based solar cells [8, 13, 21–26] which have dominated the commercial PV market for decades and continue to play an important role [27]. Knowledge about the temperature sensitivity of this technology is, therefore, of special importance for industrial applications.

As previously mentioned, the temperature sensitivity of PV device performance is influenced by the dominant recombination processes in the device. For c-Si solar cells, the dominant process is most often recombination through crystal defects, such as impurity atoms, dislocations, and grain boundaries in the crystal, which will be elaborated in Secs. 2.2.2-2.2.4. The influence of crystal defects on the temperature sensitivity of c-Si wafers and cells has only been sparsely studied [28–30], facilitated by recently developed

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[1] Recombination is a process where the generated energy in the solar cell is lost as heat or light, instead of converted into electrical energy. The recombination processes present in c-Si solar cells will be presented in Sec. 2.1.1.

spatially resolved temperature dependent characterization techniques [28, 30–34]. The results highlight spatial variations in temperature sensitivity across c-Si wafers and cells and various contributions for different types of crystal defects. Additionally, a study from Berthod *et al.* on compensated multicrystalline silicon (mc-Si) solar cells, observed variations in temperature sensitivity for cells originating from different brick heights[2] [35]. This was suggested to arise from variations in the composition of crystal defects along the brick.

The as-yet limiting studies illustrate the importance of understanding variations in temperature sensitivity to correctly understand temperature dependent device performance. The influence of crystal defects is gaining attention; however, the mechanisms causing varying temperature sensitivity across c-Si wafers and cells, variations with brick height, as well as the specific influence of various defects, have yet to be understood.

1.3 Objective and research questions

The general objective of this thesis is to expand the knowledge about temperature dependent PV device performance by investigating the influence of crystal defects on the thermal behavior of mc-Si wafers and solar cells. Variations in temperature sensitivity and the responsible mechanisms are explored both through experimental investigations and modeling. The aim of this thesis is to answer the following questions:

A. What mechanisms cause variations in temperature sensitivity with brick height observed for mc-Si solar cells?

B. What causes spatial variations in temperature sensitivity across c-Si wafers and solar cells?

C. How is the temperature dependent PV device performance influenced by crystal defects in mc-Si such as impurity atoms, grain boundaries, and dislocations?

1.4 Outline

The thesis is divided into six chapters and outlined in the following way:

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[2] Mc-Si solar cells are produced from an ingot, which is cut into smaller blocks (a brick), from where a large number of wafers are cut and processed into solar cells. The production process of mc-Si solar cells will be described in detail in Sec. 2.2.1.

Chapter 1 contextualizes solar PV and describes the motivation, objectives, and research questions of the current work.

Chapter 2 presents the information about multicrystalline silicon solar cells, necessary to understand the appended articles of this thesis. First, the fundamentals of PV device performance is introduced. The production of mc-Si solar cells is then presented, as well as the associated crystal defects and their influence on device performance. Finally, the distinct characteristics of compensated silicon are discussed.

Chapter 3 discusses the temperature sensitivity of PV devices. First, the fundamental thermal behavior of PV devices is briefly introduced. Then, temperature coefficients (TCs) are presented as a means of quantifying temperature dependent PV performance. Special focus is given to the temperature sensitivity of the voltage of the solar cell and the role of a recombination parameter γ, which will be explained later. Finally, a review of experimental observations on mc-Si wafers and cells is provided.

Chapter 4 presents the main experimental methods used throughout this PhD project, including both standard PV characterization methods and a novel temperature dependent photoluminescence imaging tool developed during the PhD project. Additionally, general details about the studied samples are provided.

Chapter 5 summarizes the main findings of each of the papers included in this thesis. Papers A and B investigate the influence of brick position on the temperature sensitivity of c-Si wafers and solar cells. Paper C presents a novel temperature dependent photoluminescence imaging system, enabling a detailed characterization of the local temperature sensitivity of c-Si wafers. Papers E and G investigate the local temperature sensitivity of crystal defects, and Papers D and F study further the role of dislocations. Finally, Paper H elaborates on the characteristics of the recombination parameter γ and the relationship with impurity atoms in the silicon material.

Chapter 6 summarizes the main findings and contributions of the current work and their potential implications. Additionally, an outlook for future work is provided.

Finally, eight papers are included in the appendices. The papers have been published or submitted for publication in peer-reviewed international conference proceedings and journals. The presented versions differ from their published versions only in formatting.

Chapter 2

Multicrystalline silicon solar cells

The aim of this chapter is to present the reader with the information about mc-Si solar cells necessary to understand the appended articles. The most important information is the characteristics of crystal defects and their influence on PV device performance. In order to understand this, fundamental PV operation is first presented with a focus on recombination processes in the PV material. Additionally, essential device parameters are introduced. After discussing crystal defects in mc-Si, the distinct characteristics of compensated mc-Si are presented.

2.1 Fundamental photovoltaic operation

The fundamental operating principle of a PV device is the conversion of electromagnetic energy from light into electrical energy. Before this process is described, some general characteristics of the semiconductor, from which a PV device is made, will be briefly introduced.

A semiconductor is characterized by a certain band structure that determines the allowed energy states of electrons in the crystal. The energy bands relevant for PV operation are illustrated in Fig. 2.1, which shows the valence band (E_V) in which the electrons are in bound states in the crystal, and the conduction band (E_C) where the electrons can move freely and participate in conduction. The energy bands are separated by a range of forbidden states, where the energy separation is denoted the band gap energy (E_g). A bound electron in E_V can be raised to E_C, leaving behind an empty state in E_V. Other electrons in E_V can move into this empty space and thus contribute to the conduction. The absence of an electron is commonly referred to as a hole and viewed as a positively charged particle that can move around freely in E_V. Both electrons and holes are referred to as *charge carriers*.

The creation of electron-hole pairs is called *generation* and can be facilitated either

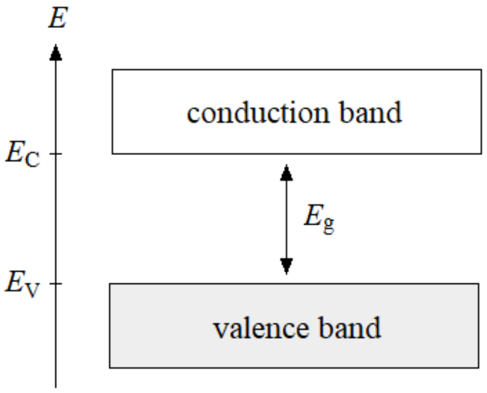

Figure 2.1: Valence and conduction bands of a semiconductor.

through thermal or optical processes. In thermal equilibrium, thermal generation of electron-hole pairs leads to the equilibrium electron and hole concentrations n_0 and p_0. Additionally, optical generation of electron-hole pairs results in an excess concentration of electrons (Δn) and holes (Δp) in the material. The total carrier concentrations of electrons and holes in the semiconductor are therefore given by $n = n_0 + \Delta n$ and $p = p_0 + \Delta p$, respectively.

The conversion of electromagnetic energy to electrical energy in a PV device takes place through the following processes: i) Generation of electron-hole pairs in the PV device by absorption of photons, ii) transport of the generated charge carriers to their respective contacts in the device, and iii) extraction of the charge carrier energy in an external circuit. The efficiency of the conversion process is determined by the characteristics of i)-iii), thus optimizing these processes is an essential objective of PV research. Because of the relevance to this PhD work, the current chapter will focus on process ii), more specifically, the so-called *recombination* mechanisms that offer a path for the electron-hole pairs to release their energy, either through photon or phonon emission, before it is extracted in an external circuit.

2.1.1 Recombination processes in multicrystalline silicon

Several recombination pathways exist in mc-Si, related to the silicon material itself and defects therein, and the wafer and cell processing. The various recombination mechanisms can be divided into *intrinsic* and *extrinsic* mechanisms.

The intrinsic recombination processes include radiative recombination and Auger recombination. Radiative recombination denotes the de-excitation of an electron from E_C to E_V through emission of a photon. The rate of recombination can be described by [9]

$$U_{\mathrm{rad}} = B(np - n_i^2), \tag{2.1}$$

where B is the radiative recombination coefficient which reflects the quantum-mechanical probability of transition [36] and n_i is the intrinsic carrier concentration.

Auger recombination is a non-radiative recombination process that involves three carriers [37]. When an electron-hole pair recombines, the energy is transferred to a third carrier, an electron in E_C, or a hole in E_V, which then relaxes to the valence or conduction band edge through thermalization. The Auger recombination rate can be described by

$$U_\mathrm{Aug} = C_n\,(n^2p - n_0^2p_0) + C_p\,(np^2 - n_0p_0^2), \tag{2.2}$$

where C_n and C_p are Auger coefficients of electrons and holes, respectively.

The extrinsic recombination mechanisms originate from both bulk properties as well as wafer and cell processing steps. An essential recombination mechanism in mc-Si is recombination through defects, also called Shockley-Read-Hall (SRH) recombination [38, 39]. Defects include both impurity atoms and structural defects, which create discrete energy levels (E_t) within the band gap. The origination and characteristics of defects in mc-Si will be discussed in Sec. 2.2, whereas the statistical description of the recombination process will be presented in the current section. A defect level E_t can be occupied either by an electron or a hole, leading to four fundamental processes, as illustrated in Fig. 2.2. When a defect level is occupied by an electron, the electron can either be emitted into the E_C [process (1) in Fig. 2.2], or the defect level can capture a hole from the E_V [process (3)]. When E_t is unoccupied (a hole is present), an electron can be captured by E_t [process (2)], or the hole can be emitted into E_V [process (4)]. Therefore, the defect level can act as a center for both recombination, generation, and trapping of a charge carrier, all facilitated by different two-step processes. Recombination takes place through the processes (2) and (3), generation is facilitated through (4) and (1) [or (1) and (4)], and trapping occurs through either (2) and (1) or (3) and (4). In the trapping process, the charge carrier is not lost but momentarily unable to be extracted.

Regardless of the capture and emission processes, the recombination rate related to E_t can be described using SRH statistics [38,39]. The net recombination rate is given by

$$U_\mathrm{SRH} = \frac{np - n_i^2}{\tau_{n0}(p + p_1) + \tau_{p0}(n + n_1)}, \tag{2.3}$$

where τ_{n0} and τ_{p0} denote the capture time constants of electrons and holes, defined by

$$\tau_{n0} = (N_\mathrm{t}\sigma_n\nu_{\mathrm{th},n})^{-1}, \tag{2.4}$$

$$\tau_{p0} = (N_\mathrm{t}\sigma_p\nu_{\mathrm{th},p})^{-1}, \tag{2.5}$$

where N_t is the defect concentration, σ_n and σ_p are the capture cross sections of electrons and holes, and $\nu_{\mathrm{th},n}$ and $\nu_{\mathrm{th},p}$ are the thermal velocities of electrons and holes, respectively.

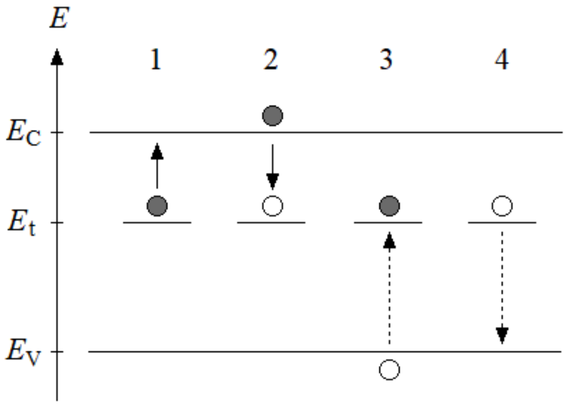

Figure 2.2: Fundamental processes of SRH recombination. The gray circles represent electrons and the white circles represent holes.

The parameters n_1 and p_1 are SRH densities defined by

$$n_1 = N_\mathrm{C} \exp\left(-\frac{E_\mathrm{C} - E_\mathrm{t}}{kT_\mathrm{c}}\right), \tag{2.6}$$

$$p_1 = N_\mathrm{V} \exp\left(-\frac{E_\mathrm{t} - E_\mathrm{V}}{kT_\mathrm{c}}\right), \tag{2.7}$$

where N_C and N_V denote the effective density of states in the conduction and valence bands, k is the Boltzmann constant, and T_c is the cell temperature. n_1 and p_1 are the densities of electrons and holes when the Fermi level coincides with E_t. The parameters τ_{n0}, τ_{p0}, and E_t can be regarded the finger print of the defect, since they mainly determine the SRH recombination rate. Fig. 2.3 illustrates E_t for various impurities in the silicon band gap. The recombination rate is largest when E_t is near mid-gap, as Eqs. (2.3), (2.6), and (2.7) demonstrate. Additionally, the recombination rate is greatly influenced by N_t.

Another extrinsic recombination mechanism is surface recombination, which originates from defect states introduced at the surfaces of the material. The defect states arise from the discontinuity of the silicon crystal lattice, leading to dangling bonds. Unlike other defect states, surface states typically introduce a continuously distributed range of states in the band gap close to the surface of the semiconductor. The surface recombination rate can be described through an extended SRH statistics, yielding [9]

$$U_\mathrm{surface} = \frac{S_{n0}\, S_{p0}(np - n_i^2)}{S_{n0}(n + n_1) + S_{p0}(p + p_1)}, \tag{2.8}$$

where S_{n0} and S_{p0} are surface recombination velocities of electrons and holes, respectively. Additional extrinsic losses can be introduced during wafer and cell processing. Since the aim of the current work is to study the influence of bulk defects, processing losses will not be addressed in detail.

The different recombination mechanisms have various relative importance in a PV device. Because of the indirect band gap nature of c-Si, the probability of radiative re-

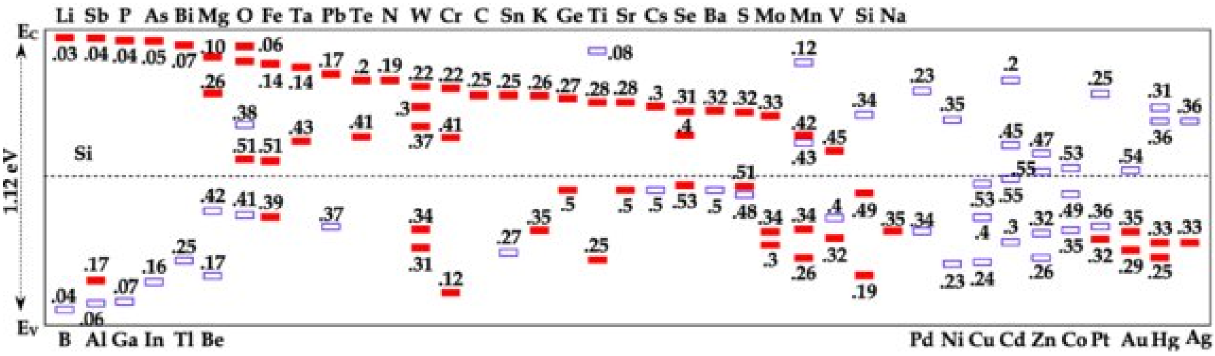

Figure 2.3: Energy levels of various impurity atoms in the silicon band gap [40].

combination is reduced, since the transition process involves both a photon and a phonon. Auger recombination is strongly dependent on the carrier concentration. Therefore, the process only becomes significant at high injection, which applies when $\Delta n \gg N_{\text{dop}}$, where N_{dop} denotes the semiconductor doping concentration. Therefore, the extrinsic recombination mechanisms often play a dominating role in c-Si devices. Surface recombination can be significantly reduced by using high quality passivation routines, reducing the number of dangling bonds at the silicon surfaces. Thus, SRH recombination can often be regarded as the dominant recombination mechanism in c-Si at low and mid-range injection conditions, provided the material has received a high quality surface passivation.

2.1.2 Essential parameters for device characterization

After briefly reviewing fundamental PV operation, the essential parameters used for device characterization are presented.

2.1.2.1 Effective lifetime

From each of the recombination rates introduced in Subsec. 2.1.1, an associated carrier lifetime can be obtained. The carrier lifetime describes the average time that a carrier spends in an excited state before recombining through the specific process. Assuming an insignificant number of trapping centers, i.e. $\Delta n = \Delta p$, the carrier lifetime of process ν can be expressed as

$$\tau_\nu = \frac{\Delta n}{U_\nu}, \tag{2.9}$$

where U_ν denotes the recombination rate of the process ν. Several or all of the recombination processes presented in Sec. 2.1.1 might be present simultaneously in the material, resulting in an effective carrier lifetime (τ_{eff}). This parameter is an important material quality indicator in early processing stages. Since the recombination processes are independent quantities, τ_{eff} can be expressed as

$$\frac{1}{\tau_{\text{eff}}} = \left(\frac{1}{\tau_{\text{rad}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{SRH}}}\right) + \frac{1}{\tau_{\text{surface}}}, \tag{2.10}$$

$$= \frac{1}{\tau_{\text{bulk}}} + \frac{1}{\tau_{\text{surface}}}, \tag{2.11}$$

where τ_{rad} is the radiative lifetime, τ_{Auger} is the Auger lifetime, τ_{SRH} is the SRH lifetime, τ_{surface} is the surface lifetime, and τ_{bulk} is the bulk lifetime. Because of the importance of SRH recombination in the current work, the quantification of the SRH lifetime is explicitly presented as [41]

$$\tau_{\text{SRH}} = \frac{\tau_{n0}(p_0 + p_1 + \Delta n) + \tau_{p0}(n_0 + n_1 + \Delta n)}{p_0 + n_0 + \Delta n}, \tag{2.12}$$

where the electron and hole densities n and p have been replaced by $n = n_0 + \Delta n$ and $p = p_0 + \Delta p$.

2.1.2.2 Cell parameters

The performance of a finished solar cell is commonly characterized by constructing a current-voltage (IV) curve of the device. An example of an IV curve is illustrated in Fig. 2.4 (blue curve) for a mc-Si solar cell. The IV curve is characterized by the following cell parameters: The short-circuit current (I_{sc}) denotes the current of the cell in short-circuit, and therefore represents the maximum extractable current. The open-circuit voltage (V_{oc}) is the voltage of the cell in open-circuit, and thus represents the maximum extractable voltage. It is physically impossible to simultaneously operate the cell at both I_{sc} and V_{oc}; however, a maximum power (P_{mpp}) can be extracted, defined as

$$P_{\text{mpp}} = I_{\text{mpp}} V_{\text{mpp}}, \tag{2.13}$$

where I_{mpp} and V_{mpp} denote the maximum power point current and voltage, respectively. The maximum power point is illustrated on Fig. 2.4. The fill factor (FF) is defined as

$$FF = \frac{V_{\text{mpp}} I_{\text{mpp}}}{V_{\text{oc}} I_{\text{sc}}}, \tag{2.14}$$

and hence represents the "squareness" of the IV-curve. Finally, the conversion efficiency (η) is defined as

$$\eta = \frac{P_{\text{mpp}}}{P_{\text{in}}}, \tag{2.15}$$

where P_{in} denotes the incoming power from the sunlight.

The characteristic cell parameters I_{sc}, V_{oc}, and FF reflect various information about processes in the material, thus providing information about how to optimize the device. The I_{sc} and the V_{oc} depend on properties related to the silicon material, including defects

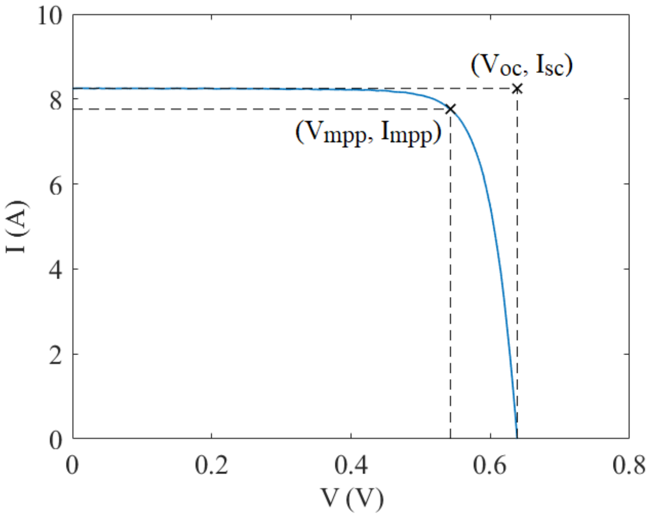

Figure 2.4: Example of an IV-curve of a mc-Si solar cell.

in the material. The FF depends on I_{sc} and V_{oc}, but is also influenced by parasitic resistance effects such as series and shunt resistance.

The importance of τ_{eff} can now be further illustrated. It can be related to the V_{oc} through the implied V_{oc} (iV_{oc}), which is derived from the carrier concentration and hence gives information about the maximum possible V_{oc} of the material. The iV_{oc} can be quantified through [42]

$$iV_{\mathrm{oc}} = \frac{kT_{\mathrm{c}}}{q} \ln\left[\frac{\Delta n(\Delta n + N_{\mathrm{dop}})}{n_i^2}\right], \tag{2.16}$$

where q denotes the elementary charge. τ_{eff} can be related to Δn through $\tau_{\mathrm{eff}} = \Delta n/U_{\mathrm{eff}}$, where U_{eff} is the effective recombination rate, illustrating the relationship between τ_{eff} and iV_{oc}.

2.2 Crystal defects in multicrystalline silicon

In this thesis, mc-Si wafers and solar cells are studied. To understand their performance, the production method of mc-Si will first be elaborated. Then, the characteristics of crystal defects, as well as their influence on device performance, will be discussed.

2.2.1 Production of multicrystalline silicon solar cells

C-Si is produced from quartz (SiO_2), which is refined using carbon-based reducing agents to become metallurgical-grade silicon (MG-Si) with a purity of 98-99 % (1-2 N) (see Ref. [43] for an overview of the c-Si production chain). The MG-Si is processed further to achieve a purity of 6-8 N, either through the Siemens process [a chemical vapor deposition (CVD) technique], using a fluidized bed reactor (FBR), or through chemical refinement to achieve upgraded metallurgical-grade silicon (UMG-Si). At this stage, the material is called polycrystalline silicon (poly-Si). From poly-Si, different types of c-Si ingots can be produced, classified depending on crystallinity. Monocrystalline silicon (mono-Si) ingots are produced either through Czochralski pulling or a float zone process, resulting in a single crystal material with a relatively high conversion efficiency. However, the production methods are highly energy demanding and result in high production costs. Mc-Si ingots have a multi-crystal nature and offer a cost-effective alternative, however, compromised by a higher density of structural defects, impurities, and precipitates, leading to lower conversion efficiencies [44–49].

Mc-Si is most commonly produced by crystallizing a silicon feedstock through the process of directional solidification [50]. In this method, the feedstock, typically poly-Si produced by the Siemens process, is melted in a crucible under vacuum or in an argon atmosphere. The material is then crystallized from the bottom of the crucible, by decreasing the temperature while maintaining a temperature gradient from the bottom to the top of the crucible. Controlled cooling and low growth rates are essential to ensure a planar growth front and avoid residual stress in the material [50].

Defects enter the mc-Si ingot through various pathways. Although the poly-Si feedstock is relatively pure, impurity atoms will be present. During crystallization, most impurities in the silicon melt will segregate in the liquid phase, which results in a higher impurity concentration at the top of the ingot. The origin of impurity atoms and impurity segregation during crystallization will be described further in Sec. 2.2.2. As the system cools down, in-diffusion of impurities from the crucible and coating will result in a higher impurity concentration at the edges of the ingot [51, 52]. Additionally, structural defects such as grain boundaries and dislocation clusters are formed in the material during crystallization and cool-down [53–55]. The level of structural defects can be controlled through grain engineering, which is utilized in high performance (HP) mc-Si, where decreased grain size is prioritized. This leads to reduced dislocation growth, which improves final cell performance [56–58]. The influence of various crystal defects on material properties will be elaborated in the following sections.

The solidified ingot is cut into bricks, on which a top and bottom cut is performed to remove areas with high impurity concentrations. The bricks are then cut into wafers that receive several processing steps in order to become finished solar cells. Typical cell processing steps include damage removal from the wafer cutting, texturing, emitter diffusion, passivation, and finally, contact formation. The emitter diffusion step acts as a gettering process, where impurities with high diffusivity tend to move into selected (and less detrimental) areas, leaving a lower impurity concentration in the remaining areas [59–61]. Passivation with hydrogen-rich layers and consequently contact formation

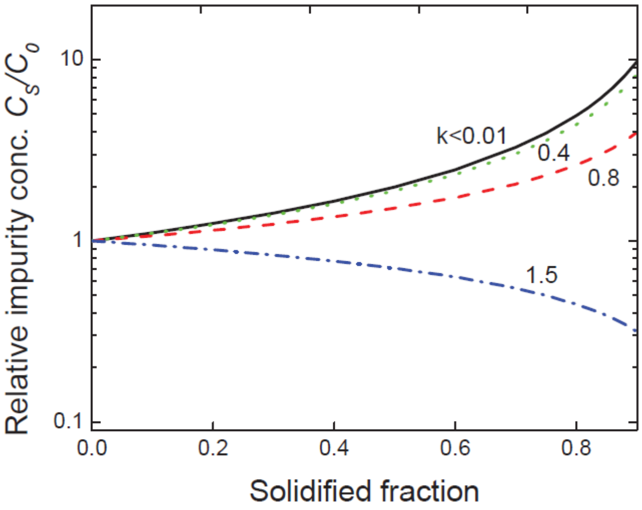

Figure 2.5: Relative impurity concentration in a c-Si ingot as a function of solidified fraction for various values of k [43]. Note that k in this figure corresponds to k_{eff} in Sec. 2.2.2.

greatly enhances material quality since the high-temperature process enables hydrogen to diffuse into the sample and passivate defects thus improve the overall material quality (see Ref. [47] as an example).

2.2.2 Impurities

Impurity atoms are point defects in the silicon lattice, introduced into the material during several steps in the solar cell production chain. Impurity atoms include both contamination sources, which are detrimental to material quality, and dopant atoms, which are intentionally introduced to enhance the conductivity of the silicon material. This section will focus on impurity contamination.

The impurity contamination sources in mc-Si ingots mainly arise from the feedstock quality, the crucible, and the coating [51,52,62,63], where contamination from the crucible and coating systems typically dominate the final impurity concentrations [63] (see Ref. [43] for an overview of contamination sources which are introduced throughout the c-Si production chain). During ingot crystallization, impurities in the melt tend to segregate in the liquid phase because of different solubilities in the solid and liquid phases. This leads to an uneven distribution of impurities in the crystallized ingot. Segregation of impurities in the silicon melt can be described using the Scheil equation, from where the impurity concentration in the solid phase (C_{s}) can be calculated as a function of the solidified fraction (f_{s}) through [64]

$$C_{\text{s}} = k_{\text{eff}}\, C_0 (1 - f_{\text{s}})^{(k_{\text{eff}}-1)}, \tag{2.17}$$

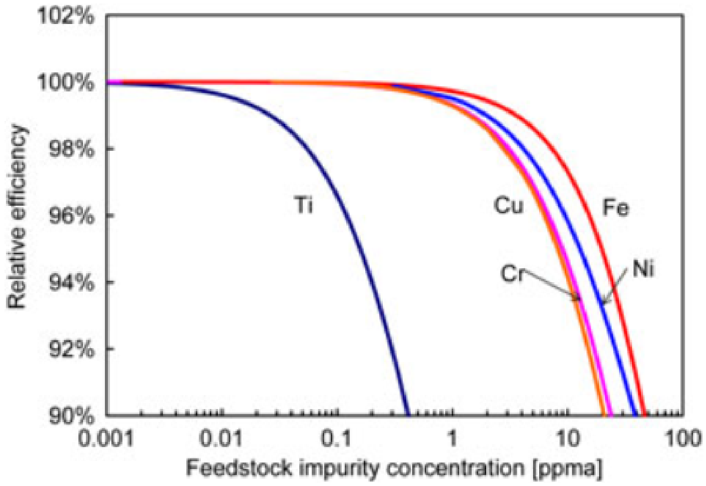

Figure 2.6: Modeled relative efficiency of a p-type mc-Si solar cell as a function of impurity concentration for various impurity atoms at 90 % ingot height [45].

where C_0 is the concentration of the element in the melt before solidification and k_{eff} is the effective segregation coefficient given by

$$k_{\mathrm{eff}} = \frac{k_0}{k_0 + (1 - k_0)\exp(-\frac{\nu\delta}{D_l})}, \tag{2.18}$$

where k_0 is the equilibrium segregation coefficient, defined as the ratio of the impurity concentration in the solid to the concentration in the liquid, ν is the growth rate, δ is the boundary layer thickness, and D_{l} is the diffusion coefficient in the melt. If $k_{\mathrm{eff}} < 1$, a higher concentration of impurities will be present in the melt compared to the solidified part, resulting in an increasing impurity concentration towards the top of the ingot. This is illustrated in Fig. 2.5, showing the relative impurity concentration in a c-Si ingot as a function of f_{s} for various values of k_{eff} (note that $k = k_{\mathrm{eff}}$ in the figure). For most impurities in mc-Si, $k_{\mathrm{eff}} < 1$ (see Tab. 2.1 in Ref. [43] as an example), and the impurity concentration will increase towards the top of the solidified ingot. Some exceptions exist, such as oxygen that has a segregation coefficient close to 1, resulting in a decreasing concentration with ingot height [65, 66].

In addition to the impurities that segregate during crystallization, in-diffusion of impurities from the crucible and back diffusion from the top of the ingot during cool-down increase the final impurity concentrations at the ingot edges, most prominent for fast diffusing atoms. The final result is an uneven impurity distribution along the brick height. As examples, this is demonstrated by Macdonald *et al.* for transition metals [67] and by Kvande *et al.* for iron [68], where the back-diffusion of iron from the top of the ingot is shown.

Impurity atoms, especially transition metals, have a detrimental impact on mc-Si solar

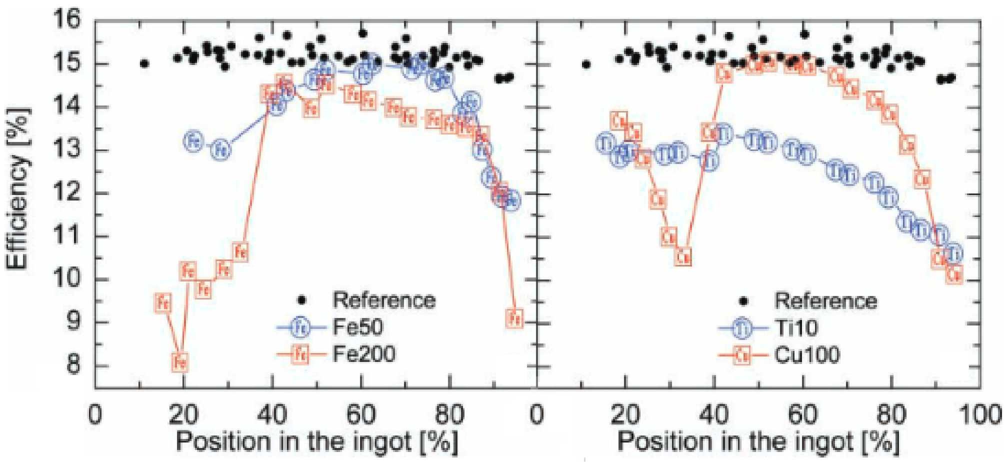

Figure 2.7: Measured cell efficiencies of p-type mc-Si solar cells as a function of ingot position contaminated with iron, titanium, and copper (modified from [44]).

cell performance [44, 45, 48, 66, 69, 70]. Fig. 2.6 shows the modeled relative efficiency of a p-type mc-Si cell as a function of impurity concentration for various impurity atoms at 90 % ingot height [45]. The figure illustrates the sensitivity of cell performance to the presence of impurity atoms. Additionally, Fig. 2.7 shows measured cell efficiencies as a function of ingot height for p-type mc-Si cells contaminated with various impurity atoms [44]. The numbers after the element symbols denote impurity concentrations in ppm wt. The impurity segregation and in-diffusion of specific metals are clearly visible from the distinct shapes found for various contamination sources.

2.2.3 Grain boundaries

A grain boundary is an interface that separates crystallites of different orientations in the mc-Si material. Grain boundaries can be categorized into three groups depending on the degree of symmetry between the surrounding crystallites (from high to low): Small-angle grain boundaries (SAGB), coincidence site lattice (CSL) grain boundaries, and random angle grain boundaries (RAGB). The degree of symmetry is determined by a misorientation angle, describing the rotation of the two crystallites compared to each other. The electrical activity depends on the structure of the grain boundary and the impurity contamination.

SAGB separate crystallites with relatively small differences in orientation. This type of grain boundary has been found to be most detrimental to electrical properties, according to Chen *et al.* [71], who also found the electrical activity to increase with increasing misorientation angle until ∼ 2 °. CSL grain boundaries constitute a group of boundaries that separate crystallites with some misorientation between them; however, still with common lattice points. The number of common lattice points is described by a coincidence index Σ, where a decreasing Σ describes increasing atomic coincidence. A low Σ value, therefore, implies a high degree of symmetry between crystallites. Metal precipitate decoration of the grain boundaries have been found to generally increase with decreasing coincidence (increasing Σ) [72], as well as electrical activity [73]. CSL grain boundaries are the most common grain boundary type found in HP mc-Si [74], which constitutes most of the material studied in the current work. RAGB separate grains without common lattice points. They have higher electrical activity than CSL [71], but are found to a lesser extend [75].

Uncontaminated grain boundaries have been found to show little electrical activity [71]. However, most grain boundaries can easily become decorated with impurity atoms and their precipitates, resulting in detrimental recombination sites that can limit final cell performance [49,72,73,76–79]. This can in some cases be mitigated by performing various cell processing steps. Different grain boundaries have been found to respond differently to various processing steps, but some general trends apply: Generally, most grain boundary types become recombination active during gettering, which can generally be reversed by hydrogenation [79–82]. However, some exceptions exist: $\Sigma 3$ boundaries have been observed to remain inactive both in as-cut, gettered, and hydrogenated states [80]. In contrast, some CSL grain boundaries and SAGB have been found to remain recombination active after hydrogenation [80,81,83]. Additionally, grain boundaries in the bottom of an ingot generally seem to remain active even after hydrogenation [82].

2.2.4 Dislocations

A dislocation is an incomplete plane of atoms in the crystal lattice that forms during growth as a result of plastic deformation of the crystal [84]. At sufficiently high temperatures, dislocations can move around in the crystal to facilitate stress release. The concentration and properties of dislocations in mc-Si are strongly influenced by the nucleation conditions [53, 85–87]. For instance, Stokkan *et al.* observed that dislocation clusters in HP mc-Si originate from CSL boundaries and terminate at RAGB [88].

Dislocations multiply and grow during solidification, leading to an increased density of dislocations and dislocation clusters towards the top of an ingot [53,88,89]. Consequently, dislocation clusters can cover a relatively large area of mc-Si wafers, especially wafers from the top of an ingot. As previously mentioned, the density of dislocation clusters can be greatly reduced through grain engineering, which is applied for HP mc-Si. However, dislocation clusters are still considered most detrimental to cell performance, for the following reasons: First, as previously mentioned, they tend to intensify and expand throughout the ingot, leading to clusters of relatively large lateral size on wafers and cells. Secondly, their interaction with impurities and their precipitates has been observed to lead to enhanced and detrimental recombination sites [72,78,90]. Kveder *et al.* modeled the dislocation-impurity interaction and found that this interaction can lead to intensified recombination [91]. Finally, and perhaps most importantly, dislocations generally cannot be effectively gettered and hydrogenated in contrast to intra-grain areas and most grain boundaries. Dislocations have been found to show increased recombination strength after gettering [47,61,92,93], whereas the effect of hydrogenation is more unclear. Some studies have reported reduced recombination strength after hydrogenation [78, 94] where others have found that dislocations remain recombination active [47,93]. Interestingly, Sio *et al.* observed that as-grown dislocations in HP mc-Si cells were inactive before gettering but became activated by the gettering and hydrogenation processes [93]. Finally, it should be mentioned that the recombination activity has been observed to vary significantly for different dislocation clusters [95,96], highlighting the complex nature of the defect.

Dislocations have a strong impact on material quality and final cell performance, as demonstrated in Refs. [48,49,70,81]. As an example, Mitchell *et al.* found that dislocation density and bulk lifetime were good predictors of passivated emitter and rear cell (PERC) performance [89]. Additionally, Needleman *et al.* modeled the impact of dislocation clusters on state-of-the-art p-type mc-Si solar cells and found that final cell efficiency could be reduced by 0.25 % absolute by dislocation clusters, mainly arising from reductions in I_{sc}. Therefore, increased understanding of dislocation clusters, their characteristics, and their influence on cell performance is of high importance to enable material optimization.

2.3 Compensated multicrystalline silicon solar cells

Most of the studied samples in the current work are fabricated from compensated mc-Si produced by REC Solar Norway. In the production of compensated mc-Si, the energy-demanding Siemens process is replaced by less energy-consuming metallurgical processes. At REC Solar Norway, the production consists of five steps: i) Reduction of quartz to produce MG-Si in an electric arc furnace, ii) a high-temperature slag treatment, iii) low-temperature wet-chemical leaching, iv) directional solidification, and v) post treatment [97]. The result is a purification process that requires less energy compared to conventional processes, and consequently, significant reductions in energy consumption [97–99].

Compensated silicon distinguishes itself from conventional silicon by containing both acceptor atoms (typically boron) and donor atoms (typically phosphorus) in relatively large amounts [100, 101]. This implies that relatively high concentrations of dopants can be tolerated in the melt, which would otherwise be challenging to refine using metallurgical routes. Because of the different segregation coefficients of boron and phosphorus, uneven net doping and resistivity profiles can arise along the ingot, and result in a transition from

p-type to n-type towards the top of the ingot. This can be avoided by adding a second acceptor atom (typically gallium), which provides a more stable net doping and resistivity profile compared to uncompensated silicon [102, 103]. The level of compensation (C) in the material is defined by

$$C = \frac{N_{\mathrm{A}} + N_{\mathrm{D}}}{n_{\mathrm{maj}}}, \tag{2.19}$$

where N_{A} and N_{D} denote the acceptor and donor concentrations, respectively. n_{maj} is the majority carrier concentration, defined as $n_{\mathrm{maj}} = \mid N_{\mathrm{A}}^{-} - N_{\mathrm{D}}^{+} \mid$, where N_{A}^{-} and N_{D}^{+} are ionized acceptor and donor concentrations, respectively. The compensation level can vary from 1 for an uncompensated material to $+\infty$ for a fully compensated material. It should be noted that most of the material studied in the current work is lightly compensated, with a C value close to 1.

The presence of a relatively high dopant density can affect the electrical properties of the material, especially the carrier lifetime and carrier mobility [104]. The mobility can be significantly reduced for highly compensated silicon compared to uncompensated silicon [105–110], but can be modeled using the mobility model proposed by Schindler *et al.* [111]. Additionally, the relatively high doping concentrations can lead to incomplete ionization of dopants [109, 110]. This becomes relevant for doping densities starting from approximately $10^{17} - 10^{18}\,\mathrm{cm}^{-3}$ [103]. For example, non-ionized dopants have been observed to reach 25 % at boron concentrations of $N_{\mathrm{A}} \approx 2 \cdot 10^{18}\,\mathrm{cm}^{-3}$ [112]. Despite the changes in electronic properties caused by compensation, studies suggest no significant reduction in cell performance compared to uncompensated silicon when compensation levels are relatively low [23, 113, 114].

Chapter 3

Temperature coefficients

In this chapter, the temperature sensitivity of PV device performance is discussed. The fundamental mechanisms driving the thermal behavior of PV devices are introduced, and TCs are presented as a means of quantifying temperature dependent PV performance. The temperature sensitivity of the open-circuit voltage and the recombination parameter γ are assessed in detail because of their importance for the current work.

3.1 Temperature dependent performance in perspective

The power production from PV devices is significantly influenced by the operating temperature [7–11]. This is illustrated in Fig. 3.1, showing the normalized efficiency of different PV cell technologies as a function of operating temperature. The efficiency decreases approximately linearly with increasing temperature for most cell types [6, 13], except for amorphous silicon (a-Si) [17]. The rate of change in efficiency depends on various factors, which will be described in detail later in this chapter.

PV devices are characterized and optimized by the manufacturer at standard test conditions (STC), defined as a global standard solar spectrum air mass 1.5G (AM1.5G), an irradiance of $1000\,\mathrm{W\,m^{-2}}$, and a cell temperature of $25\,^{\circ}\mathrm{C}$ [115]. However, real operating conditions can differ significantly from STC depending on the climate at the location of the installed device [6, 15, 20]. This is exemplified in Fig. 3.1, showing the operating temperatures in southern Norway and a desert in Southwest US. Additionally, Fig. 3.2 further illustrates the climatic variations that can be encountered for a PV module at a fixed location. It shows monthly average values of ambient and module temperature for PV modules installed in (a) Grimstad, Norway, and (b) Málaga, Spain. The data is averaged from sunrise to sunset over the period of 2014-2018 for Fig. 3.2(a) and in 1997 for Fig. 3.2(b). Fig. 3.2 illustrates the possible differences between standard character-

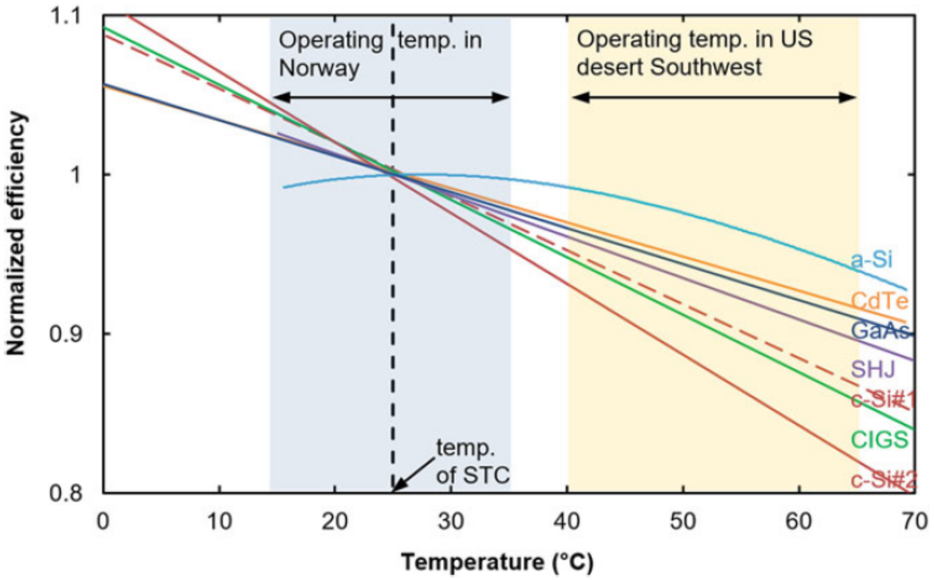

Figure 3.1: Normalized efficiency as a function of operating temperature for various PV cell technologies (a-Si: Amorphous silicon. CdTe: Cadmium telluride. GaAs: Gallium arsenide. SHJ: Silicon hetero-junction. CIGC: Copper indium gallium selenide) [6].

ization conditions (25 °C) and actual conditions encountered in the field. Fundamental understanding and quantification of temperature dependent performance are thus of high importance to enable accurate power predictions as well as device optimization for different climatic conditions.

3.2 Fundamental temperature sensitivity of photovoltaic devices

The temperature sensitivity of PV device performance is determined by the temperature dependence of the intrinsic and extrinsic energy losses in the device. These losses will be described briefly in this section.

Five fundamental energy losses can be identified in a single-junction cell [118]: i) A conversion loss originating from the conversion of thermal energy from the sun into electrical energy (usually referred to as the Carnot loss), ii) an emission loss resulting from unavoidable emitted radiation from the device, according to Kirchhoff's law of radiation, iii) an entropy generation loss, originating from the mismatch between the solid angles of the light which is absorbed and emitted by the PV device (usually referred to as the Boltzmann loss), iv) a thermalization loss due to inefficient absorption of high-energy photons, and v) a sub-band gap loss originating from the photons with energy $E < E_g$, which are not absorbed. An overview of analytical expressions for the five losses can be

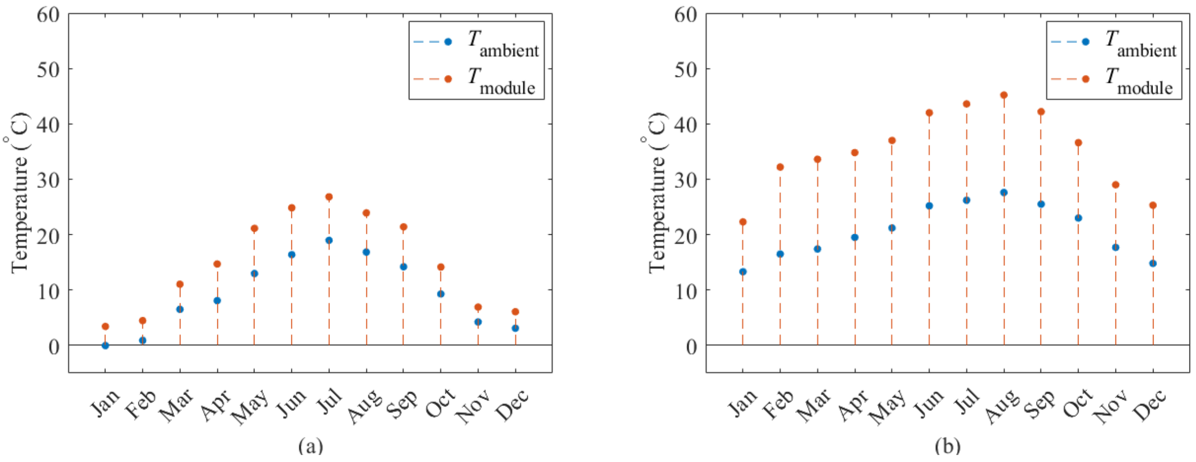

Figure 3.2: Monthly average values of ambient temperature (T_{ambient}) and module temperature (T_{module}) for PV modules installed in (a) Grimstad, Norway, and (b) Málaga, Spain. Modified from Refs. [116] and [117], respectively.

found in Refs. [119, 120]. The losses are intrinsic to a single-junction cell and, therefore, unavoidable.

The temperature sensitivity of the intrinsic losses has been investigated by Dupré *et al.* [11] and is illustrated in Figs. 3.3(a) and (b). Fig. 3.3(a) shows the fraction of incident radiation which is lost to a certain intrinsic process, as a function of cell temperature. The calculations are made assuming that the band gap energy is independent of temperature, with $E_g = 1.12\,\text{eV}$, corresponding to c-Si at $T_c = 25\,^\circ\text{C}$ and under 1 Sun illumination. Each of the intrinsic processes presented in the previous section is highlighted in the figure. Additionally, the figure includes the fraction of incident radiation which is converted into useful power. The power is observed to decrease with increasing temperature, primarily because of an increase in the solid angle mismatch loss. Fig. 3.3(b) illustrates further the temperature sensitivity of each of the loss mechanisms. It shows the change in the fraction of incident radiation for each parameter X (loss mechanism or output power), as a function of cell temperature. The majority of loss mechanisms increase linearly with increasing temperature, except for the sub-E_g and thermalization losses that remain unchanged. The result is a linearly decreasing output power with increasing temperature.

In reality, E_g is temperature dependent and has a substantial impact on the temperature sensitivity of a PV device. This is due to the fact that most of the intrinsic losses depend on E_g (as can be seen from the analytical expressions presented in Ref. [119]). The temperature sensitivity of E_g originates from two mechanisms: i) Temperature dependent electron-phonon interactions, and ii) temperature dependent lattice expansion due to increased atomic vibrations [121, 122]. For c-Si, this results in an approximately linear decrease in E_g by $-0.27\,\text{meV}\,\text{K}^{-1}$ for normal operating temperatures [123]. The

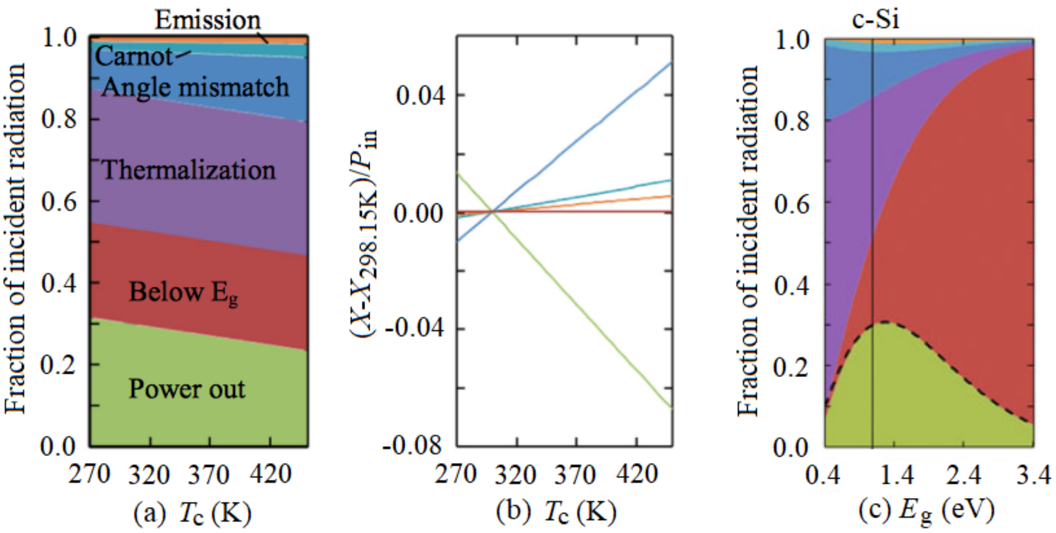

Figure 3.3: (a) Fraction of incident radiation which is lost to intrinsic processes, and the resulting output power, as a function of cell temperature for c-Si under 1 Sun illumination. (b) Change in fraction of incident radiation for each parameter X (loss mechanism or output power) as a function of cell temperature. Adapted from [11]. (c) Fraction of incident radiation which is lost to intrinsic processes, and the resulting output power, as a function of E_g. The dotted line denotes a numerical computation of the Shockley-Queisser limit, and the straight line marks the E_g of c-Si at 25 °C. Adapted from [6].

influence of E_g on the intrinsic losses is illustrated in Fig. 3.3(c), showing the fraction of incident radiation that is lost to a certain intrinsic process, as well as the output power, as a function of E_g. The dotted line shows a numerical computation of the fundamental upper limit for energy conversion (the Shockley-Queisser (SQ) limit [124]), and the straight line marks the E_g of c-Si at 25 °C. The figure illustrates how a reduction in E_g results in increased thermalization and angle mismatch losses but a decrease in the sub-E_g loss. The remaining losses are less affected by changes in E_g. For c-Si, the consequence is a reduction of the fundamental upper limit for energy conversion. The total temperature sensitivity of the fundamental losses is thus a combined effect from the PV device temperature itself, and the thermal behavior of E_g. This is illustrated in Fig. 3.4, showing the SQ limit at various temperatures from 5 °C to 85 °C. Additionally, a selection of semiconductor bang gap energies and their temperature sensitivities are included in the figure.

In addition to the five fundamental losses presented in the previous sections, Auger recombination should be included as an intrinsic loss, since the process is a consequence of fundamental material properties. The temperature dependence has been investigated by Altermatt *et al.*, who made an empirical parameterization for low injection conditions (see Eqs. (2), (3), (5), and (6) in Ref. [125]). The Auger lifetime was found to increase

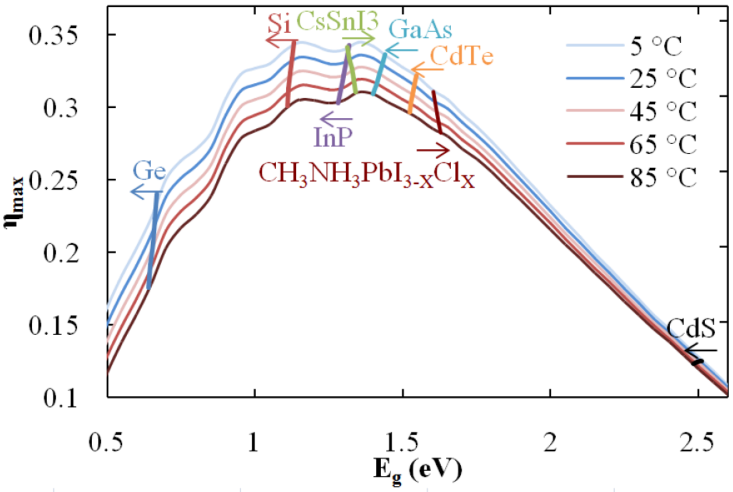

Figure 3.4: Shockley-Queisser limit at various temperatures from 5 °C to 85 °C, including the temperature sensitivity of selected semiconductor band gap energies [11].

with increasing temperature for both n and p-type silicon; however, the temperature dependence was observed to weaken at high doping concentrations.

Extrinsic losses are present in actual PV devices, influencing the total temperature sensitivity of the performance. The most important extrinsic loss mechanisms for c-Si solar cells are SRH and surface recombination, as explained in Ch. 2. Additionally, other extrinsic losses can be present, such as electrical shunts, losses originating from imperfect contact formation, reflection from the front side of the cell, and transmission losses. However, these losses are less often encountered. Because of the relevance for the current work, the discussion of extrinsic recombination processes will be limited to SRH recombination.

The temperature sensitivity of SRH recombination can be assessed by revisiting the quantification of the SRH lifetime, presented in Eq. (2.12), and the definitions given in Eqs. (2.4)-(2.7). The influence of temperature is captured by the thermal velocity of electrons and holes, $\nu_{\text{th},n}(T)$ and $\nu_{\text{th},p}(T)$, the capture cross section of electrons and holes, $\sigma_n(T)$ and $\sigma_p(T)$, and the intrinsic carrier concentration $n_i(T)$. Additionally, the SRH densities n_1 and p_1 are dependent on temperature itself and through the effective density of states in the conduction and valence bands, $N_\text{C}(T)$ and $N_\text{V}(T)$. For a specific semiconductor material, the temperature sensitivity of the SRH recombination will be determined by the defects present in the material, through $\sigma_n(T)$ and $\sigma_p(T)$. This is illustrated in Fig. 3.5, showing a simulation of τ_SRH as a function of temperature for various defects [substitutional gold (Au_s), chromium-boron (CrB), interstitial tungsten (W_i), and iron-boron (FeB)] in p-type c-Si (defect parameters from Ref. [126] have been used). The simulation is made for $N_\text{A} = 1 \cdot 10^{16}\,\text{cm}^{-3}$, $N_\text{t} = 5 \cdot 10^{12}\,\text{cm}^{-3}$, and a photon

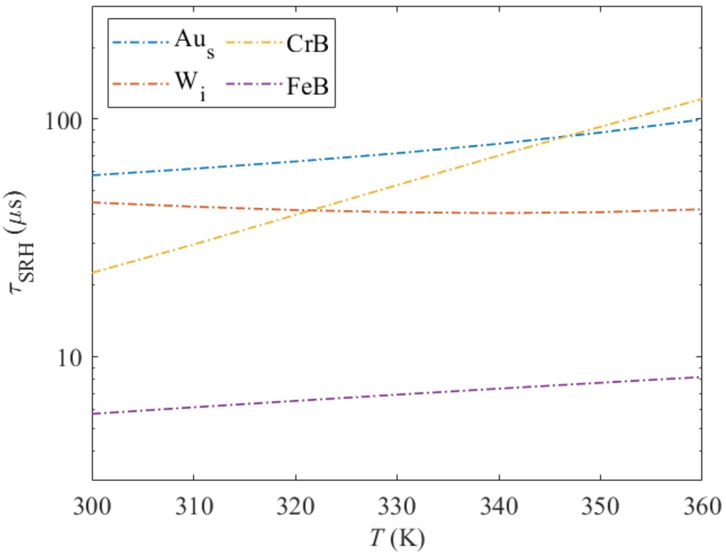

Figure 3.5: Simulated τ_{SRH} as a function of temperature for various defects in p-type c-Si ($N_{\mathrm{A}} = 1 \cdot 10^{16}\,\mathrm{cm}^{-3}$, $N_{\mathrm{t}} = 5 \cdot 10^{12}\,\mathrm{cm}^{-3}$) at $\phi = 2.25 \cdot 10^{17}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

flux of $\phi = 2.25 \cdot 10^{17}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, corresponding to 1 Sun illumination.

The relative importance of the intrinsic and extrinsic loss mechanisms depends strongly on the specific material considered. For c-Si, the intrinsic loss mechanisms account for approximately half of the total temperature sensitivity of the device [6]. Therefore, extrinsic losses play an important role in determining the temperature sensitivity. It should be noted that, as technology improves, the extrinsic losses will have less impact on temperature dependent device performance.

3.3 Quantification of temperature sensitivity

The temperature sensitivity of PV device performance can be quantified using temperature coefficients (TCs). The relative TC of a device parameter Y (β_Y) is defined as [10]

$$\beta_Y = \frac{1}{Y} \frac{\delta Y}{\delta T_{\mathrm{c}}}, \tag{3.1}$$

usually normalized by $Y(T_{\mathrm{c}=25\,^\circ\mathrm{C}})$. The relative TC is typically presented in the literature as either $\%\,\mathrm{K}^{-1}$ or $\mathrm{ppm}\,\mathrm{K}^{-1}$ (or alternatively C^{-1}) and used to enable comparison between different cell technologies. The TCs can be presented either as absolute and relative values, and are useful for illustrating different aspects of temperature sensitivity. The relative form enables comparison between cell technologies or individual cells but hides some information about the actual change in parameter pr. unit temperature. The absolute form visualizes the actual change in parameter but hides some information about material quality.

The most important device parameters [V_{oc}, short circuit current density (J_{sc}), FF, and P_{mpp}] vary approximately linearly with temperature for most solar cell materials over a moderate temperature range [14,18]. Consequently, the TC of each device parameter can be approximated as a constant, and the temperature sensitivity of P_{mpp} can be expressed as the sum of the TCs of each device parameter:

$$P_{\mathrm{mpp}}(T_{\mathrm{c}}) = V_{\mathrm{oc}}(T_{\mathrm{c}})\, J_{\mathrm{sc}}(T_{\mathrm{c}})\, FF(T_{\mathrm{c}}), \tag{3.2}$$

$$\beta_{P_{\mathrm{mpp}}} = \beta_{V_{\mathrm{oc}}} + \beta_{J_{\mathrm{sc}}} + \beta_{FF}, \tag{3.3}$$

where $\beta_{P_{\mathrm{mpp}}}$, $\beta_{V_{\mathrm{oc}}}$, $\beta_{J_{\mathrm{sc}}}$, and β_{FF} denote the temperature coefficients of P_{mpp}, V_{oc}, J_{sc}, and FF, respectively. Each device parameter and respective TC in Eqs. (3.2) and (3.3) can provide different information about the underlying physics in the device.

As described in the previous sections, the P_{mpp}, and consequently, the conversion efficiency, decreases with increasing temperature for most cell types. The total temperature sensitivity is mainly determined by $\beta_{V_{\mathrm{oc}}}$ which accounts for approximately $80 - 90\%$ for a cell which is not constrained by resistance or other FF losses [14]. Fundamentally, the V_{oc} decreases with increasing temperature due to the reduction of E_{g} [14, 22, 127]. Consequently, the intrinsic carrier density increases, leading to increased charge carrier recombination. Because of the importance of $\beta_{V_{\mathrm{oc}}}$, the parameter will be given special attention in this work, and a detailed theoretical background will be presented in the following section.

For completion, $\beta_{J_{\mathrm{sc}}}$ and β_{FF} are briefly considered. The J_{sc} increases slightly with temperature. This is due to increased band-to-band absorption facilitated by the reduction of E_{g}, as has been described analytically by Green in Ref. [14]. The temperature sensitivity of FF is mainly determined by the temperature sensitivity of V_{oc}, resulting in a reduced FF with increasing temperature as described in Refs. [13, 26]. Additionally, FF can be influenced by the temperature sensitivity of the series resistance and, in some cases, also the temperature sensitivity of the shunt resistance and the ideality factor, as suggested in Ref. [21].

3.3.1 The temperature coefficient of the open circuit voltage

The V_{oc} essentially describes the balance between the rates of photogeneration and recombination of carriers in the material. Consequently, $\beta_{V_{\mathrm{oc}}}$ reflects the temperature sensitivity of this balance.

The $\beta_{V_{\mathrm{oc}}}$ was first described analytically by Green in 1982, making use of the single diode equation as the starting point [9]:

$$J = J_{\mathrm{sc}} - J_0\left[\exp\left(\frac{qV}{kT_{\mathrm{c}}}\right) - 1\right] \tag{3.4}$$

$$\approx J_{\mathrm{sc}} - J_0\exp\left(\frac{qV}{kT_{\mathrm{c}}}\right). \tag{3.5}$$

Here J is the output current density from the solar cell and J_0 denotes the diode saturation current density approximated as

$$J_0 = A\,T_{\mathrm{c}}^{\gamma}\exp\left(-\frac{E_{\mathrm{g0}}}{kT_{\mathrm{c}}}\right), \tag{3.6}$$

where A is a factor independent of temperature, γ is a factor that includes the temperature sensitivity of several parameters influencing J_0, and E_{g0} is the band gap energy linearly extrapolated to 0 K through

$$E_{\mathrm{g}} = E_{\mathrm{g0}} + T_{\mathrm{c}}\frac{dE_{\mathrm{g}}}{dT_{\mathrm{c}}}. \tag{3.7}$$

This form of J_0 is used several places in the literature with semi-empirical parameters to determine A and γ (see Refs. [8, 128, 129] for examples). According to Ref. [9], γ usually takes values between 1 and 4.

Differentiating Eq. (3.5) and neglecting the temperature sensitivity of J_{sc}, $\beta_{V_{\mathrm{oc}}}$ can be approximated as

$$\beta_{V_{\mathrm{oc}}} = \frac{dV_{\mathrm{oc}}}{dT_{\mathrm{c}}} = -\frac{1}{T_{\mathrm{c}}}\left(\frac{E_{\mathrm{g0}}}{q} - V_{\mathrm{oc}} + \gamma\frac{kT_{\mathrm{c}}}{q}\right). \tag{3.8}$$

The material dependent variability of Eq. (3.8) is mainly determined by the V_{oc} [13, 26]. The equation predicts an approximately linear relationship between the temperature sensitivity ($\beta_{V_{\mathrm{oc}}}$) and the material quality (V_{oc}) over a moderate temperature range [13]. This indicates that a cell with a high V_{oc} will have the inherent advantage of reduced temperature sensitivity, as illustrated in Fig. 3.6 for various silicon solar cells. The V_{oc} plays an important role in determining $\beta_{V_{\mathrm{oc}}}$; however, the last term in Eq. (3.8) containing the γ parameter can have significant influence as well. For example, it accounted for up to 10 % for the cells mentioned in Ref. [11]. Fig. 3.6 displays some variation along the linear trend, which could be explained by variations in γ. One essential thing to notice from Eq. (3.8) is that a low γ value will contribute to reducing the temperature sensitivity.

In 2003, Green derived a more general formulation of $\beta_{V_{\mathrm{oc}}}$ based on internal device physics without the use of semi-empirical parameters [14]. He did this by realizing that all recombination processes driving V_{oc} can be described using the product of the carrier concentrations of electrons and holes (np), resulting in the expression

$$\beta_{V_{\mathrm{oc}}} = \frac{dV_{\mathrm{oc}}}{dT_{\mathrm{c}}} = -\frac{1}{T_{\mathrm{c}}}\left(\frac{\langle E_{\mathrm{g0}}\rangle}{q} - V_{\mathrm{oc}} + \frac{kT_{\mathrm{c}}}{q}\langle\gamma\frac{f}{\xi}\frac{d\xi}{df}\rangle\right), \tag{3.9}$$

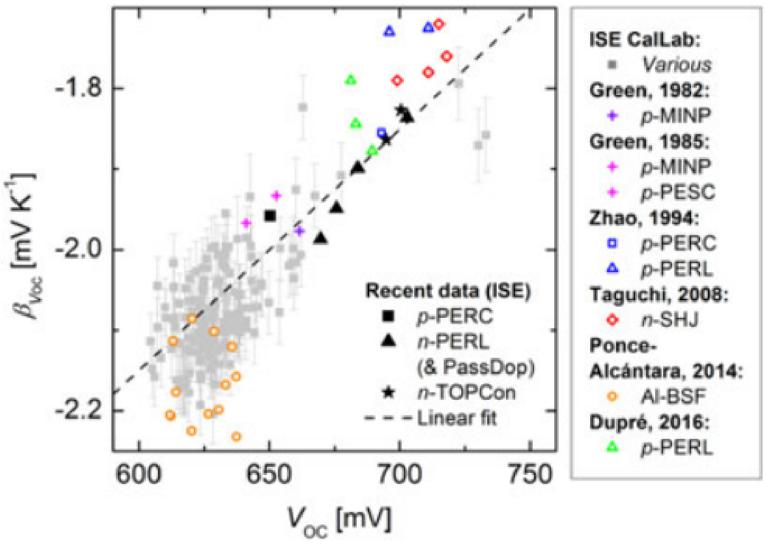

Figure 3.6: Measured values of $\beta_{V_{\mathrm{oc}}}$ as a function of V_{oc} for various silicon solar cells [22].

with

$$\xi = np \exp\left(-\frac{E_{\mathrm{g}}}{kT_{\mathrm{c}}}\right)/n_i^2, \tag{3.10}$$

where $\langle Z \rangle$ denotes the weighted value of the parameter Z and f is an appropriate function relating the np product to the specific recombination mechanism. Second order terms have been neglected in the derivation of Eq. (3.9). The format of Eq. (3.9) is similar to Eq. (3.8), but now the term $\langle \gamma \frac{f}{\xi} \frac{d\xi}{df} \rangle$ makes the link to physical processes in the material. The parameter γ is still not directly related to device physics, and knowledge about the recombination processes present in the specific solar cell of interest is necessary to accurately compute the value. This can lead to modeling errors as demonstrated in Ref. [14].

In 2015, Dupré *et al.* took a different approach to quantifying $\beta_{V_{\mathrm{oc}}}$, making use of the concept of external radiative efficiency (ERE) [11]. The ERE is defined as "the fraction of total dark saturation current in the device that results in radiative emission from the device" [130]. The output current from the solar cell can then be expressed as [11]

$$J = C_{\mathrm{F}} J_{\mathrm{sc,1sun}} - \frac{1}{ERE} J_{0,\mathrm{rad}} \left[\exp\left(\frac{qV}{kT_{\mathrm{c}}}\right) - 1 \right], \tag{3.11}$$

$$\approx C_{\mathrm{F}} J_{\mathrm{sc,1sun}} - \frac{1}{ERE} J_{0,\mathrm{rad}} \exp\left(\frac{qV}{kT_{\mathrm{c}}}\right), \tag{3.12}$$

where C_{F} is a concentration factor, $J_{\mathrm{sc,1sun}}$ denotes the J_{sc} at 1 Sun, and $J_{0,\mathrm{rad}}$ is a prefactor of the dark current density in the radiative limit. The V_{oc} can then be written as

$$V_{\mathrm{oc}} = V_{\mathrm{oc,1sun}} + \frac{kT_{\mathrm{c}}}{q} [\ln(ERE_{\mathrm{oc}}) + \ln(C_{\mathrm{F}})], \tag{3.13}$$

where ERE_{oc} is the ERE at open-circuit conditions and $V_{\mathrm{oc,1sun}}$ denotes the V_{oc} at 1 Sun. It should be noted that Eq. (3.13) neglects transport resistance and assumes a linear behavior between J_{sc} and C_{F}. Linearizing the temperature dependence of E_{g} and approximating $J_{0,\mathrm{rad}}$ as

$$J_{0,\mathrm{rad}} \approx q\frac{2\,\Omega_{\mathrm{emit}}}{c^2h^3}kT_{\mathrm{c}}E_{\mathrm{g}}^2\exp\left(-\frac{E_{\mathrm{g}}}{kT_{\mathrm{c}}}\right), \tag{3.14}$$

the temperature sensitivity of V_{oc} takes the well-known form

$$\beta_{V_{\mathrm{oc}}} = -\frac{1}{T_{\mathrm{c}}}\left(\frac{E_{\mathrm{g0}}}{q} - V_{\mathrm{oc}} + \gamma\frac{kT_{\mathrm{c}}}{q}\right), \tag{3.15}$$

with the γ parameter now explicitly quantified as

$$\gamma = 1 - \frac{d\ln ERE_{\mathrm{oc}}}{d\ln T_{\mathrm{c}}} + \left(2\frac{d\ln E_{\mathrm{g}}}{d\ln T_{\mathrm{c}}} - \frac{d\ln J_{\mathrm{sc,1sun}}}{d\ln T_{\mathrm{c}}}\right), \tag{3.16}$$

where $\frac{d\ln X}{d\ln T_{\mathrm{c}}}$ is equivalent to $\frac{dX}{dT_{\mathrm{c}}}\frac{T_{\mathrm{c}}}{X}$. In Eq. (3.14), Ω_{emit} denotes the solid angle of emission from the device, c is the speed of light in vacuum, and h is the Planck constant. Eq. (3.16) is mainly determined by the first two terms (according to Ref. [11], the term in parenthesis is less than 0.5). Since the temperature dependence of ERE depends on the recombination processes in the material, Eq. (3.16) illustrates how γ contains information about the limiting recombination mechanisms in the material. The correlation between γ and material properties will be discussed in Sec. 3.4.

3.3.2 Review of experimental observations

Now that the analytical expressions for $\beta_{V_{\mathrm{oc}}}$ have been reviewed, attention will be given to experimental observations relevant for the current work. It is well-known that lowering the bulk resistivity of mc-Si cells can lead to advantageous $\beta_{V_{\mathrm{oc}}}$ values [18, 24, 131–133]. Though rarely regarded as a design parameter, optimizing TCs for specific climatic conditions might be beneficial and lead to higher energy yield. This was mentioned by Landis in 1994, who suggested that "increasing the open-circuit voltage, even at the expense of decreases in other cell parameters (for example, by increasing base doping of the cell) may result in higher power under actual space operating conditions" [18]. This also applies for less exotic applications, as has been shown in Paper D in this thesis, where compensated mc-Si aluminum back surface field (Al-BSF) cells with low bulk resistivity (and relatively low efficiency at 25 °C) were found to outperform cells with higher resistivity (and higher efficiency at 25 °C) at temperatures above 45 °C.

Some correlation has been found between $\beta_{V_{\mathrm{oc}}}$ and cell position in the brick. Berthod *et al.* found lower temperature sensitivity for compensated mc-Si Al-BSF cells originating from the top of the bricks despite low V_{oc} values observed for these cells [35]. Additionally, Haug *et al.* observed a trend of generally decreasing temperature sensitivity towards the top of several mc-Si ingots (both compensated and uncompensated); however, the exact trend was found to be dependent on cell architecture [131].

The relationship between compensation engineering and TCs has been discussed in the literature. Ref. [134] found advantageous $\beta_{V_{\mathrm{oc}}}$ values for compensated mc-Si cells compared to uncompensated cells. In contrast, other studies found no observable effect of compensation level [35, 131]. Haug *et al.* demonstrated through modeling that the variations observed between compensated and uncompensated silicon most likely arise from variations in bulk resistivity rather than compensation [131]. However, it should be noted that compensation engineering allows for better control of the resistivity profile along the ingot height because of co-doping (see Ref. [135], for example), enabling better tuning of $\beta_{V_{\mathrm{oc}}}$.

Usually, $\beta_{V_{\mathrm{oc}}}$ and other TCs are reported as global values for the entire cell (see for instance Refs. [13, 21, 26, 35, 127, 133, 134]). As an example, $\beta_{V_{\mathrm{oc}}}$ values range from $-1.7\,\mathrm{mV\,K^{-1}}$ to $-2.3\,\mathrm{mV\,K^{-1}}$ for the c-Si cells included in Fig. 3.6. As technology improves and V_{oc} increases, less negative $\beta_{V_{\mathrm{oc}}}$ values are expected. Recently, spatially resolved temperature dependent characterization techniques have emerged and enabled spatially resolved investigations of TCs and the underlying physical mechanisms [28, 31–33, 136]. Special attention has been given to crystal defects in c-Si and their influence on the thermal characteristics of silicon wafers and cells. Eberle *et al.* reported increased temperature sensitivity of V_{oc} in contaminated regions of mc-Si cells, but reduced temperature sensitivity in areas containing dislocation clusters [28]. This was further investigated by Eberle *et al.* in a following study, reporting reduced temperature sensitivity of dislocation clusters of both mc-Si wafers and cells [29]. The authors suggested that the reduction in temperature sensitivity could be caused by the presence of impurity atoms in the dislocation clusters.

3.4 The γ parameter

The γ parameter can have significant impact on $\beta_{V_{\mathrm{oc}}}$, as explained in Sec. 3.3.1. Therefore, knowledge about the parameter is important to accurately predict PV performance under real operating conditions. Furthermore, as γ depends on the dominant recombination processes in the material, understanding the correlation between γ and material properties could potentially provide important material and device information.

The explicit quantification of γ in Eq. (3.16) allows for the calculation of the parameter for various conditions, and illustrates the functionality of γ. Dupré *et al.* estimated γ using the single-diode model for several scenarios determined by the recombination mechanisms dominating J_0 [11]. The authors computed $\gamma \approx 5$ for the scenario where J_0 is dominated by SRH recombination in the depletion region, the recombination rates are limited by both minority and majority carriers, and hence the ideality factor is approximately 2. The depletion width, the built-in voltage, and the minimum electron lifetime have been assumed independent of temperature in this calculation. Furthermore, the authors calculated $\gamma \approx 3$ for the scenario where J_0 is dominated by SRH recombination in the bulk, and at the surface, hence the recombination rate is dominated by minority carriers, resulting in an ideality factor of approximately 1. It should be noted that the carrier lifetime, mobility, electron and hole effective masses, and surface recombination velocities have been assumed independent of temperature. In Ref. [6], the authors calculate $\gamma = 1.2$ for c-Si in the radiative limit. Additionally, through an experimental study, the authors found that a strong temperature dependence of ERE can lead to negative γ values for mono-Si cells [21].

Berthod *et al.* observed a trend of decreasing γ values with increasing brick height for compensated mc-Si Al-BSF cells [35]. Similar observations were made by Haug *et al.* on both compensated and uncompensated mc-Si cells with Al-BSF and passivated emitter and rear totally diffused cell (PERCT) structures [131]. Average values were found to be between 1.6 and 3.2 depending on cell architecture and resistivity. The decreasing trend was suggested as the explanation for beneficial $\beta_{V_{\mathrm{oc}}}$ values found towards the top of the bricks.

Eberle *et al.* recently demonstrated a γ-mapping technique based on temperature dependent photoluminescence (PL) imaging [28]. The authors found significant spatial variations in γ across a mc-Si cell, and interestingly, variations between low-quality areas with different characteristics. Impurity-contaminated parts of the cell showed γ values of 3-4, and dislocation clusters exhibited relatively low, and even negative, γ values. Similar observations were made for dislocations in a further study by Eberle *et al.* [29].

Chapter 4

Experimental methods

This chapter presents the main experimental methods used throughout the PhD project. The majority of characterization techniques have the ability to obtain measurements at elevated temperatures, in order to investigate the thermal behavior of silicon wafers and cells. The chapter describes standard characterization techniques such as temperature dependent *IV* testing but also a novel temperature dependent PL imaging tool, which was developed during a research exchange at the School of Renewable Energy Engineering at the University of New South Wales (UNSW SPREE) in Sydney, Australia. Finally, general details about the studied wafers and cells are provided.

4.1 Characterization techniques for unmetalized samples

4.1.1 Temperature dependent microwave-induced photoconductive decay

Microwave-induced photoconductive decay (μ-PCD) was used to obtain spatially resolved measurements of τ_{eff} of the silicon wafers presented in Paper A. The measurements were performed using a μ-PCD system (Semilab, WT-2000PVN [137]) with an integrated heat plate (externally fabricated) enabling data acquisition at elevated temperatures.

The operating principle of μ-PCD is based on optical excitation of the sample, and signal detection from the sample using a microwave detection system [137]. The excitation is facilitated by an infrared laser, generating electron-hole pairs on a selected area of the sample. When the laser is turned off, the electron-hole pairs recombine and the concentration of carriers, and hence the conductivity, decreases. This is sensed by the detector, which consists of a ring-shaped microwave antenna that forms a resonator with the wafer and is operated near the resonance frequency. The sample conductivity influences the reflected microwave power, which is detected as a function of time. The time-dependent signal is then fitted to an exponential function, and the obtained time constant is interpreted as τ_{eff} at the given location. The process is performed on various locations across the wafer, yielding a spatially resolved τ_{eff} map. A typical resolution of a μ-PCD measurement is $500 \times 500\,\mu\text{m}^2$.

The integrated heat plate consists of a layered structure of (from top to bottom): Aluminum oxide (Al_2O_3), brass (copper and zinc alloy), a 0-300 W heating element, and aluminum. The thicknesses of the Al_2O_3 and brass layers are chosen such that the underlying metallic parts do not interfere with the τ_{eff} measurements. The heat plate enables image acquisition at temperatures ranging from room temperature to a maximum value determined by the heating element power. The temperature of the sample is monitored using a thermocouple in contact with the sample through the Al_2O_3 layer. The heat plate was kept at maximum 56 °C during our experiments to simulate actual operating temperatures and avoid permanent annealing effects on the wafers.

4.1.2 Temperature dependent photoluminescence imaging

As a part of the PhD project, a temperature dependent PL imaging tool was developed during a research exchange at UNSW SPREE. The method was published in Paper C in this thesis and used as experimental method in the Papers D-E and G-H. The measurement technique and calibration procedure will be described in detail in this section.

4.1.2.1 Background

PL imaging has been widely implemented in both industry and academia since it was developed by Trupke and Bardos in 2005 [138,139]. The technique enables spatially resolved characterization of silicon wafers and cells, providing information about important material parameters such as τ_{eff} [139], minority carrier diffusion length (L) [140,141], iV_{oc} [142], shunt and series resistance [143–145], and interstitial iron concentration [146].

Recently, PL imaging at elevated temperatures has emerged as a means to obtain additional information about material properties such as defect identification and TCs [28, 30–34, 147]. The technique can provide useful material information; however, the calibration procedure is challenging because of the temperature sensitivity of the luminescence signal from a silicon sample [36]. This is due to the temperature dependence of the radiative recombination coefficient B, the optical properties of the sample, the spectral distribution of the luminescence signal, and the temperature sensitivity of the camera. Current existing methods for calibration are: i) Optical measurement techniques [quasi-steady-state (QSS) PL], where the lifetime is calibrated either through the time dependence of the luminescence signal [33, 34, 148] or a self-consistent method (presented in Paper F in this thesis) [147], ii) a theoretical approach, where a temperature-dependent calibration parameter is found through modeling [31], and iii) calibration through QSS photoconductance (PC) based measurements obtained at various temperatures [32].

The temperature dependent PL imaging tool developed in the current work is based on a QSS-PC calibration method and will be described in detail later in this chapter. The QSS-PC based approach has the advantage of reduced complexity since it requires a relatively uncomplicated measurement setup compared to QSS-PL and is associated with few assumptions compared to the theoretical approach. It should be noted, however, that it is suitable only for unmetalized samples since metal contacts will dominate the measured PC signal and interfere with the calibration process.

The QSS-PC based calibration procedure applied to temperature dependent PL imaging was first introduced by Haug *et al.* [32], where the authors used two separate systems for image acquisition and calibration. Image acquisition was performed at various temperatures in a PL imaging tool with an integrated heat plate, and calibration was performed by moving the imaged wafer to a temperature dependent lifetime tester (Sinton Instruments, WCT-120TS [149]) and obtaining a calibration lifetime at various temperatures. The illumination condition during calibration is quasi-steady-state, where the actual image acquisition is in steady-state. Therefore, errors might be introduced in the calibration process from variation in illumination conditions. Additionally, the calibration might be affected by variations in temperature conditions and issues related to characterizing a non-uniform material, which will be elaborated later in this chapter. To address these challenges, we developed a setup where a temperature-controlled PC stage (calibration) is integrated into a PL imaging system (image acquisition), enabling direct wafer calibration under similar illumination and temperature conditions, further reducing the assumptions in the calibration process.

4.1.2.2 Setup

An illustration of the setup is shown in Fig. 4.1. A temperature-controlled PC stage is integrated into a PL imaging system. The PL imaging system consists of an 808 nm laser for excitation of the sample and a silicon charge-coupled device (CCD) camera for collection of the emitted band-to-band PL from the sample. The camera enables a resolution of approximately $100 \times 100\,\mu\text{m}^2$. To ensure collection of only the relevant photons, several filters are attached in front of the camera: Two long-pass filters of 850 nm and 950 nm are used to reduce reflections of the laser beam, and a 1050 nm short-pass filter is used to reduce reflections of the PL signal originating from the stage. The photon flux from the laser was calibrated using a silicon photodiode connected to a low-noise

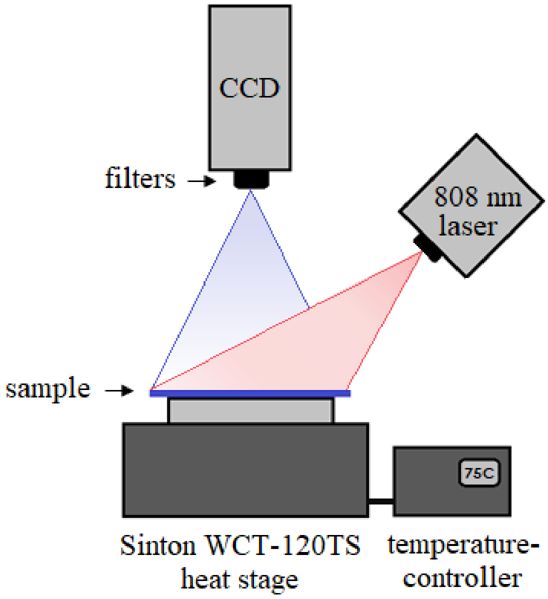

Figure 4.1: Illustration of PC-calibrated temperature dependent PL imaging setup (not to scale).

preamplifier.

The temperature-controlled PC stage (Sinton Instruments, WCT-120TS [149]) consists of a non-conductive circular hot plate (diameter of 150 mm) with a build-in eddy-current conductance sensor (diameter of 20 mm). The stage enables measurements at any desired temperature ranging from 25 °C to 200 °C. However, temperatures were kept at maximum 75 °C during our experiments to prevent the equipment from heating up and to minimize the possibility of permanent annealing effects on the wafers. The temperature was monitored using a k-type thermocouple attached at various places across a similar sample. For a sample temperature of 65 °C, a variation of ± 2 °C was found across the sample within the area of the heat plate.

The conductance sensor consists of a circular coil in which an alternating current is passed through, and a magnetic field is generated. This magnetic field induces an opposing current flow and an associated magnetic field in the sample, increasing the impedance of the coil. This results in a voltage drop across the coil proportional to the sample conductance [149, 150]. From the sample conductance, the carrier concentrations can be found, which further can be related to the excess carrier concentration and the carrier lifetime upon excitation (see Sec. 4.1.2.3 for detailed explanation). The voltage drop across the coil is recorded directly from a PC output on the heat stage using a data acquisition card connected to a computer. Average signal values are computed in the dark and during illumination.

4.1.2.3 Calibration

The calibration procedure is based on the principle that the emitted PL signal from a sample (I_{PL}) can be related to Δn through [138]

$$I_{\mathrm{PL}} = A_i \, B \, \Delta n \, (\Delta n + N_{\mathrm{dop}}), \tag{4.1}$$

where A_i is a calibration parameter that depends on the specific sample and PL measurement system, and B is the radiative recombination coefficient [36]. In cases where a compensated material is studied, $N_{\mathrm{dop}} = N_{\mathrm{eff}}$, where N_{eff} is the effective doping concentration. The parameter A_i depends on various factors such as the optical properties of the sample, the geometry of the measurement setup, and the influence of attached filters [138].

In order to relate the emitted PL signal from the sample to actual material properties, the calibration parameters A_i and B must be accurately determined. As mentioned previously, this is a non-trivial task at elevated temperatures. In our calibration technique, both parameters are determined experimentally (A_iB) from a direct measurement of the photoconductance ($\Delta\sigma$) generated in the sample during image acquisition at the same illumination and temperature conditions. The $\Delta\sigma$ is found from the following principle: When a sample is placed on the measurement stage, a voltage drop (V) is measured by the inductive coil, which can be related to the conductance (σ) of the sample through [149]

$$\sigma = A_{\mathrm{cal}}(V - B_{\mathrm{cal}})^2 + C_{\mathrm{cal}}(V - B_{\mathrm{cal}}), \tag{4.2}$$

where A_{cal}, B_{cal} and C_{cal} are calibration constants related to the specific measurement system. The constants can be found from calibrating the measurement stage using calibration wafers provided with the WCT-120TS system. The photoconductance generated in the sample during illumination can then be calculated as

$$\begin{aligned} \Delta\sigma &= \sigma_{\mathrm{ill}} - \sigma_{\mathrm{dark}} && (4.3) \\ &= A_{\mathrm{cal}}(V_{\mathrm{ill}} - C_{\mathrm{cal}})^2 + B_{\mathrm{cal}}(V_{\mathrm{ill}} - C_{\mathrm{cal}}) - [A_{\mathrm{cal}}(V_{\mathrm{dark}} - C_{\mathrm{cal}})^2 + B_{\mathrm{cal}}(V_{\mathrm{dark}} - C_{\mathrm{cal}})], && (4.4) \end{aligned}$$

where σ_{ill} and σ_{dark} denote the conductance during illumination and in the dark, and V_{ill} and V_{dark} are the measured voltages during illumination and in the dark. The measured $\Delta\sigma$ can be translated into an average Δn in the area over the inductive coil (Δn_{PC}) using [42]

$$\Delta\sigma = qW(\mu_n + \mu_p)\Delta n_{\mathrm{PC}}, \tag{4.5}$$

where W is the sample thickness, and μ_n and μ_p denote the electron and hole mobilities. Since μ_n and μ_p are functions of temperature, N_{dop} and Δn, Eq. (4.5) is solved iteratively to yield values consistent with the measured $\Delta\sigma$ of the sample [42]. The inductive coil has a non-uniform radial sensitivity, meaning that the measured $\Delta\sigma$, and therefore Δn_{PC}, are actually weighted average values determined by the coil sensitivity [151, 152].

The calibration parameters A_iB can now be found by combining Eqs. (4.1) and (4.5) with $\Delta n = \Delta n_{\mathrm{PC}}$ and computing a weighted average of PL counts in the coil area ($I_{\mathrm{PL,PC}}$) according to a suitable coil sensitivity function [151, 152]. The implementation of the sensitivity function is especially important for inhomogeneous samples such as mc-Si. Once A_iB is determined, the PL counts at every pixel (x,y) of the image ($I_{\mathrm{PL},xy}$) can be translated into a local Δn (Δn_{xy}) through

$$\Delta n_{xy} = -\frac{N_{\mathrm{dop}}}{2} + \sqrt{\left(\frac{N_{\mathrm{dop}}}{2}\right)^2 + \frac{I_{\mathrm{PL},xy}}{A_iB}}\,. \tag{4.6}$$

Knowing the value of Δn_{xy} enables image calibration into other material parameters such as τ_{eff}, iV_{oc}, the temperature coefficient of iV_{oc} ($\beta_{iV_{\mathrm{oc}}}$), and the recombination parameter γ. In steady-state, Δn_{xy} can be related to the local τ_{eff} ($\tau_{\mathrm{eff},xy}$) through

$$\tau_{\mathrm{eff},xy} = \frac{\Delta n_{xy}}{G}, \tag{4.7}$$

where G denotes the generation rate given by

$$G = \frac{\phi}{W}(1 - R_{\mathrm{f,808\,nm}}), \tag{4.8}$$

where $R_{\mathrm{f,808\,nm}}$ is the front surface reflectance of the sample measured at 808 nm. The local iV_{oc} ($iV_{\mathrm{oc},xy}$) can be calculated using [42]

$$iV_{\mathrm{oc},xy} = \frac{kT_{\mathrm{c}}}{q}\ln\left[\frac{\Delta n_{xy}(\Delta n_{xy} + N_{\mathrm{dop}})}{n_i^2}\right]. \tag{4.9}$$

Images of $\beta_{iV_{\mathrm{oc}}}$ can then be computed from two images of iV_{oc} obtained at different temperatures, by applying to each pixel the following operation:

$$\beta_{iV_{\mathrm{oc},xy}} = \frac{iV_{\mathrm{oc},xy,T2} - iV_{\mathrm{oc},xy,T1}}{T_{\mathrm{c},2} - T_{\mathrm{c},1}}, \tag{4.10}$$

where $iV_{\mathrm{oc},xy,T1}$ and $iV_{\mathrm{oc},xy,T2}$ denote the local iV_{oc} values at the sample temperatures $T_{\mathrm{c},1}$ and $T_{\mathrm{c},2}$. Note that Eq. (4.10) assumes that the $iV_{\mathrm{oc},xy}$ varies linearly with temperature in the studied temperature range. Finally, images of the recombination parameter γ can be created by computing the local γ (γ_{xy}) through [13, 28]

$$\gamma_{xy} = \frac{q}{kT_{\mathrm{c}}}\left(iV_{\mathrm{oc},xy} - \frac{E_{\mathrm{g0}}}{q} - T_{\mathrm{c}}\beta_{iV_{\mathrm{oc},xy}}\right). \tag{4.11}$$

A flat field correction is applied to the acquired images to minimize spatial non-uniformities in the camera sensitivity [153].

4.1.2.4 Discussion

The method presents a natural development of the work of Haug *et al.* [32], with sample calibration being performed directly on the wafer during PL image acquisition in one combined system. This results in a more robust calibration routine since calibration and image acquisition are performed with the same temperature and illumination conditions. Uncertainties are further reduced by ensuring the correct correlation between the coil area in the PL image and the PC measurement. This is especially important when characterizing non-uniform materials. The method enables a robust and relatively uncomplicated calibration; however, some general considerations should be made regarding the challenges of PC-based calibration and PL imaging.

Perhaps most importantly, the challenges concerning inhomogeneous samples should be addressed, since the majority of samples used in the current work are made from mc-Si. As previously mentioned, errors can be introduced in the calibration of non-uniform materials if the radial sensitivity of the inductive coil is not accounted for. By implementing a suitable sensitivity function, such errors can be minimized [151].

Additionally, lateral carrier flow can influence the lifetime calibration in experimental setups where the sample is excited by a homogeneous illumination source. A gradient in quasi-Fermi level splitting is introduced at non-uniformities, which can lead to lateral carrier flow between areas of high and low material quality and hence altered apparent lifetimes [154]. This effect becomes significant when the diffusion length is comparable to or larger than the pixel size of the camera [155]. The current flows in a combination of drift and diffusion, where a carrier de-smearing procedure can be applied to account for the diffusion part [154]. The drift current is challenging to account for and typically dominates diffused samples. A sophisticated approach to address this issue is by applying non-uniform spatial illumination to ensure a spatially homogeneous injection level across the sample. This was first demonstrated for room temperature by Zhu *et al.* [156], and has recently been developed for elevated temperatures by Nie *et al.* [157].

Moreover, it should be mentioned that the calibration parameter A_iB has been observed to be injection dependent [30], in contrast to what is generally assumed. This can affect the calibration of non-uniform materials since localized defects, such as grain boundaries and dislocation clusters, cause the injection level to vary across the sample. The authors suggested that this observation could arise from variations in the injection dependence of the PL and QSS-PC measurements, potentially caused by carrier trapping [158, 159] or non-uniformities in the coil area. Such potential errors should be minimized by monitoring trapping and accounting for non-uniformities. In the current work, trapping was monitored by performing separate measurements of temperature and injection dependent lifetime curves on a Sinton lifetime tester (Sinton Instruments, WCT-

120TS [149]). Trapping was observed on the wafers presented in the Papers E and G, where a front-detection system was added to our setup [147] to enable trapping-free calibration of the studied wafers. Non-uniformities can be accounted for by implementing a coil sensitivity function, as previously mentioned. It should be noted the injection dependence of the calibration parameter could arise from other factors than what has been mentioned above.

Other general issues additionally affect PC-based calibration. As shown by Black and Kessels, errors can be introduced in the PC measurement when characterizing wafers with different thicknesses compared to the wafers used to calibrate the conductance [160]. These errors arise from a decay of the coil magnetic field strength with the distance from the coil and can be corrected for using a function presented in Refs. [150, 160]. Since these studies are very recent, the correction has not been taken into account in the published work of the PhD project. All the studied wafers have thicknesses in the range of $180 - 220\,\mu$m, and the error is therefore assumed to be systematic.

Lastly, an important thing to address is the calibration of compensated silicon, which has been used in most of the current work. Some necessary precautions should be made in order to correctly account for the differences in material properties compared to conventional mc-Si, as mentioned in Sec. 2.3. For PC-calibrated PL imaging, this includes the use of a suitable mobility model for compensated silicon (we have used Schindler *et al.* [111]) and N_{eff} as replacement for N_{dop}.

This section has discussed advantages and challenges regarding temperature dependent PL imaging and the PC-based calibration method, as well as suggestions on how to address the various challenges. Finally, it should be stressed that PC measurements are standard procedures in both academia and industry, used to quantify carrier lifetime, and the technique provides a suitable calibration of temperature dependent PL imaging with limited assumptions compared to other existing methods. However, it is instructive to keep in mind the associated uncertainties.

4.2 Characterization techniques for metalized samples

4.2.1 Temperature dependent current-voltage testing

Temperature dependent *IV* characterization was used to obtain the TCs presented for metalized samples in Paper D. The measurements were performed using a class AAA sun simulator (NeonSee® [161]) with an integrated heat plate.

The sun simulator enables acquisition of the *IV* characteristics of a solar cell under an AM 1.5G spectrum at various illumination intensities ranging from $0 - 1200\,\mathrm{W\,m^{-2}}$ with associated errors of $\pm 15\,\mathrm{W\,m^{-2}}$. The IV characteristics are obtained by applying a series of voltages to the cell while simultaneously monitoring the current. The heat plate consists of a metal plate connected to a water-controlled heating system, enabling characterization at various cell temperatures. The temperature is monitored with an integrated sensor with associated errors of $\pm\,0.4°\,\mathrm{C}$.

The TCs can be obtained by measuring the IV characteristics at various temperatures. Since the most important cell parameters (V_{oc}, J_{sc}, FF, and P_{mpp}) vary approximately linearly with temperature for most solar cell materials [14, 18], the TCs are found from a linear fit to the cell parameters as a function of temperature. The irradiance was kept at $1000\,\mathrm{W\,m^{-2}} \pm\, 15\,\mathrm{W\,m^{-2}}$ during all TC measurements to mimic standard test conditions.

4.2.2 Temperature dependent suns-V_{oc}

The class AAA sun simulator (NeonSee® [161]) was additionally used to obtain the temperature dependent suns-V_{oc} measurements presented in Paper B. Suns-V_{oc} measurements are performed by varying the incident light intensity, while monitoring the V_{oc} of the cell. The light source is varied slowly to enable quasi-steady-state conditions. The light intensity is monitored through a calibrated reference cell, resulting in a voltage vs. illumination curve that can be converted into an implied-IV curve without the effect of series resistance [162]. Additionally, the implied-IV data can be converted into information about the injection dependence of τ_{eff} through [162]

$$\tau_{\mathrm{eff}} = n_i^2 \exp\left(\frac{V_{\mathrm{oc}}}{kT_{\mathrm{c}}/q}\right)\left(\frac{J_{\mathrm{ph}}[N_{\mathrm{dop}} + \Delta n]}{qW}\right), \tag{4.12}$$

where J_{ph} denotes the photogenerated current density. Similar to the IV measurements, the integrated heat plate enables characterization at various temperatures.

4.3 Sample details

Most of the samples studied throughout the PhD project are made from Elkem Solar Silicon® (ESS®), a compensated silicon material produced by REC Solar Norway. The feedstock production of ESS® is based on metallurgical processes, including purification steps such as slag treatment and leaching, as explained in Sec. 2.3. Typical concentrations of the main dopants are 0.20 ppmw boron and 0.60 ppmw phosphorus, depending on the targeted resistivity. Additionally, small amounts of gallium are added to the melt to enable high resistivity control along the ingot. The studied samples were all made from a blend of ESS® feedstock and a poly-Si feedstock at a desired blend-in-ratio; however, all lightly compensated. Additionally, most of the samples were fabricated from HP mc-Si ingots. Detailed material and processing information for the various samples can be found in the individual papers attached to the thesis.

As described in Sec. 2.3, compensation can lead to i) reduced carrier mobility, ii) reduced carrier lifetime, and iii) incomplete ionization. The mobility model proposed by Schindler *et al.* [111] has been used in the current work to account for changes in mobility due to compensation. Incomplete ionization is assumed to be negligible in the current work since the studied samples are lightly compensated with relatively low dopant densities (typically 1-5 $\cdot 10^{16}\,\mathrm{cm}^{-3}$). As explained in Sec. 2.3, incomplete ionization becomes relevant for doping concentrations starting from approximately $10^{17} - 10^{18}\,\mathrm{cm}^{-3}$ [103]. Regarding carrier lifetime, no significant reduction in cell performance has been found for compensated silicon compared to uncompensated silicon, when compensation levels are relatively low [23,113,114]. Since all samples in the current work are lightly compensated, this is assumed to have little effect on the material quality. The purpose of the current work is to study the influence of defects on the temperature sensitivity of mc-Si solar cells. For this purpose, lightly compensated silicon provides a suitable material if the reduced mobility is modeled correctly. Additionally, since the resistivity profile along the ingot height typically is better controlled with compensation engineering, it might ease comparison between wafers and cells from various brick positions.

Chapter 5

Summary of papers

This chapter presents a summary of each of the papers A-H. The contributions of the current author are stated for papers where the current author does not hold the main authorship.

Paper A

Minority carrier lifetime variations in multicrystalline silicon wafers with temperature and ingot position

Summary: This paper investigates the influence of temperature on spatially resolved τ_{eff} across mc-Si wafers from various brick positions. Spatially resolved measurements were performed at room temperature and elevated temperature using μ-PCD with an integrated heat plate. Low-lifetime areas across the wafers were found to improve in quality with increasing temperature while most high lifetime areas either deteriorated or remained unchanged. The relative improvement in low-lifetime areas was considerably larger than the relative change in high lifetime areas. Wafers originating from the top of the brick were observed to contain larger areas of low lifetime compared to wafers from the bottom and the middle. The relative quality enhancement of especially top wafers could explain why previous studies have found an improvement in relative TCs of mc-Si cells towards the top of the brick.

Published as:
S. T. Søndergaard, J. O. Odden, and R. Strandberg, "Minority carrier lifetime variations in multicrystalline silicon wafers with temperature and ingot position", in: *Proceedings of the 44^{th} IEEE Photovoltaic Specialists Conference*, pp. 2651-2655, 2017.
doi: 10.1109/PVSC.2017.8366683.

Paper B

Temperature dependent suns-V_{oc} of multicrystalline silicon solar cells from different ingot positions

Summary: This paper presents temperature dependent suns-V_{oc} measurements of mc-Si cells originating from various brick positions. The objective was to study the influence of brick position on the temperature sensitivity of mc-Si solar cells, without the effect of series resistance, allowing a better study of bulk material properties. Injection dependent τ_{eff} curves were acquired and found to increase with temperature for all cells; however, a considerably larger increase was found for cells from the top of brick, and a corresponding lower decrease in V_{oc}. The variation in relative $\beta_{V_{\mathrm{oc}}}$ was observed to be 5 % along the brick at 1 Sun illumination, with improved TCs towards the top of the brick.

Published as:
S. T. Søndergaard, J. O. Odden, and R. Strandberg, "Temperature dependent suns-V_{oc} of multicrystalline silicon solar cells from different ingot positions", in: *Proceedings of the 7th World Conference on Photovoltaic Energy Conversion*, pp. 2244-2247, 2018.
doi: 10.1109/PVSC.2018.8547273.

Paper C

A high-accuracy calibration method for temperature dependent photoluminescence imaging

Summary: This paper presents a novel temperature dependent PL imaging technique, enabling spatially resolved imaging of essential device parameters for silicon wafers. The PL images are calibrated using temperature dependent PC measurements, performed directly on the wafer during image acquisition. This results in a robust calibration routine with reduced uncertainties in illumination and temperature conditions compared to existing methods. The technique was applied to two compensated mc-Si wafers, one from the bottom of a brick and one from the top. Images of the recombination parameter γ were created, and the wafer from the top was found to show a larger distribution in γ with substantially lower values compared to the bottom wafer.

Published as:
S. T. Kristensen, S. Nie, M. S. Wiig, H. Haug, C. Berthod, R. Strandberg, and Z. Hameiri, "A high-accuracy calibration method for temperature dependent photoluminescence imaging", *AIP Conference Proceedings*, vol. 2147, p. 020007, 2019.
doi: 10.1063/1.5123812.

Paper D

Temperature sensitivity of multicrystalline silicon solar cells

Summary: This paper investigates the TCs of the main device parameters (V_{oc}, I_{sc}, FF, and η) of mc-Si cells, and their variations with brick height. Cells from ingots with various bulk resistivities and blend-in-ratios of ESS®, different brick heights, and with various cell architectures were studied using temperature dependent IV-curve measurements. Al-BSF cells were found to exhibit reduced (less negative) $\beta_{V_{\mathrm{oc}}}$ values towards the top of the brick, originating from a decreasing trend in average γ values with brick height. The root cause for the variation in γ was investigated using the tool presented in Paper C, by creating spatially resolved γ images of sister wafers. Significant spatial variations in γ were observed across the wafers, with dislocation clusters exhibiting low γ values compared to other crystal regions. An increasing dislocation density was observed across wafers towards the top of the brick, resulting in a decreasing average γ, and consequently, reduced $\beta_{V_{\mathrm{oc}}}$ values.

Published as:
C. Berthod, **S. T. Kristensen**, R. Strandberg, J. O. Odden, S. Nie, Z. Hameiri, and T. O. Sætre, "Temperature sensitivity of multicrystalline silicon solar cells", *IEEE Journal of Photovoltaics*, vol. 9, pp. 957-964, 2019.
doi: 10.1109/JPHOTOV.2019.2911871.

Author contribution: The current author conducted the PL imaging experiments on the wafers presented in Fig. 3, performed the data analysis, and wrote the corresponding section in the paper. Additionally, the current author produced Fig. 2, and supported the writing of the remaining parts of the manuscript.

Paper E

How gettering affects the temperature sensitivity of the implied open circuit voltage of multicrystalline silicon wafers

Summary: This paper investigates spatially resolved variations in $\beta_{iV_{\mathrm{oc}}}$ and γ across mc-Si wafers from various brick positions. The objective was to study the influence of crystal defects on the temperature sensitivity of mc-Si wafers. Intra-grain regions, grain boundaries, and dislocation clusters were investigated using temperature dependent PL imaging. The spatial variations in $\beta_{iV_{\mathrm{oc}}}$ and γ were assessed before and after subjecting the wafers to a phosphorus diffusion gettering, with the purpose of altering the impurity composition in various regions across the wafers. Large spatial variations in $\beta_{iV_{\mathrm{oc}}}$ and γ were observed both before and after gettering. The gettering process was found to alter both $\beta_{iV_{\mathrm{oc}}}$ and γ; however, areas with lowest temperature sensitivity could be correlated with dislocation clusters both before and after gettering. The temperature sensitivity of dislocation clusters and their response to gettering were found to depend on brick position, with the lowest temperature sensitivity observed for the top wafer.

Published as:
S. T. Kristensen, S. Nie, C. Berthod, R. Strandberg, J. O. Odden, and Z. Hameiri, "How gettering affects the temperature sensitivity of the implied open circuit voltage of multicrystalline silicon wafers", in: *Proceedings of the 46th IEEE Photovoltaic Specialists Conference*, pp. 0061-0067, 2019.
doi: 10.1109/PVSC40753.2019.8980880.

Paper F

Photoluminescence-based spatially resolved temperature coefficient maps of silicon wafers and solar cells

Summary: This paper presents a novel temperature dependent PL imaging technique calibrated using a PL-based self-consistent method. The technique was applied to mc-Si wafers and cells from two ingots with different dislocation densities, in order to study dislocations further. Reduced (less negative) $\beta_{iV_{\mathrm{oc}}}$ and $\beta_{V_{\mathrm{oc}}}$ values were observed towards the top of the bricks for wafers and cells from both ingots, and similar $\beta_{iV_{\mathrm{oc}}}$ and $\beta_{V_{\mathrm{oc}}}$ values were found for the two ingots. Dislocation clusters were observed to show both high and low $\beta_{iV_{\mathrm{oc}}}$ values. Two clusters with different temperature sensitivities were studied in detail using μ-PL and found to be associated with different activation energies.

Published as:
S. Nie, **S. T. Kristensen**, A. Gu, R. L. Chin, T. Trupke, and Z. Hameiri, "Photoluminescence-based spatially resolved temperature coefficient maps of silicon wafers and solar cells", *IEEE Journal of Photovoltaics*, vol. 10, no. 2, pp. 585-594, 2019.
doi: 10.1109/JPHOTOV.2019.2956261.

Author contribution: The current author organized the wafer processing (which was carried out by the Solar Industrial Research Facility [SIRF] at UNSW SPREE), contributed to the discussion of the TC results, and supported the writing of the manuscript.

Paper G

Temperature coefficients of crystal defects in multicrystalline silicon wafers

Summary: This paper presents an extension of Paper E with a more detailed investigation of the influence of crystal defects on the temperature sensitivity of mc-Si wafers. Intra-grain areas, grain boundaries, and dislocation clusters were assessed in further detail, and the physical meaning of γ was addressed. Before gettering, intra-grain areas and grain boundaries were observed to show similar temperature dependent characteristics. After gettering, the temperature sensitivity of the intra-grain areas remained unchanged, but increased for most grain boundaries, resulting from a change in material quality. Dislocation clusters exhibited both high and low $\beta_{iV_{\mathrm{oc}}}$ values compared to other crystal regions both before and after gettering. The γ parameter was discussed and related to the SRH lifetime of impurity atoms in the material. The results suggested that the gettered intra-grain areas and grain boundaries are limited by SRH centers with a modest carrier lifetime temperature sensitivity in the studied temperature range. Additionally, all dislocation clusters were found to contain recombination centers characterized by effective lifetimes with beneficial temperature sensitivity, with variations dependent on the specific cluster.

Published as:
S. T. Kristensen, S. Nie, C. Berthod, R. Strandberg, J. O. Odden, and Z. Hameiri, "Temperature coefficients of crystal defects in multicrystalline silicon wafers", *IEEE Journal of Photovoltaics*, vol. 10, no. 2, pp. 449-457, 2020.
doi: 10.1109/JPHOTOV.2020.2968111.

Paper H

Improved temperature coefficient modeling through the recombination parameter γ

Summary: This study presents a temperature and injection dependent numerical model, relating SRH defect parameters in c-Si with γ. The model was used to predict γ for various single-level defects in c-Si and identify potential root causes of low γ values. The γ parameter was found to be significantly influenced by injection level and correlate with the temperature sensitivity of the SRH lifetime. Finally, it was demonstrated that the model can be used to predict spatially resolved $\beta_{iV_{\mathrm{oc}}}$ images without the use of a temperature dependent measurement.

Submitted as:

S. T. Kristensen, A. S. Garcia, S. Nie, Z. Hameiri, and R. Strandberg, "Improved temperature coefficient modeling through the recombination parameter γ", in: *Proceedings of the 47th IEEE Photovoltaic Specialists Conference*, *in press*, 2020.

Chapter 6

Conclusion and further work

6.1 Conclusion and outlook

This thesis has expanded the knowledge about temperature dependent PV device performance by studying the influence of crystal defects on the thermal behavior of mc-Si solar cells. The temperature coefficient $\beta_{V_{\text{oc}}}$ and the recombination parameter γ were focus parameters throughout the work, providing information about the temperature sensitivity of the device performance and the underlying physical mechanisms. Additionally, a novel temperature dependent PL imaging tool was developed in order to facilitate temperature dependent and spatially resolved characterization of c-Si wafers.

Large spatial variations in temperature sensitivity ($\beta_{iV_{\text{oc}}}$ and $\beta_{V_{\text{oc}}}$) were observed across mc-Si wafers and solar cells and attributed to crystal defects in the material. Therefore, grain boundaries, dislocation clusters, and intra-grain regions were assessed in detail at various wafer and cell processing steps. Before phosphorus diffusion gettering, grain boundaries and intra-grain areas were found to be characterized by similar temperature dependencies. After the gettering process, increased temperature sensitivity was observed for most grain boundaries, resulting from a reduction in material quality. The temperature sensitivity of intra-grain regions remained unchanged.

Dislocation clusters were observed to show both reduced and increased temperature sensitivity compared to other areas across mc-Si wafers. This was found both before and after phosphorus diffusion gettering. Additionally, dislocation clusters were associated with low γ values compared to grain boundaries and intra-grain regions. The characteristics of clusters with various thermal behavior were investigated in detail, and various clusters were found to respond differently to phosphorus diffusion gettering, indicating that they might be limited by different SRH recombination centers. Two dislocation clusters with various thermal behavior were studied further and observed to be associated with different activation energies and γ, supporting this hypothesis.

The spatial variation in temperature sensitivity was found to be more pronounced across wafers compared to a sister cell, which was suggested to result from incomplete processing of the wafers and lateral conduction across the cell. Especially grain boundaries were difficult to identify after cell processing. Most importantly, the areas with reduced temperature sensitivity were correlated with dislocation clusters at all fabrication steps.

Brick position was found to significantly affect the average $\beta_{iV_{\mathrm{oc}}}$ and $\beta_{V_{\mathrm{oc}}}$ of mc-Si wafers and cells, similar to what has previously been observed. Wafers and cells originating from the top of their respective bricks generally exhibited reduced average temperature sensitivity (less negative $\beta_{iV_{\mathrm{oc}}}$ and $\beta_{V_{\mathrm{oc}}}$ values) compared to other brick positions. This was observed for both compensated and uncompensated mc-Si wafers and cells. The reduced temperature sensitivity was found to arise mainly from the presence of dislocation clusters, because of associated low γ values, and a typically increasing density towards the top of a mc-Si brick.

To investigate the physical meaning of γ, a temperature and injection dependent numerical model was developed, relating γ to the SRH defect parameters [E_{t}, N_{t}, $\sigma_n(T)$, and $\sigma_p(T)$] of single-level defects in c-Si. The model was used to predict γ for various impurities in c-Si and identify potential root causes of low γ values. Additionally, it was shown that γ can be significantly influenced by the injection level. Finally, it was demonstrated that the model can be used to predict spatially resolved $\beta_{iV_{\mathrm{oc}}}$ images without a temperature dependent measurement.

Increased knowledge about the thermal behavior of photovoltaic devices is essential to accurately forecast the power production of photovoltaic installations and to enable device optimization at different climatic conditions. This is of special importance for c-Si wafers and cells because of the industrial relevance of the technology. This work has mapped the influence of various crystal defects on the thermal behavior of mc-Si wafers and solar cells. Additionally, the work has established a relationship between γ and crystal defects in SRH limited c-Si devices, enabling more accurate TC predictions and thus, final cell performance under realistic operating conditions.

6.2 Further work

In this thesis, dislocation clusters were observed to exhibit a complex thermal behavior, and various clusters were found to be characterized by different activation energies and γ. However, the mechanisms causing low and high temperature sensitivity are still not fully uncovered. Further work could explore the recombination centers present in dislocation clusters with various thermal behavior, where the developed numerical γ model could be useful for defect identification.

The temperature sensitivity of grain boundaries and dislocation clusters has been in focus during the current work; however, the structural characteristics of the various defects have not been studied. Another interesting subject for further work would be a detailed investigation combining crystallography and temperature dependent analysis, to study the individual TCs of various grain boundary groups and dislocations. The influence of the coincidence index Σ for grain boundaries, and the dislocation size and height in the brick, could be investigated to uncover the influence of the crystallographic microstructure of various defects, and hence their influence on temperature dependent device performance.

The current work has studied the TCs of wafers at various processing steps (before and after phosphorus diffusion gettering) as well as finished samples. However, the influence of firing could be investigated further. In Paper F, the spatial variations in temperature sensitivity were found to be more pronounced across mc-Si wafers compared to a sister cell, which could arise from the firing process. However, further investigations are needed to confirm this hypothesis.

Finally, the temperature dependent non-uniform excitation method presented by Nie *et al.* [157] may be implemented to increase the accuracy of temperature dependent characterization for future studies.

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Appendices

The appended papers have been published or submitted for publication in peer-reviewed international conference proceedings and journals. The versions included in this thesis only differ in formatting. Therefore, abbreviations and symbols are individually defined in each article.

Paper A

Minority carrier lifetime variations in multicrystalline silicon wafers with temperature and ingot position

Published as:

S. T. Søndergaard, J. O. Odden, and R. Strandberg, "Minority carrier lifetime variations in multicrystalline silicon wafers with temperature and ingot position", in: *Proceedings of the 44^{th} IEEE Photovoltaic Specialists Conference*, pp. 2651-2655, 2017.
doi: 10.1109/PVSC.2017.8366683

Minority carrier lifetime variations in multicrystalline silicon wafers with temperature and ingot position

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Abstract **— The minority carrier lifetimes of multicrystalline silicon wafers are mapped using microwave photoconductive decay for different temperatures and ingot positions. Wafers from the top of the ingot display larger areas with lower lifetimes compared to wafers from the bottom. The lifetimes of low-lifetime areas are found to increase with the temperature, while the lifetimes of some high-lifetime areas decrease or remain unchanged. The relative improvement of the low-lifetime areas is considerably larger than the relative change in the high-lifetime areas. We suggest that the above-mentioned observations explain, at least partially, why previous studies have found the relative temperature coefficients of mc-Si cells to improve towards the top of the ingot.**

A.I. Introduction

The performance of a silicon solar cell depends on the minority carrier lifetime, which is affected by several parameters such as temperature, injection level and the type and concentration of impurities in the cell [1–4]. The temperature dependence of the lifetime should be of special interest for industrial purposes since field operation temperatures can be relatively high, negatively affecting the power output from the cell [5].

Multicrystalline (mc-Si) wafers made from a polycrystalline feedstock (poly-Si) are widely used for industrial production of silicon solar cells due to the cost-effectiveness of the fabrication process. However, a relatively large and uneven distribution of impurities and crystal defects can be found throughout the ingot because of the quality of the feedstock and the solidification process [6, 7]. Several papers have shown that the minority carrier lifetime of mc-Si wafers varies with the wafer position in the ingot and this effect is considered to be impurity related [3, 8]. In recent work, it has been shown that the temperature coefficients of solar cells made from mc-Si vary along the height of an ingot [9]. A natural question to be raised is thus whether temperature variations affect the minority carrier lifetime differently throughout the ingot. Investigating this might provide information about how to optimize cells originating from different positions in an ingot as well as improve our understanding of how silicon cells perform in the field.

The present work is a study of the variations in minority carrier lifetime of mc-Si wafers, combining the effect of temperature and ingot position using microwave photoconductive decay (μ-PCD). The lifetimes are mapped at room temperature and at an elevated temperature of 56 °C, which is close to temperatures often encountered in the field.

A.II. Experimental Details

The studied samples were mc-Si wafers made from directional solidification of a poly-Si feedstock, produced industrially and passivated with a layer of 43 nm a-Si:H in a research laboratory. The lifetimes were measured using μ-PCD in a Semilab WT-2000PVN. To heat the wafers, a heat plate with a top section consisting of a thick slab of sintered aluminum oxide (alsint) was used. This material is an electrical insulator and the thickness of the slab ensures that underlying metallic parts do not interfere with the lifetime measurements. To secure exactly similar conditions, the wafers were placed on the heat plate also when mapping lifetimes at room temperature.

To control the repeatability of the lifetime measurements, one particular wafer was mapped at several occasions throughout the period through which the series of measurements was conducted. The results of these repeated control measurements are shown in Fig. A.1 where the shortest measured lifetime is presented as a function of measurement number. The error bars show the standard deviation of the 23 °C and the 56 °C measurements, respectively. The measured lifetimes change slightly during the period considered, however within the statistical fluctuations.

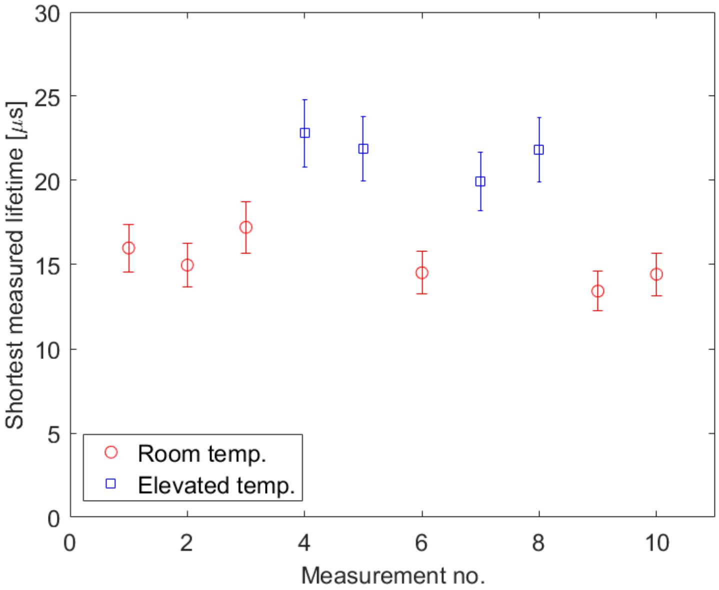

Figure A.1: Repeated control measurements of the shortest measured lifetime on a wafer. The error bars show the standard deviation of the 23 °C and the 56 °C measurements, respectively.

A.III. Results

The average lifetime of each wafer is shown in Fig. A.2 as a function of the position of the wafer in the ingot. Position 1 indicates the wafer closest to the bottom whereas 600 is close to the top. The average lifetime is found to increase by 3.4 % on average when the temperature is increased from 23 °C to 56 °C. However, conducting a Student's t-test, the difference in lifetimes with temperature is not found to be statistically significant. Furthermore, we observe a tendency that the average lifetime decreases throughout the ingot, which matches results in the literature [3, 8, 10].

The 0.1 % pixels with the longest measured lifetime on each wafer is shown in Fig. A.3 as a function of the wafer position. The longest lifetime decreases by 6.5 % on average when the temperature is increased, however this decrease is also not found to be statistically significant. Furthermore, we observe the tendency that the longest measured lifetime is lowest towards the top of the ingot.

The 0.1 % pixels with the shortest measured lifetime on each wafer is shown in Fig. A.4 as a function of the wafer position. The shortest lifetime is found to increase by 47.3 % on average when the temperature is increased. Furthermore, we observe a tendency that the shortest measured lifetime takes the shortest value at the top of the ingot.

A consistent increase in lifetime with temperature was found for areas on the wafers with lifetimes below 50 μs. The fraction of pixels on each wafer with lifetimes below 50 μs is shown in Fig. A.5 as a function of the wafer position. The fraction decreases by 55.3 %

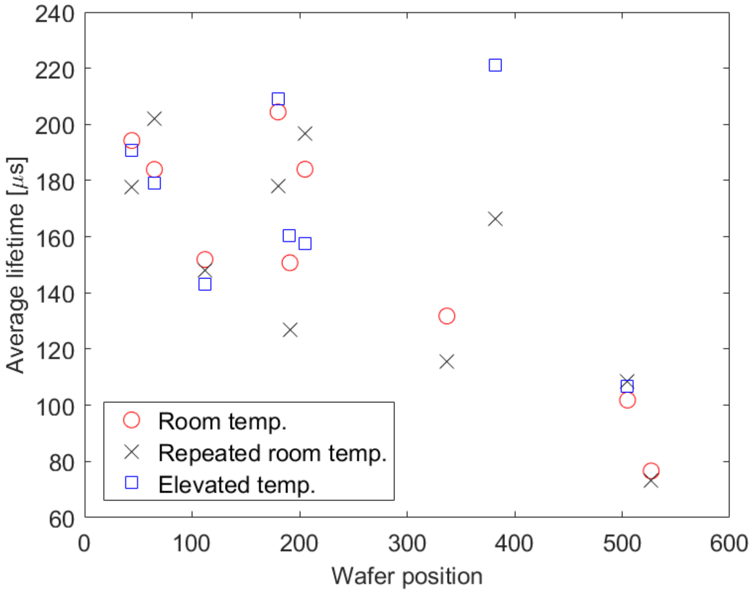

Figure A.2: Average lifetime of each wafer as a function of wafer position.

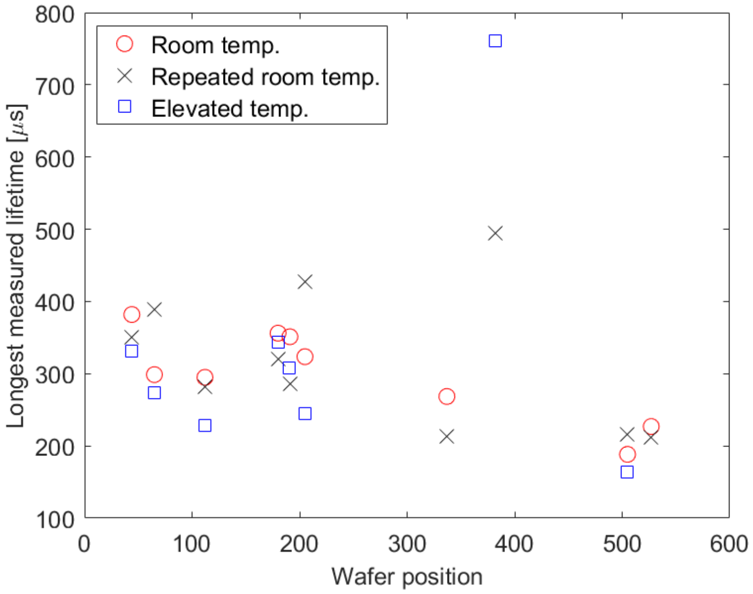

Figure A.3: 0.1 % pixels with longest measured lifetime as a function of wafer position.

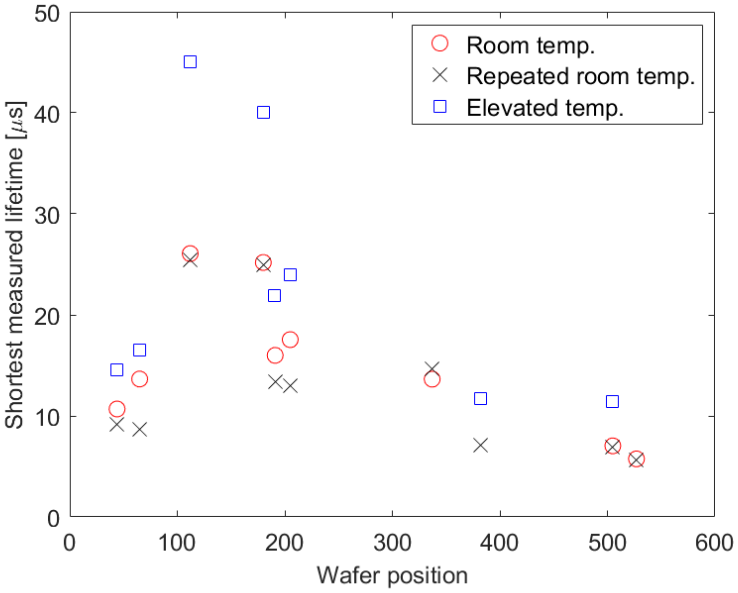

Figure A.4: 0.1 % pixels with shortest measured lifetime as a function of wafer position.

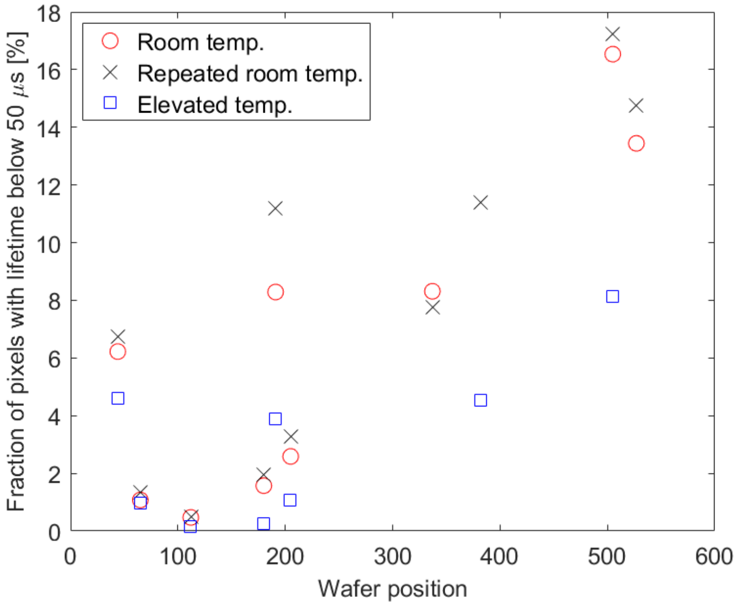

Figure A.5: Fraction of pixels with lifetime below 50 μs as a function of wafer position.

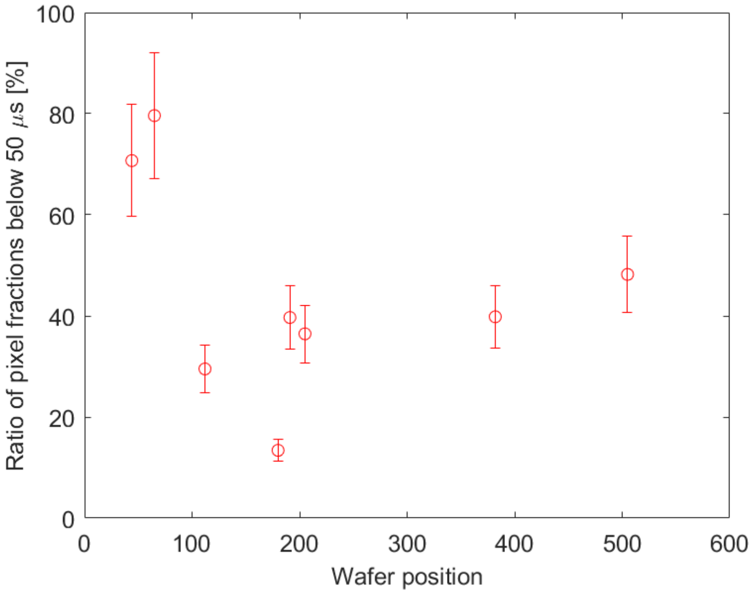

Figure A.6: Ratio of fractions of pixels with lifetime below 50 μs at 56 °C to 23 °C as a function of wafer position. The error bars are estimated from the standard deviation of repeated control measurements.

on average when the temperature is increased. In addition, Fig. A.5 shows the tendency that the wafers at the top of the ingot consist of a larger number of pixels with lifetimes below 50 μs. This matches the tendency found in Fig. A.4 where the shortest measured lifetime was shortest at the top of the ingot.

To visualize the effect of the temperature change, some additional data of the $< 50\,\mu$s areas are plotted in Fig. A.6. It shows the ratio of the fraction of pixels with lifetimes below 50 μs at 56 °C to the same fraction at 23 °C. Hence a low ratio corresponds to a drastic decrease in the number of low lifetime pixels when the temperature is increased. The error bars are estimated from the standard deviation of repeated control measurements of the lifetimes below $< 50\,\mu$s. This was calculated for one particular wafer and generalized to the remaining wafers.

We observe that the number of low-lifetime pixels decreases for all wafers when the temperature is increased. In addition, we see a tendency that the wafers from the middle and the top of the ingot seem to benefit considerably from the temperature increase, whereas the effect is relatively small for wafers from the bottom. Because of the low number of measurements this should only be interpreted as a possible trend. From Fig. A.6, we would expect a constant ratio throughout the ingot. However, the change in composition and distribution of impurities throughout the ingot might cause the wafers to respond differently to temperature changes, as will be discussed later.

A further investigation of the temperature effect can be seen in Fig. A.7, which shows

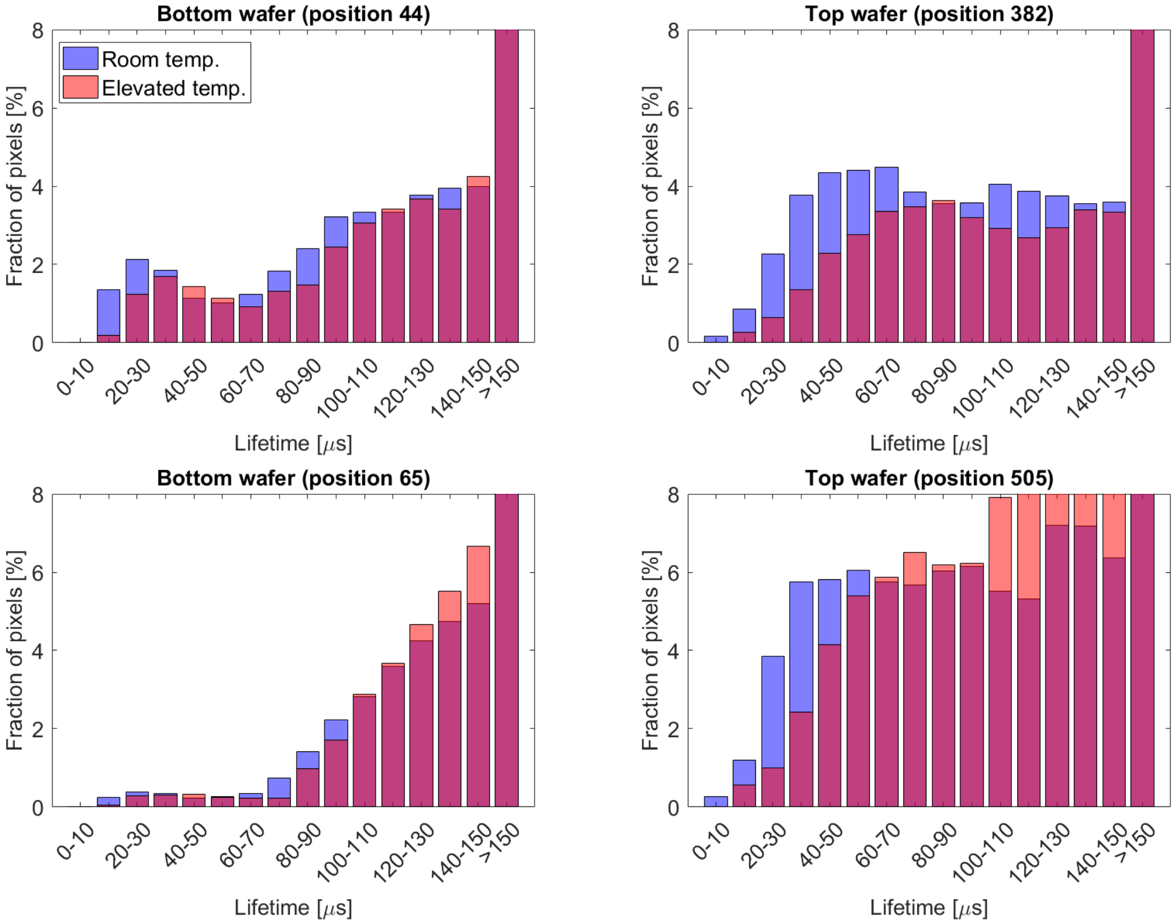

Figure A.7: Fraction of pixels of different low-lifetime intervals for bottom and top wafers.

the fraction of pixels in different lifetime intervals for two bottom and two top wafers at the relevant temperatures. The top wafers are found to consist of a larger fraction of pixels with lifetimes below 50 μs compared to bottom wafers, consistent with the trend observed in Fig. A.5. This fraction decreases with temperature for all lifetime intervals below 50 μs for top wafers, while this is not always the case for bottom wafers. Furthermore, the decrease seems to be larger for top wafers. The number of pixels with lifetimes above 150 μs responds differently to the temperature increase for the different wafers as shown in Fig. A.8. Some of the wafers experience a shift of the pixels towards lower lifetimes, whereas one of the top wafers display the opposite trend (note that the lifetime intervals for ”top wafer (position 382)” differ from the other wafers). This shows that an increase in temperature in general is beneficial for areas with low lifetime but not necessarily for areas with a high lifetime.

A PC1D simulation is shown in Fig. A.9 relating the cell efficiency to the carrier lifetime at the two relevant temperatures. The simulation is based on standard cell parameters. For cells with lifetimes above 50 μs, a temperature increase results in a relatively large

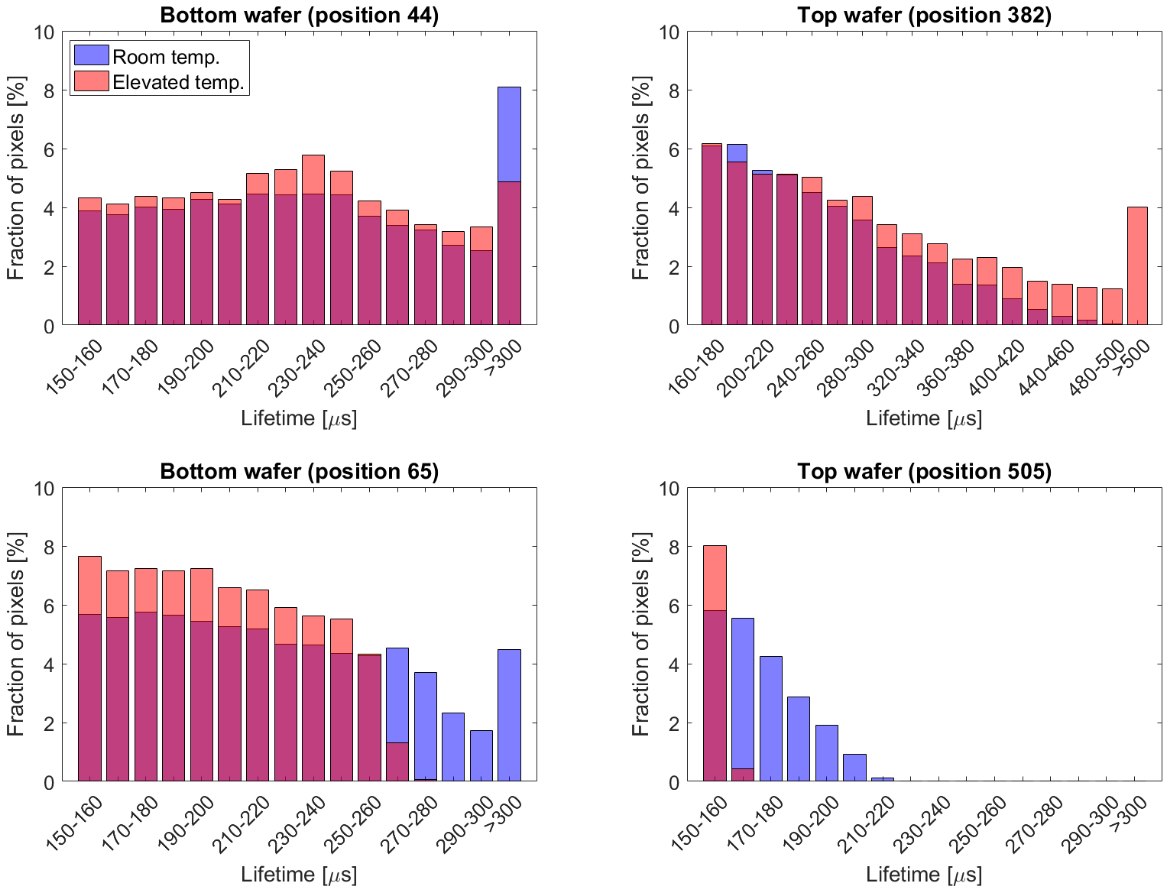

Figure A.8: Fraction of pixels of different high-lifetime intervals for bottom and top wafers. Note that the intervals for top wafer (position 382) differ from the other wafers.

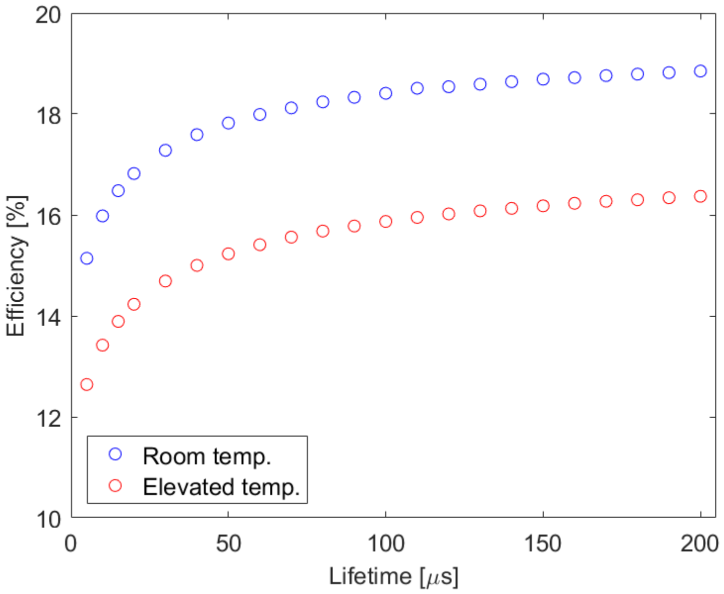

Figure A.9: PC1D simulation of cell efficiency as a function of lifetime.

efficiency reduction regardless of how the lifetime changes. For cells with lifetimes below 50 μs, an increase in temperature results in a significantly smaller efficiency reduction if the lifetime increases with the temperature, as is the case for the low-lifetime areas in this study. Since wafers from the top of the ingot in general show larger areas with low lifetimes, the relative performance of such cells is expected to decrease less with temperature compared to cells originating from the bottom of the ingot. Consequently, we expect the top cells to show better temperature coefficients, which agrees with the results in Ref. [9].

During the directional solidification of mc-Si, the majority of impurities will segregate towards the top of the ingot leaving a higher concentration of impurities in this area [8]. In addition, back diffusion from the crucible into the ingot can result in a higher concentration of impurities with large diffusion coefficients right at the bottom of the ingot [6]. An uneven distribution and composition of impurities might cause the wafers to respond differently to temperature changes and the wafers from the top of the ingot to display better temperature coefficients. This seems plausible since the capture cross sections of different impurities depend differently on temperature and might decrease, as observed for iron, copper, molybdenum and titanium [4, 11-13].

A.IV. Conclusion

The minority carrier lifetimes of mc-Si wafers have been studied for different temperatures and ingot positions. We found that wafers from the top of the ingot contained larger areas with lifetimes below 50 μs compared to wafers from the bottom. Areas with lifetimes below 50 μs in general experienced an increased lifetime when the temperature was increased. In high-lifetime areas, the lifetime decreased with temperature for some of the wafers, whereas others increased or remained constant.

These findings are believed to be impurity related, since the composition and distribution of impurities change throughout the ingot and in general is found to be larger at the top. Since the capture cross sections of some impurities decrease with temperature, this could explain why temperature coefficients previously have been found to be better for cells originating from the top of an ingot.

Acknowledgment

We would like to thank Gaute Stokkan at SINTEF, for generously sharing the heat plate with us, and Elin Stubhaug and Ragnar Ekker, who designed and made the heat plate as a part of their Masters project at NTNU.

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Paper B

Temperature dependent suns-V_{oc} of multicrystalline silicon solar cells from different ingot positions

Published as:
S. T. Søndergaard, J. O. Odden, and R. Strandberg, "Temperature dependent suns-V_{oc} of multicrystalline silicon solar cells from different ingot positions", in: *Proceedings of the 7th World Conference on Photovoltaic Energy Conversion*, pp. 2244-2247, 2018.
doi: 10.1109/PVSC.2018.8547273

Temperature dependent suns-V_{oc} of multicrystalline silicon solar cells from different ingot positions

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Abstract **— This paper presents temperature dependent Suns-V_{oc} measurements on multicrystalline silicon cells originating from different ingot positions. The effective lifetime is found to increase for all cells when the temperature is increased from 25 °C to 65 °C. However, cells from the top of the ingot show a considerably larger increase of $40 - 48\,\%$ for illumination conditions of 0.1-1 Sun, compared to an increase of $20 - 30\,\%$ observed for cells from the bottom. The decrease in V_{oc} with increasing temperature is found to be lower for cells from the top of the ingot compared to cells from the bottom. The temperature coefficient of the V_{oc} is found to vary 5 % along the ingot at 1 Sun, highlighting the influence of ingot position for applications at elevated temperatures.**

B.I. Introduction

Solar cells are usually characterized and compared at standard test conditions (STC) which correspond to an irradiance of 1000 W/m^2, an air mass 1.5 spectrum and a cell temperature of 25 °C. However, under real operating conditions, temperatures rarely resemble the STC and are typically higher [1,2]. An increase in cell temperature negatively affects the power output from most cell types [1,3,4]. It is therefore of high importance to understand and quantify this temperature sensitivity to make proper field predictions and to enable device optimization.

Multicrystalline silicon (mc-Si) wafers made from a polycrystalline silicon (poly-Si) feedstock are often used for industrial production of silicon solar cells because of the cost-effectiveness of the fabrication process. However, mc-Si ingots contain a relatively large amount of crystal defects compared to monocrystalline silicon (mono-Si), resulting in a lower cell efficiency [5]. In addition, these crystal defects are unevenly distributed throughout the ingot causing the efficiency and other cell parameters to vary with cell position, and typically to reduce towards the top [6–9].

Recently, it has been found that the relative temperature coefficients (TC) of mc-Si cells vary along the ingot height and that cells originating from the top show better relative TCs compared to the cells from the bottom [9]. Ref. [10] studied the spatial distribution of mc-Si wafers from different ingot positions and found that wafers from the top of the ingot consisted of a larger number of cell-limiting lifetimes compared to cells from the bottom. These cell-limiting lifetimes were found to improve with increasing temperature, whereas no trend was found for the higher lifetime-areas.

Understanding the physical processes responsible for the reduced temperature sensitivity observed for cells and wafers originating from the top of an ingot is an important step in the process of quantifying the thermal behavior of mc-Si cells. In this work, temperature-dependent Suns-V_{oc} measurements are performed on compensated mc-Si cells originating from different ingot positions. Suns-V_{oc} measurements enables the generation of pseudo light IV curves without the effect of series resistance and therefore allows a better study of the bulk material properties of the cells [11]. The measurements were performed at room temperature and at 65 °C, the latter corresponding to realistic field operating conditions.

B.II. Experimental Details

Seven compensated p-type mc-Si cells were studied, originating from an ingot produced by directional solidification of a mix of 55 % poly-Si and 45 % compensated Elkem Solar Silicon® (ESS®) with a targeted resistivity of 1.25 Ω·cm. ESS® is a tri-doped compensated material where gallium is added to the boron and phosphorous dopants to avoid a pn-changeover throughout the ingot and for better resistivity control along the ingot height [13]. A central brick was cut into wafers which were labelled with the numbers 1-37, representing positions from the bottom to the top of the brick. Seven wafers were then chosen from different ingot positions from the bottom to the top. The 180 μm thick 6” wafers were passivated with a-Si:H at a research laboratory and processed into Al-BSF cells at ISC Konstanz. The cells were then light-soaked for 48 h to ensure full light-induced degradation.

The Suns-V_{oc} measurements were performed under standard AM 1.5G conditions using

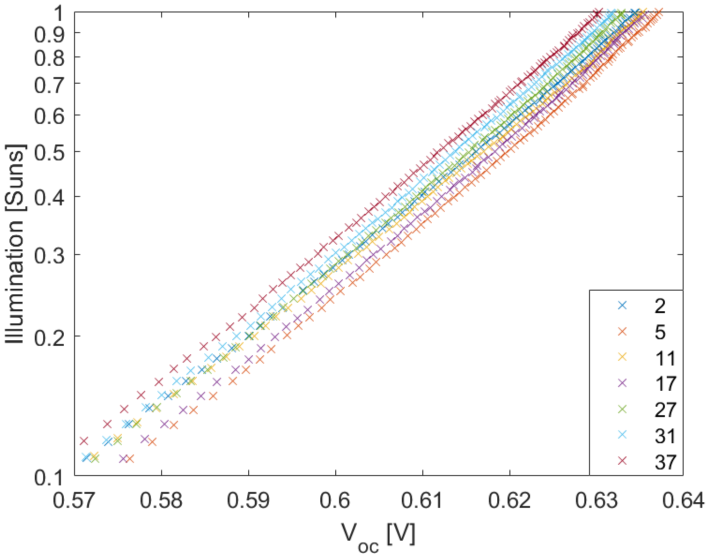

Figure B.1: Open-circuit voltage at different light intensities obtained at 25 °C for cells originating from different ingot positions.

a NeonSee$^{\mathrm{TM}}$ AAA sun simulator at the temperatures 25 °C ± 0.3 °C and 65 °C ± 0.4 ° C. Since the cell parameters of mc-Si cells vary approximately linearly with temperature for normal operating temperatures [12], two temperatures are assumed to give a proper representation of the temperature dependence. To ensure repeatability, the same cell was studied several times during the total period of data acquisition.

B.III. Results and Discussion

A. Influence of Ingot Position on V_{oc} and τ_{eff}

Fig. B.1 shows Suns-V_{oc} curves obtained at 25 °C for cells from different ingot positions. For all light intensities, V_{oc} is found to be lowest for the three top cells and highest for cells originating from the middle and near the bottom of the ingot, similar to the findings presented in Ref. [9]. This is illustrated further in Fig. B.2 which shows the V_{oc} as a function of cell number for the light intensities 0.1, 0.5 and 1 Sun. An illumination intensity of 0.1 Sun corresponds to an injection level close to the maximum power point of the cells considered. No substantial difference is observed for the change in V_{oc} with ingot height for the different illumination conditions.

Fig. B.3 shows the effective lifetime as a function of injection level obtained at 25 °C. The lifetime is found to be lowest for the three top cells for an injection level of $2\cdot10^{13}\,\mathrm{cm}^{-3}$ and higher. This is illustrated further in Fig. B.2 showing the effective lifetime as a function of cell number for the light intensities 0.1, 0.5 and 1 Sun. The lifetime at 0.1 Sun seems to be most sensitive to ingot position.

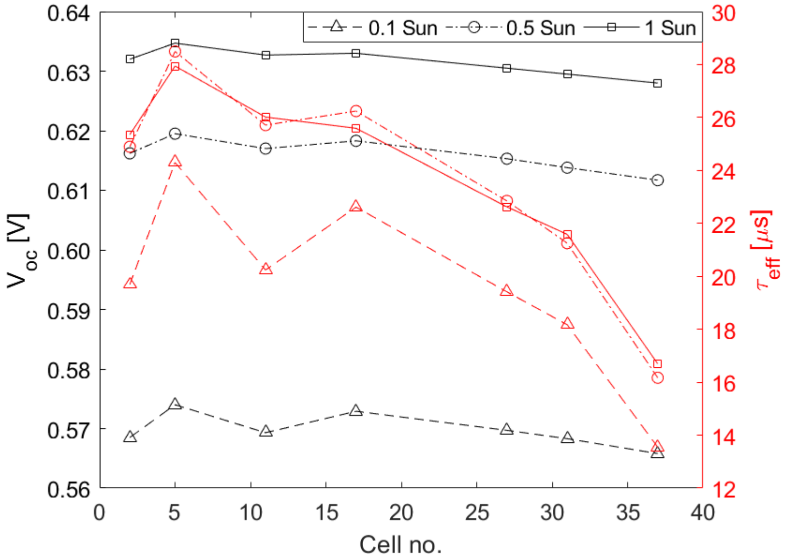

Figure B.2: Open-circuit voltage and effective lifetime as a function of cell number at 25 °C for the light intensities 0.1, 0.5 and 1 Sun.

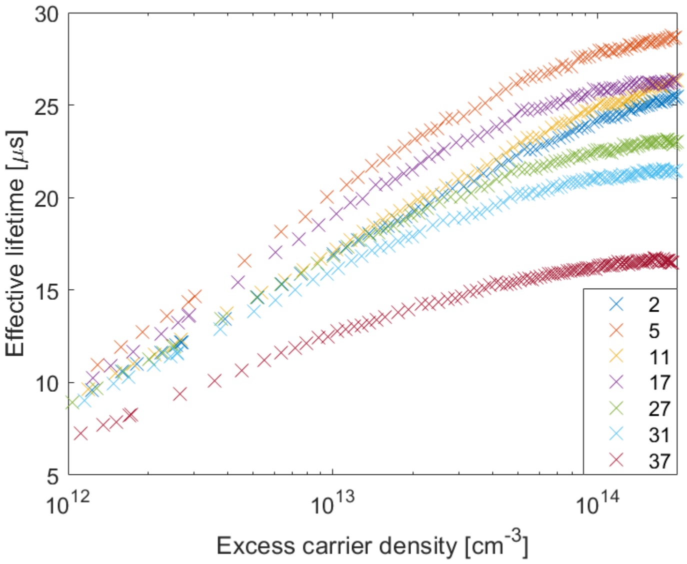

Figure B.3: Effective lifetime as a function of injection level at 25 °C.

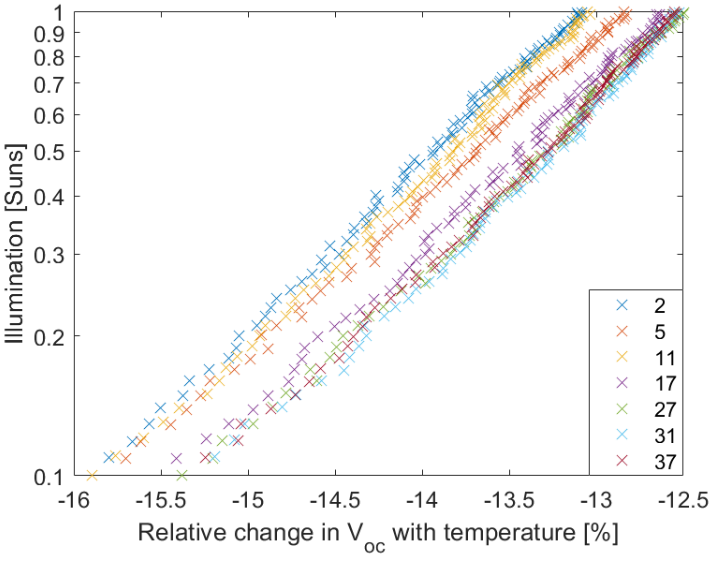

Figure B.4: Relative change in open-circuit voltage for different light intensities when the cell temperature is changed from 25 °C to 65 °C.

B. Temperature Sensitivity of V_{oc} and τ_{eff} with Ingot Position

Fig. B.4 shows the relative change in V_{oc} when the temperature is increased from 25 °C to 65 °C for the intensities 0.1-1 Sun. The data is presented such that a small negative change in V_{oc} corresponds to a cell with a low temperature sensitivity. In Fig. B.4 we see a tendency that the three top cells are less sensitive to a temperature increase, whereas the three cells from the bottom are most sensitive. This is illustrated further in Fig. B.5 which shows the relative change in V_{oc} with temperature as a function of ingot position for the light intensities 0.1, 0.5 and 1 Sun. For all intensities considered, we see a trend that the temperature sensitivity is reduced towards the top of the ingot.

From Fig. B.5, the TCs of the V_{oc} can be calculated for different ingot heights. The relative TCs at 1 Sun are found to vary from $-0.330\,\%$ to $-0.317\,\%$ throughout the ingot, corresponding to a relative change of 5 %. This trend is similar to the findings of Ref. [9] where the TCs of the V_{oc} of compensated mc-Si cells were found to vary with ingot height, from $-0.325\,\%$ for cells from the bottom to $-0.313\,\%$ for cells from the top, corresponding to a relative change of 4 %. The relative change is found to be 4 % at 0.1 Sun and 5 % at 0.5 Sun. Therefore, the relative variation along the ingot does not seem to change with illumination conditions. This variation in TCs of the V_{oc} throughout the ingot illustrates a potentially non-negligible influence of ingot position for applications at elevated temperatures.

Fig. B.5 shows the relative increase in lifetime with temperature as a function of ingot position for injection levels corresponding to the light intensities 0.1, 0.5 and 1 Sun. The

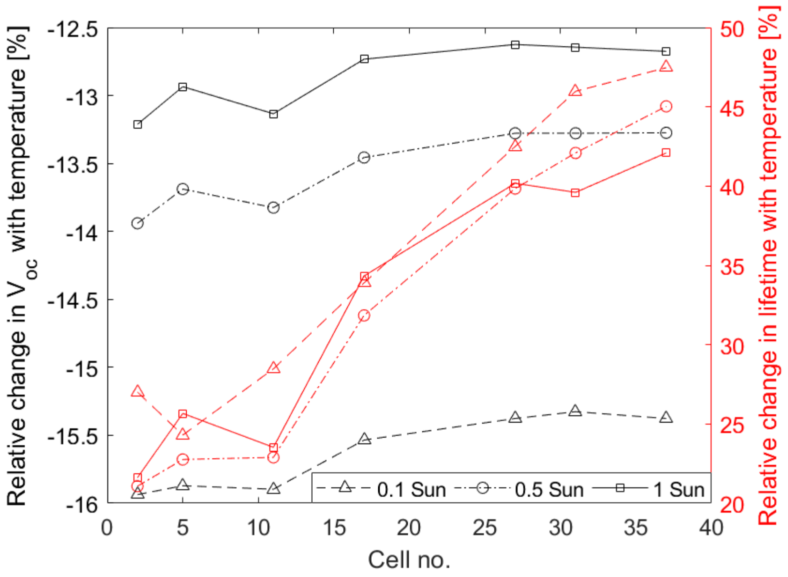

Figure B.5: Relative change in open-circuit voltage and lifetime when the cell temperature is changed from 25 °C to 65 °C for the light intensities 0.1, 0.5, and 1 Sun.

three top cells experience the largest increase in lifetime of $40-48\,\%$ for the injection levels considered. In contrast, the bottom three cells experience the lowest increase between $20-30\,\%$. The relative variation in lifetime seem to be similar for the three injection levels considered.

A Suns-V_{oc} measurement is a global measurement and therefore it does not give information about the temperature sensitivity of the lifetime in different areas of the cell. However, in Ref. [10], mc-Si wafers from the top of an ingot were found to consist of larger areas of cell-limiting lifetimes that improved with increasing temperature. The lifetime of high-quality areas remained unchanged when the temperature was increased. This could explain the beneficial temperature sensitivity of the effective lifetime observed for cells from the top.

The main parameters affecting the performance of a mc-Si PERC cell are the bulk lifetime, the resistivity and the dislocation density [8, 14]. Any performance-limiting factor attributed to the Al-BSF architecture is assumed to have a similar influence on all cells from one ingot. Therefore, the mechanisms affecting the performance of PERC cells are assumed to be good indicators of performance variations for the Al-BSF cells used in this study. Since tri-doped compensated mc-Si was used to fabricate the cells for this study, the resistivity is assumed to be relatively uniform throughout the ingot. The concentration and composition of defects, however, varies significantly because of the directional solidification process that causes most impurities to segregate and accumulate towards the top of the ingot. In addition, back-diffusion from the crucible introduces a high level of impurities at the bottom [6]. The dislocation density also varies throughout a mc-Si ingot and is typically found to increase towards the top [8]. Crystal defects could therefore be responsible for the improved temperature sensitivity observed for cells from the top, however, further studies are needed to explore this hypothesis.

B.IV. Summary

In this study, the combined effect of temperature and ingot position on the V_{oc} of mc-Si cells has been investigated. The V_{oc} was found to decrease with ingot position for a range of light intensities. However, the relative decrease in V_{oc}, when the cell temperature was increased from 25 °C to 65 °C, was found to be lowest for cells from the top. The relative change in temperature sensitivity throughout the ingot was found to be similar for illumination conditions of 0.1, 0.5 and 1 Sun. At 1 Sun, the TCs of the V_{oc} were found to vary with approximately 5 % throughout the ingot.

The lifetime was found to decrease with ingot height for injection levels of around $10^{14}\,\text{cm}^{-3}$. The effective lifetime increased for all cells when the temperature was increased from 25 °C to 65 °C. However, the lifetime increase was considerably larger for top cells, ranging from $40-48\,\%$ for the injection levels considered. For bottom cells, the increase was found to be $20-30\,\%$. The observed variation in both V_{oc} and effective lifetime with cell position in the ingot illustrates the influence of cell position for applications at elevated temperatures.

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Paper C

A high-accuracy calibration method for temperature dependent photoluminescence imaging

Published as:
S. T. Kristensen, S. Nie, M. S. Wiig, H. Haug, C. Berthod, R. Strandberg, and Z. Hameiri, ”A high-accuracy calibration method for temperature dependent photoluminescence imaging”, *AIP Conference Proceedings*, vol. 2147, p. 020007, 2019.
doi: 10.1063/1.5123812

A high-accuracy calibration method for temperature dependent photoluminescence imaging

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Abstract **— This work demonstrates a novel technique for calibrating temperature dependent photoluminescence (PL) images of silicon wafers with high accuracy. The PL signal is calibrated using a heat-controlled photoconductance (PC) stage integrated into the PL imaging system. The PC signal is measured in true steady-state condition and used to determine the calibration constant under the same temperature and illumination as the PL image, thus providing a high-precision calibration. This results in a robust method for imaging of important physical parameters, such as the minority carrier lifetime and the implied voltage at different temperatures, as well as the temperature coefficients and the recombination parameter γ. The method is verified through comparison with a similar PL imaging system, where the calibration is made from a conventional flash-based quasi-steady-state PC measurement. Finally, the method is applied to compensated multicrystalline silicon wafers, demonstrating the usefulness of the proposed calibration routine for analysing complex materials.**

C.I. Introduction

Photoluminescence (PL) imaging is a spatially resolved measurement technique enabling fast acquisition of important parameters for silicon wafers and cells [1]. Of these, a key parameter is the minority carrier lifetime [2], which is essential for estimating the final performance of a solar cell.

In the later years, the interest in PL imaging at elevated temperatures has increased, since knowledge about the temperature sensitivity of a material can unlock important information about the material properties [3–6]. In addition, it can give a more accurate representation of the performance of a photovoltaic device under real operating conditions, where temperatures can differ significantly from the standard test condition (STC) temperature of 25 °C [7].

Calibration of temperature dependent PL images is a complex task. This is due to a strong temperature dependence of the luminescence signal from a silicon sample, originating from the temperature dependence of the radiative recombination coefficient, the optical properties of the sample, the spectral distribution of the luminescence signal, and the temperature sensitivity of the camera [8]. Current calibration procedures for elevated temperatures include modeling [3], purely optical measurement techniques utilizing the time dependence of the luminescence signal [4], or calibration by temperature dependent quasi-steady-state (QSS) photo-conductance (PC) measurements [5]. A QSS-PC based calibration is the most accessible option in many laboratories since it requires only standard equipment and carry limited assumptions. However, some uncertainties might be introduced since the calibration process and image acquisition are conducted on separate systems [5].

In this paper, we present a calibration routine based on a direct measurement of the PC of a wafer during PL image acquisition. The calibration parameters are therefore obtained under similar temperature and illumination conditions as the PL image, resulting in a high-precision calibration with even fewer assumptions.

C.II. Experimental Method

Figure C.1 illustrates the measurement setup consisting of a temperature-controlled PC stage integrated into a PL imaging system. The PL imaging system consists of an 808 nm laser for excitation of the wafer and a silicon charge-coupled device (CCD) camera for collection of the PL signal emitted from the wafer. Several filters are attached in front of the camera to remove reflections of the laser beam and reflections of the PL signal originating from the stage. The collected PL signal from the wafer, I_{PL}, can be expressed

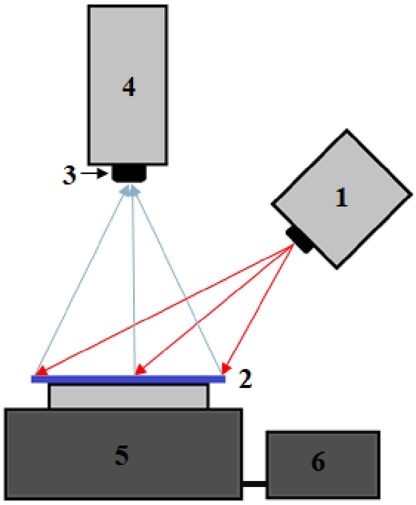

Figure C.1: Illustration of the temperature dependent PL imaging setup (System I) consisting of: (1) 808 nm laser diode; (2) sample; (3) objective and filters; (4) Si CCD camera; (5) combined PC and heat stage; (6) temperature-controller.

as

$$I_{\mathrm{PL}} = A_i B\, \Delta n \left(\Delta n + N_{\mathrm{dop}}\right), \tag{C.1}$$

where A_i is a constant depending on the specific PL measurement system and sample, B denotes the radiative recombination coefficient [8], Δn is the excess carrier density, and N_{dop} is the bulk doping concentration.

The temperature-controlled PC stage (Sinton Instruments WCT-120TS [9]) measures the conductance of the wafer using an inductive coil, thus allowing a direct measure of the PC during image acquisition in true steady-state at any desired temperature from 25 °C to 200 °C. Note that the temperature was kept at maximum 75 °C during our experiments to prevent the equipment from heating up and to avoid permanent changes in the carrier lifetime of the wafers. Using a suitable mobility model applied at the specific conditions of image acquisition, the measured PC, $\Delta\sigma$, can be translated into an average Δn in the coil area of the wafer, Δn_{PC}, using [10]

$$\Delta n_{\mathrm{PC}} = \frac{\Delta\sigma}{qW\mu_{\mathrm{tot}}}, \tag{C.2}$$

where q denotes the elementary charge, W is the thickness of the silicon wafer, and μ_{tot} is the sum of the mobilities of electrons and holes in the material. Combining Eqs. (C.1) and (C.2) and assuming that Δn_{PC} equals the average Δn in the coil area of the PL image, the calibration constants $A_i B$ can be determined. Hence, Δn can be obtained for each pixel of the PL image. This allows for a high-accuracy conversion of the PL images into images of important device parameters, such as the effective minority carrier lifetime, τ_{eff}, and the implied open circuit voltage, iV_{oc}. In steady-state, τ_{eff} is directly proportional to Δn and can be calculated using $\tau_{\mathrm{eff}} = \Delta n / G$ where G is the generation rate. The iV_{oc} can be determined from Δn using [10]

$$V_{\mathrm{oc}} = \frac{kT_{\mathrm{c}}}{q} \ln \left[\frac{\Delta n(\Delta n + N_{\mathrm{dop}})}{n_i^2} \right], \tag{C.3}$$

where k denotes Boltzmann's constant, T_{c} is the temperature of the cell, and n_i is the intrinsic carrier concentration at the specific temperature of interest.

Following the method described in Ref. [6], additional maps can be generated displaying the temperature coefficient of iV_{oc}, $\beta_{iV_{\mathrm{oc}}}$, and the recombination parameter γ, related to V_{oc} through [11]

$$\beta_{V_{\mathrm{oc}}} = \frac{dV_{\mathrm{oc}}}{dT_{\mathrm{c}}} = -\frac{E_{\mathrm{g0}}/q - V_{\mathrm{oc}} + \gamma k T_{\mathrm{c}}/q}{T_{\mathrm{c}}}, \tag{C.4}$$

where E_{g0} is the semiconductor bandgap energy extrapolated to 0 K. The parameter γ includes the temperature dependence of the dark saturation current, J_0, and gives information regarding the dominating recombination mechanism in the material [7]. This setup will be referred to as 'System I' hereafter.

To verify the method, the wafers were characterized using a similar PL imaging system, but with a calibration process performed on a separate PC system (also a WCT-120TS from Sinton Instruments) following Ref. [5]. The calibration is based on conventional QSS-flash lifetime curves acquired at different temperatures to obtain Δn_{PC} and τ_{eff} at comparable generation conditions as the PL images. The obtained τ_{eff} is then assumed to equal the average τ_{eff} in the coil area of the PL image. The setup will be referred to as 'System II' hereafter. A constant photon flux of $1.2 \cdot 10^{17}\,\mathrm{cm^{-2}s^{-1}}$ was used for excitation in both Systems I and II.

Two different wafers were characterized to compare Systems I and II: Wafer A) a 2" n-type monocrystalline silicon (mono-Si) wafer with a resistivity of $3-4\,\Omega\cdot$cm and passivated with an aluminum oxide (AlO$_x$) and silicon nitride (SiN$_x$) stack layer, and Wafer B) a 6" p-type multicrystalline silicon (mc-Si) wafer with a resistivity of $2-3\,\Omega\cdot$cm passivated with SiN$_x$. The wafers were characterized using both systems within a period of three weeks. The stability of the wafers was monitored using a WCT-120TS lifetime tester. A third and fourth wafer were used for application of System I: Two 6" compensated p-type mc-Si wafers originating from the same central brick of a compensated ingot containing boron, gallium and phosphorus, with a resistivity of $1-2\,\Omega\cdot$cm. Wafer C) was taken from the bottom of the brick at a relative height of 0.06, while Wafer D) was taken from the top of the brick at a relative height of 0.82. Both wafers were passivated with hydrogenated amorphous silicon (a-Si:H) and SiN$_x$.

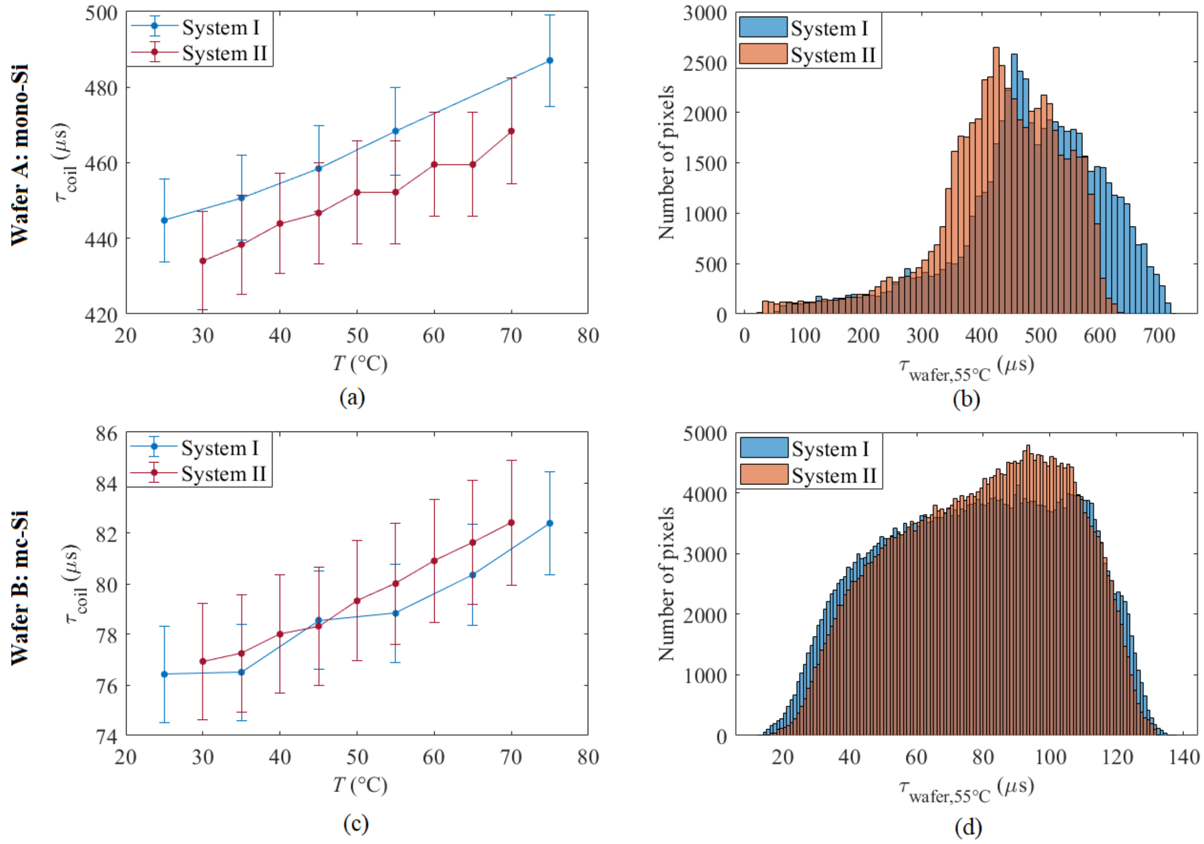

Figure C.2: Average τ_{eff} in the PC coil area of the PL images of (a) Wafer A and (c) Wafer B measured using Systems I and II at various temperatures; (b) lifetime histogram of Wafer A and (d) Wafer B measured using both Systems I and II at 55 °C.

C.III. Results and Discussion

A. Verification: Average and Spatial Comparison

The average τ_{eff} in the PC coil area of the PL image of Wafer A and Wafer B can be seen in Figs. C.2(a) and (c), respectively, as a function of temperature measured on both systems. The errors on System I are estimated based on the uncertainty of the PC measurement and the repeatability of the system, the former found to have the biggest impact on the calibrated lifetime. The errors on System II are estimated based on repeatability of the lifetime measurement. The errors thus represent minimum uncertainties associated with the Systems I and II. A good agreement within the estimated errors is observed when comparing the two systems. System II displays slightly lower average τ_{eff} for Wafer A compared to System I, however, the variation is within the estimated minimum errors. The temperature sensitivity of τ_{eff} shows similar trends on both systems for both wafers.

To investigate the spatial distribution across the wafers, histograms were created to examine the number of pixels with different lifetimes. This is shown in Figs. C.2(b) and (d) for Wafers A and B, respectively, measured on both systems at 55 °C. A similar shape of distributions can be observed on the two systems; However, System II is found to exhibit a slightly narrower distribution compared to System I and an increased number of high-lifetime pixels for both wafers. This could be a consequence of differences in reflection from the PC coil area in the two systems, causing a larger contrast in the PL signal around the coil area of System I (visible on raw PL images of the mono-wafer). Note that the lifetimes of Wafer A measured on System II are shifted to slightly lower values compared to System I, as expected from the average values.

Good agreement is found between both calibration procedures for the studied samples, and System I can be considered a further development of System II with a more robust calibration routine. The new calibration is performed directly in the PL system under true steady-state condition using the same illumination and temperature as the PL image resulting in fewer possible errors. Furthermore, both Systems I and II obtain their calibration constants by correlating the measured PC signal of the wafer with the location of the PC coil in the PL image. Since the PC stage is built into System I, the calibration is performed based on the correct location on the wafer. This reduces uncertainties arising especially for non-uniform materials such as mc-Si wafers.

B. Temperature Sensitivity of Compensated Silicon Wafers

When investigating the temperature sensitivity of solar cells, average parameter values are often used. Most commonly, the temperature sensitivity of V_{oc} is quantified using $\beta_{V_{\mathrm{oc}}}$ defined in Eq. (C.4) [11]. As demonstrated in Ref. [6], a large variation of this parameter can be found across a wafer which suggests that spatial analysis is important for an in-depth analysis.

To illustrate the usefulness of our procedure for characterization of more complex materials, and for understanding the temperature sensitivity of iV_{oc} across different wafers, the method is applied to two compensated mc-Si wafers originating from the bottom and the top of a central brick. Images of the relative $\beta_{iV_{\mathrm{oc}}}$ [Eq. (C.4), normalized to iV_{oc} at 25 °C at each pixel] of Wafers C and D are shown in Figs. C.3(b) and (e), respectively. Large variations are found across both wafers, however, the non-uniformity is more pronounced for Wafer D. This wafer mostly shows a lower temperature sensitivity than Wafer C and additionally contains small areas with much lower sensitivity than the rest of the wafer [bright areas in Fig. C.3(e)].

To correlate $\beta_{iV_{\mathrm{oc}}}$ with material quality and recombination mechanisms, maps of iV_{oc} and γ are shown in Figs. C.3(a) and (c) for Wafer C and Figs. C.3(d) and (f) for Wafer D. A region of interest (ROI) is selected on Wafer D exhibiting reduced temperature sensitivity. Comparing Figs. C.3(d) and (e), the ROI can be identified as a low-quality area on the wafer containing patches with reduced iV_{oc}. This is surprising, since Eq. (C.4) predicts

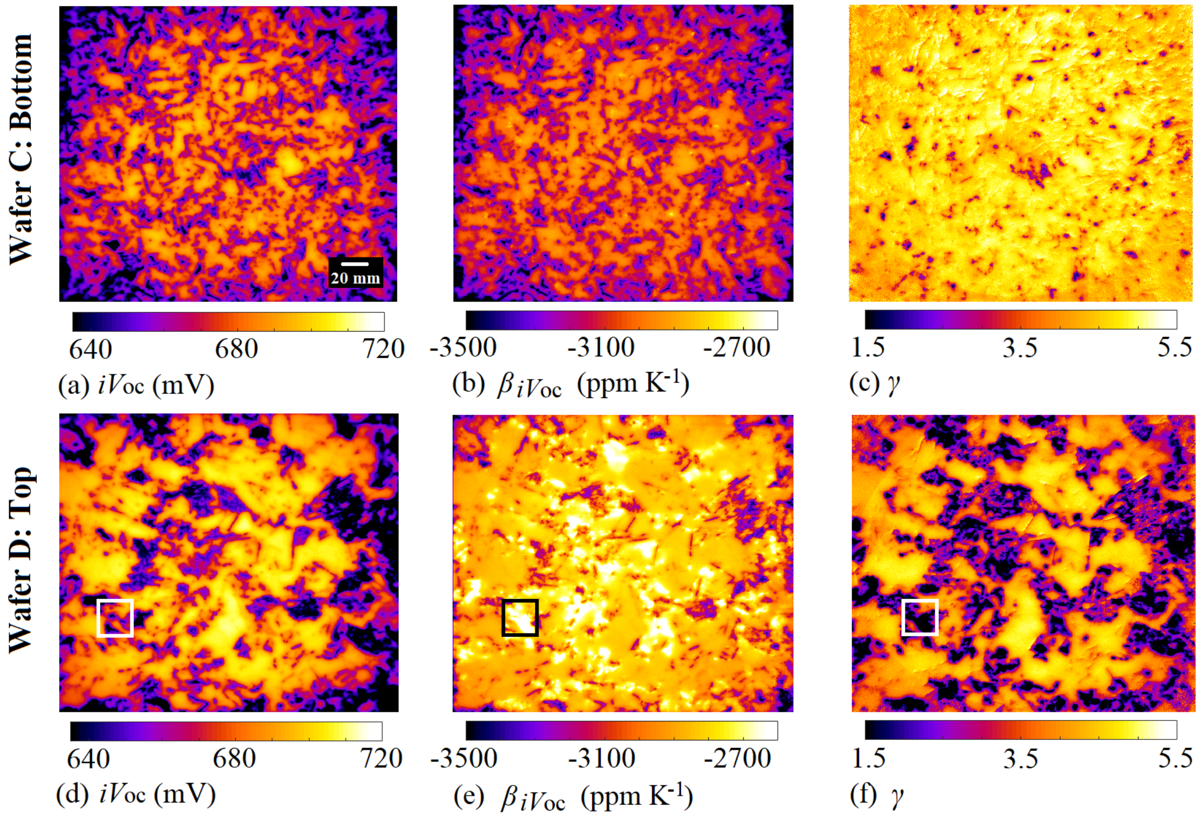

Figure C.3: Images of iV_{oc} at room temperature, $\beta_{iV_{\text{oc}}}$, and γ of two compensated mc-Si wafers from (a-c) the bottom and (d-f) the top of a central brick. The wafers were characterized using System I.

low iV_{oc} areas to result in an increased temperature sensitivity, as is the case on other areas on the wafer. Turning our attention to Fig. C.3(f), the ROI is found to originate from an area with γ values sufficiently low to counteract the reduced iV_{oc}, resulting in lower temperature sensitivity in that specific area.

To examine the spatial distribution of γ values across the Wafers C and D, Fig. C.4 shows histograms of the number of pixels with different γ values. Wafer D is found to show a considerably larger variation in γ values across the wafer compared to Wafer C. This indicates that different recombination centers are limiting the two wafers and influencing their temperature sensitivity.

C.IV. Summary

In this paper, we presented a novel calibration routine for temperature dependent PL imaging based on a direct measurement of the PC of a wafer during image acquisition. This allows for the calibration constant to be obtained in true steady-state under similar temperature and illumination conditions as the PL image, resulting in a high-precision calibration with only few assumptions. The method was verified through comparison with

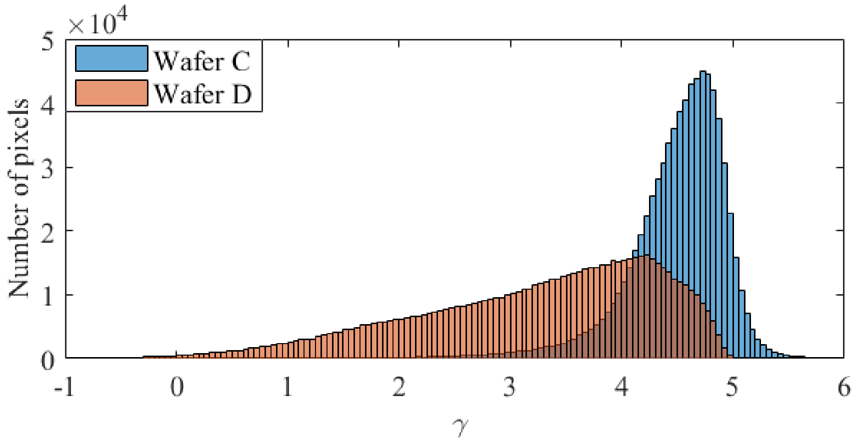

Figure C.4: Histograms of γ values for Wafers C (bottom wafer) and D (top wafer).

a similar PL imaging system with a different calibration process based on conventional flash-based QSS-PC measurements performed on a separate system. Good agreement was found between the two measurement systems when analyzing both a mono-Si and a mc-Si wafer and the proposed method can be considered a further development of existing procedures, however, with a more robust calibration routine.

Finally, the method was applied to two compensated mc-Si wafers from different brick positions to demonstrate the usefulness of our technique for characterizing more complex materials. Large variations in temperature sensitivity and γ values were found across the wafers. An area with low temperature sensitivity was investigated and surprisingly identified as a low-iV_{oc} area on the wafer, indicating that the temperature sensitivity in that specific area is determined by a recombination mechanism with a low γ value. The two wafers were found to exhibit different γ values, indicating that the different recombination centers must be limiting the two wafers and influencing their temperature sensitivity.

Acknowledgments

The authors would like to thank Jan Ove Odden (REC Solar Norway), Daniel Chung (UNSW), and Kyung Kim (UNSW) for providing wafers for the study; and SIRF (UNSW) and Rune Søndenå (IFE) for passivating the wafers.

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Paper D

Temperature sensitivity of multicrystalline silicon solar cells

Published as:

C. Berthod, **S. T. Kristensen**, R. Strandberg, J. O. Odden, S. Nie, Z. Hameiri, and T. O. Sætre, "Temperature sensitivity of multicrystalline silicon solar cells", *IEEE Journal of Photovoltaics*, vol. 9, pp. 957-964, 2019.

doi: 10.1109/JPHOTOV.2019.2911871

Temperature sensitivity of multicrystalline silicon solar cells

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Abstract **— This paper presents an experimental investigation of the temperature coefficients of multicrystalline silicon solar cells. The aim was to determine if some cell parameters can affect positively the temperature sensitivity without detrimental impact on the efficiency. Commercial solar cells with different bulk resistivities, compensation levels, and cell architectures have been studied. We report that the base net doping, the location of the solar cell along the brick and the cell architecture have significant impacts on the temperature coefficients. Moreover, we show how the change in recombination mechanisms along the ingot height affects the temperature coefficients. The compensation level was observed to have no significant effect on the temperature coefficients. We also demonstrate why aluminum back-surface-field and passivated emitter rear contact solar cells have similar temperature sensitivities despite a better passivation and higher open-circuit voltage for the latter cell architecture. Finally, we have found that reducing the bulk resistivity can improve the solar cells' performance in hot climates.**

D.I. Introduction

Solar cells are normally characterized under standard test conditions (STC), with a temperature of 25 °C, a light intensity of $1000\,\mathrm{W/m^2}$ with an air mass (AM) 1.5G spectrum although solar panels operating in the field very often exceed 25 °C. Temperature increases have a negative effect on solar cell performance [1–3]. In the recent years, more focus has been given to mitigating the losses caused by high temperatures either by using advanced cell architectures [4, 5] or by engineering sub-bandgap reflection and radiative cooling [6].

The temperature sensitivity of a solar cell depends on many factors, among them the most well-known element is the open-circuit voltage, V_{oc}. A reduction of the temperature sensitivity can be achieved by increasing the open-circuit voltage, thanks to the use of high-performance cell structures [4,5,7–10]. This means that an efficiency improvement, if caused by an increase of the open-circuit voltage, results in a reduction of the temperature sensitivity. Other factors can also affect the temperature coefficients, such as the base net doping [11–13] the use of an upgraded-metallurgical grade silicon (UMG-Si) as feedstock [11, 14–16], as well as indirect effects such as the wafer position in the brick [17] and light-induced degradation [18].

In this paper, we investigate the possibility of engineering the temperature coefficients. This is done by studying the impacts of the net doping with the compensation level on the temperature sensitivity of multicrystalline silicon (mc-Si) solar cells. First, expressions of the temperature coefficients made by previous authors [1–3, 8] are presented to give an overview of the dependencies with cell parameters [short-circuit current (I_{sc}), open-circuit voltage, fill factor (FF), and efficiency (η)]. Second, experimental temperature coefficients are presented as a function of the cell's position in the brick and of the cell parameters. The brick position of the cells with the lowest temperature sensitivities is investigated. Finally, we show how lowering the resistivity can be a valid method to engineer the temperature coefficients.

D.II. Theoretical Background

The efficiency of a solar cell varies linearly with temperature for the majority of cell types under normal operating temperatures [2]. This variation can be characterized using temperature coefficients. The relative temperature coefficient of a parameter X, β_X, is defined as the rate of change of this parameter over the considered temperature range divided by the value of the parameter at 25 °C

$$\beta_X = \frac{1}{X\,(25°\mathrm{C})} \frac{dX(T)}{dT}\bigg|_{T=25°\mathrm{C}} . \tag{D.1}$$

The efficiency can be expressed as the product of the open-circuit voltage, the short-circuit current, and the fill factor, divided by the incident solar power. Differentiating this relation and dividing by the efficiency yields

$$\beta_\eta = \beta_{V_\mathrm{oc}} + \beta_{I\mathrm{sc}} + \beta_{FF}. \tag{D.2}$$

The first term is the relative temperature coefficient of the open-circuit voltage (β_{V_oc}) which can be expressed as follows [3]:

$$\beta_{V_\mathrm{oc}} = \frac{1}{V_\mathrm{oc}}\frac{dV_\mathrm{oc}}{dT_\mathrm{c}} = -\frac{1}{V_\mathrm{oc}T_\mathrm{c}}\left[\frac{E_\mathrm{g0}}{q} - V_\mathrm{oc} + \gamma\frac{kT_\mathrm{c}}{q}\right], \tag{D.3}$$

where k, q, T_c, and E_g0 are Boltzmann's constant, the elementary charge, the cell temperature, and the bandgap energy linearly extrapolated to 0 K, respectively. γ is a parameter depending on the limiting recombination mechanisms in the cell and it can be expressed using the external radiative efficiency (ERE) at the open-circuit voltage by [1]

$$\gamma = 1 - \frac{d\ln ERE_\mathrm{oc}}{d\ln T_\mathrm{c}} + \left(2\frac{d\ln E_\mathrm{g}}{d\ln T_\mathrm{c}} - \frac{d\ln j_\mathrm{sc}}{d\ln T_\mathrm{c}}\right), \tag{D.4}$$

where E_g is the bandgap energy of the material and j_sc the short-circuit current density. ERE is defined as the fraction of the total dark current recombination that is emitted from the cell. γ usually take values from 0 to 5, such as 1.2 in the radiative limit of a crystalline silicon solar cell or 5 for a solar cell limited by Shockley-Read-Hall recombination at the junction (neglecting the temperature dependence of the carrier lifetime and the surface recombination velocity) [19]. The open-circuit voltage decreases with the temperature due to the increase of the dark saturation current, resulting in a negative β_{V_oc}.

The second term of (D.2) is the relative temperature coefficient of the short-circuit current ($\beta_{I\mathrm{sc}}$) . The short-circuit current can be written as the product of the ideal short-circuit current ($I_\mathrm{sc,1sun}$) and the collection fraction (f_c) . The latter is the fraction of useful photons (with $E \geq E_\mathrm{g}$) which are collected as carriers in the device. $\beta_{I\mathrm{sc}}$ can be expressed as follows [2]

$$\beta_{I\mathrm{sc}} = \frac{1}{I_\mathrm{sc}}\frac{dI_\mathrm{sc}}{dT_\mathrm{c}} = \frac{1}{I_\mathrm{sc,1sun}}\frac{dI_\mathrm{sc,1sun}}{dE_\mathrm{g}}\frac{dE_\mathrm{g}}{dT_\mathrm{c}} + \frac{1}{f_\mathrm{c}}\frac{df_\mathrm{c}}{dT_\mathrm{c}}. \tag{D.5}$$

This temperature coefficient depends on the variation of f_c with temperature, and on the increase of current induced by the bandgap decrease with temperature. Therefore, the coefficient is positive but with a smaller amplitude than β_{V_oc}.

Finally, the last term of (D.2) is the relative temperature coefficient of the fill factor (β_{FF}) . This coefficient can be written as follows [8]

$$\begin{aligned}\beta_{FF} =& \frac{1}{FF}\frac{dFF}{dT_\mathrm{c}} = (1 - 1.02FF_0)\left(\frac{1}{V_\mathrm{oc}}\frac{dV_\mathrm{oc}}{dT_\mathrm{c}} - \frac{1}{T_\mathrm{c}}\right) \\ &- \frac{R_\mathrm{s}}{(V_\mathrm{oc}/J_\mathrm{sc} - R_\mathrm{s})}\left(\frac{1}{R_\mathrm{s}}\frac{dR_\mathrm{s}}{dT_\mathrm{c}}\right),\end{aligned} \tag{D.6}$$

where R_s is the series resistance, FF_0 the ideal fill factor (free of series and shunt resistance effects), and v_oc is the normalized open-circuit voltage. The latter two parameters can be expressed as follows:

$$FF_0 = \frac{v_\mathrm{oc} - \ln\left(v_\mathrm{oc} + 0.72\right)}{v_\mathrm{oc} - 1} \qquad v_\mathrm{oc} = \frac{q}{nkT} V_\mathrm{oc}\,. \tag{D.7}$$

An increase in the open-circuit voltage will increase the FF_0 and reduce the β_{V_oc} both resulting and in an increase of β_{FF}. The right-hand term in (D.6) is expected to have more variations for cells with large R_s values.

D.III. Experimental Procedure

In this paper, mc-Si solar cells were investigated. Two groups of high-performance G5-ingots were produced, and all wafers were picked from the center brick of these ingots.

The first group of ingots consists of four ingots with the same targeted resistivity and different blend-in-ratios of compensated silicon (made of Elkem Solar Silicon) and non-compensated silicon (material produced by chemical vapor deposition). The wafers were processed into aluminum back surface field (Al-BSF) cells in a laboratory production line. The blend-in-ratio was varied between the ingots to study the effect of compensation level on the temperature coefficients. Ingots with larger blend-in-ratios of Elkem Solar Silicon will see their compensation levels increasing due to a larger addition of compensating dopants. The compensation level can be calculated by dividing the total dopant concentration by the net doping, as shown in the following equation:

$$C_l = \frac{[\mathrm{B}] + [\mathrm{Ga}] + [\mathrm{P}]}{\left([\mathrm{B}^-] + \left[\mathrm{Ga}^-\right]\right) - [\mathrm{P}^+]}. \tag{D.8}$$

The second group of ingots is composed of four ingots with different resistivities ranging from 0.5 to $1.3\,\Omega \cdot \mathrm{cm}$. The ingots were made from the same feedstocks as described previously, one consisting entirely of non-compensated silicon and three of 70 % compensated silicon. Passivated emitter rear contact (PERC) cells were produced in an industrial production line. In this group, the effect of different resistivities on the temperature coefficients is of interest. The initial dopant concentrations and the net doping for these ingots can be found in Table D.1, the data are taken from [20].

The solar cells are standard $15.6 \times 15.6\,\mathrm{cm}^2$ (6 inch) cells, with an approximate thickness of $200\,\mu\mathrm{m}$. The originating wafers were selected at various locations distributed along the height of a center brick of each ingot. All cells underwent a 48 h light-soaking treatment to ensure a degraded state and avoid instabilities during measurements. All values for the distinct ingots are displayed in Table D.2. Note that the average efficiency of Ref is slightly lower than the one for Res 1.3. This is not usually encountered by the

Table D.1: Initial dopant concentrations in the melt, with the net doping averaged between 0 and 90 % of the relative ingot height, for the ingots with different resistivities.

Ingot name	P (cm^{-3})	B (cm^{-3})	Ga (cm^{-3})	Net doping (cm^{-3})
Ref	1.9×10^{16}	5.2×10^{16}	1.6×10^{17}	1.2×10^{16}
Res 0.5	1.9×10^{16}	3.0×10^{16}	1.6×10^{17}	3.8×10^{16}
Res 0.9	1.9×10^{16}	2.4×10^{16}	1.6×10^{17}	1.8×10^{16}
Res 1.3	–	1.3×10^{16}	–	1.2×10^{16}

ingot's producer (REC Solar). Therefore, we suppose it originates from fluctuations in the solidification process from ingot to ingot.

The current-voltage (IV) characteristics of the cells were measured under a standard AM1.5G spectrum with a NeonSee AAA sun simulator. The temperature coefficients of a cell were obtained by measuring the IV characteristics at different temperatures ranging from 25 to 70 °C. The temperature of the measurement chuck was controlled by a water heater. A linear fitting over the temperature range is then performed for each parameter and normalized to 25 °C to obtain the relative temperature coefficient of this parameter.

Note that the values for the open-circuit voltage, the short-circuit current, and the fill factor were normalized with the maximum value of each parameter, and are called "relative" values, so that it is not confused with the normalized open-circuit voltage defined in (D.7).

Sister wafers from ingot CL 4 (see Table D.2) were examined to study the material properties more closely. The wafers were gettered and passivated with silicon nitride (SiN_x) and hydrogenated amorphous silicon (a-Si:H). They were then analyzed using a temperature-dependent photoluminescence (PL) imaging system consisting of an 808 nm diode laser and a silicon charge-coupled device camera. A Sinton WCT-120TS (Sinton Instruments) was integrated into the PL system and was used both to adjust the temperature of the wafer and to calibrate the PL signal into carrier lifetimes. For a more detailed description of the setup and the calibration procedure, see [21]. PL images were acquired at 25 and 70 °C and calibrated into implied V_{oc} at the two temperatures. Maps of $\beta_{iV_{oc}}$ and γ were then obtained by applying (D.3) at each pixel, following the method in [22].

Table D.2: Description of ingots.

Cell architecture	Ingot name	Targeted resistivity ($\Omega \cdot \mathrm{cm}$)	Dopants	Blend-in ratio (% ESS®)	Efficiency ± STD (%)	V_{oc} ± STD (mV)	I_{sc} ± STD (A)	FF ± STD (%)
Al-BSF	CL1	1.25	B-P	25	16.6 ± 0.2	631 ± 3	8.01 ± 0.05	80.1 ± 0.1
	CL2	1.25	B/Ga-P	40	16.9 ± 0.2	634 ± 3	8.12 ± 0.06	80.1 ± 0.1
	CL3	1.25	B/Ga-P	56	17.0 ± 0.2	634 ± 2	8.14 ± 0.04	79.9 ± 0.1
	CL4	1.25	B/Ga-P	73	16.9 ± 0.1	634 ± 1	8.09 ± 0.02	80.2 ± 0.1
PERC	Ref	1.3	B	0	18.0 ± 0.4	637 ± 8	8.70 ± 0.09	78.9 ± 0.2
	Res 0.5	0.5	B/Ga-P	70	18.2 ± 0.2	650 ± 3	8.57 ± 0.04	79.5 ± 0.2
	Res 0.9	0.9	B/Ga-P	70	18.6 ± 0.3	650 ± 5	8.77 ± 0.07	79.5 ± 0.2
	Res 1.3	1.3	B/Ga-P	70	18.3 ± 0.2	644 ± 3	8.76 ± 0.05	79.1 ± 0.2

D.IV. Results

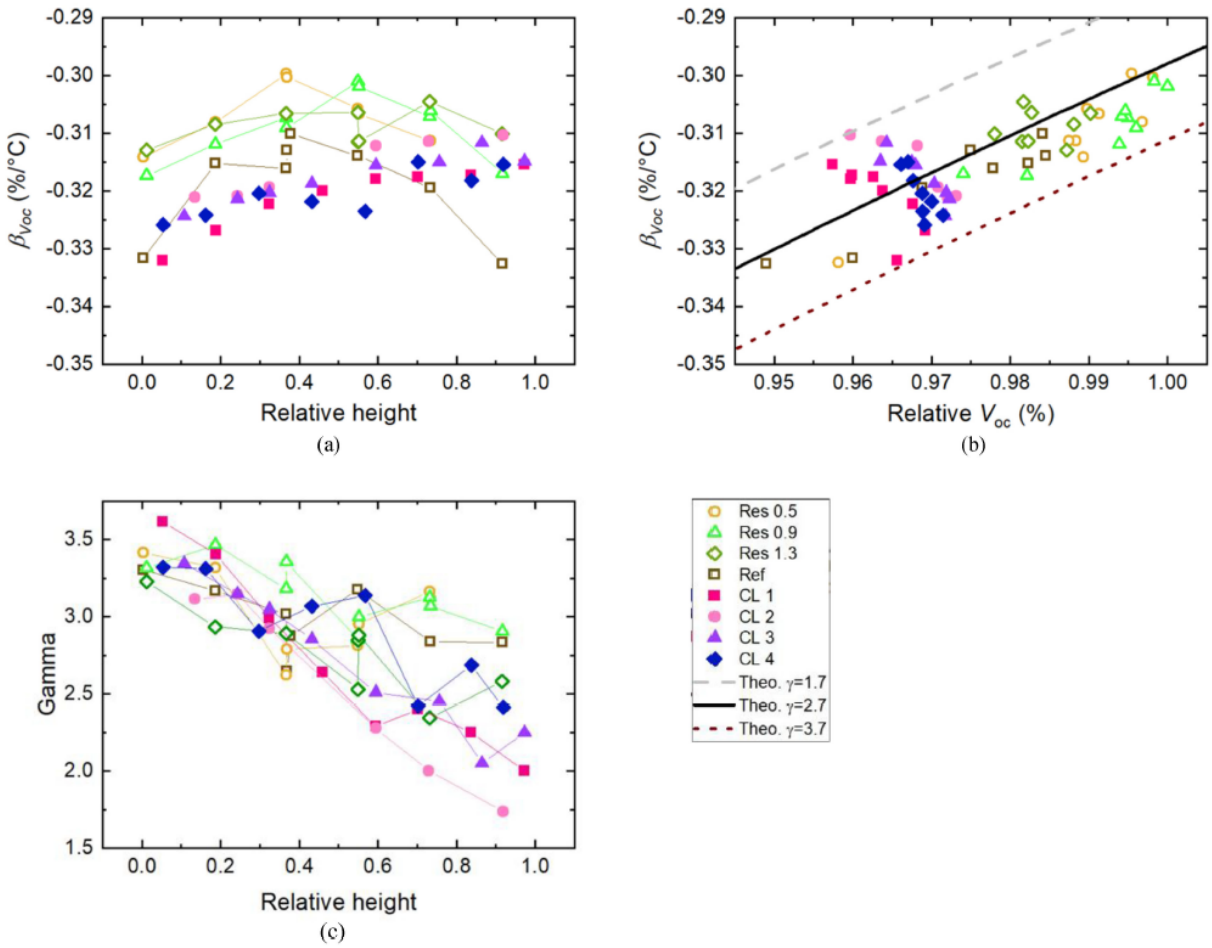
The four main solar cell parameters vary with the bulk resistivity and the compensation level, which all (including the cell parameters) depend on the position of the cell along the brick. This increases the degree of correlation between these parameters and complicates a correct understanding of the causality. As an example, $\beta_{V_{\mathrm{oc}}}$ is improving toward the top of the ingot for Al-BSF cells even though the open-circuit voltage shows a corresponding decrease as shown in a previous study [17]. This result suggests a direct dependency of $\beta_{V_{\mathrm{oc}}}$ with the relative height in the brick which needs to be demonstrated. Therefore, in the next section, the temperature coefficients of the four cell parameters will be studied as a function of the cell parameters themselves and the cell's position in the brick.

A. Temperature Coefficient of the Open-Circuit Voltage

In Fig. D.1(a), where $\beta_{V_{\mathrm{oc}}}$ is plotted as a function of the relative height in the brick, two distinct trends are observed. The Al-BSF cells (CL 1 to 4) have the highest $\beta_{V_{\mathrm{oc}}}$ at the top of the ingot, while the $\beta_{V_{\mathrm{oc}}}$ of the PERC cells peak in the middle and decrease near the top. To understand this difference, first the γ parameter will be evaluated. From Fig. D.1(c) we observe that the γ values are decreasing along the whole ingot, except for the PERC cells which flattens out near the top. Nevertheless, the two different architectures show very similar values for γ. This could imply that both types of cells are limited by the same recombination mechanisms. The decreasing trend has a positive effect on $\beta_{V_{\mathrm{oc}}}$, i.e., it increases with increasing ingot height. The decrease of $\beta_{V_{\mathrm{oc}}}$ for the PERC cells is thus explained by a large decrease of their V_{oc} (not shown here) along the ingot height.

These results are summed up in Fig. D.1(b), where the Al-BSF cells (CL 1 to 4) are found to not follow the V_{oc} trend, instead the data points go perpendicularly as a consequence of the γ variations. The $\beta_{V_{\mathrm{oc}}}$ values of the PERC cells are more aligned with the inserted theoretical curve with $\gamma = 2.7$ because of the larger variation of V_{oc} for these cells.

The ingots with different blend-in-ratios vary in compensation levels: starting values at the bottom of the ingot from 1.4 to over 2 for CL 1 and CL 4, respectively (see Fig. D.7 for all values of compensation level). However, these results show that the compensation level does not have any impact on $\beta_{V_{\mathrm{oc}}}$ with these levels and this cell architecture. Indeed, the compensation level of the studied cells is mainly below 2.5, which is a relatively low value and higher compensation levels might have an impact. Moreover, the cell architecture, Al-BSF, is not the most sensitive to the material quality and a difference could be observed with more advanced cell architectures such as heterojunction cells. In contrary, the ingots with different resistivities exhibit an advantageous $\beta_{V_{\mathrm{oc}}}$ for the cells



(a)

(b)

(c)

Figure D.1: $\beta_{V_{oc}}$ as a function (a) of the relative height in the brick and (b) of the relative open-circuit voltage with three iso-γ curves, γ-parameter extracted from Eq. (D.3), as a function of (c) the relative height in the brick, for the ingots defined in Table D.2.

made from a low-resistivity material. This is explained by an improvement of V_{oc} [see in Fig. D.1(b)]

To examine what is causing the change in γ values, mapping of this parameter was conducted on sister wafers from ingot CL 4. Fig. D.2 shows the harmonic average of γ over the wafers and the measured γ of the cells as a function of relative brick height. Like the cells, the wafers exhibit a decreasing γ with increasing brick height. However, the wafers display a larger variation along the brick compared to the cells, indicating a variation in limiting recombination mechanism along the brick. The net dopings of the compensated ingots are more constant than the reference ingot [20], we suppose the cause of the variation of γ is a crystallographic defect variation along the ingot.

Figs. D.3(d)-(f) show γ maps of three wafers originating from the bottom, middle, and the top of the brick. The three wafers are highlighted by star symbols in Fig. D.2 for reference. From the maps we observe a relatively uniform and large γ parameter across

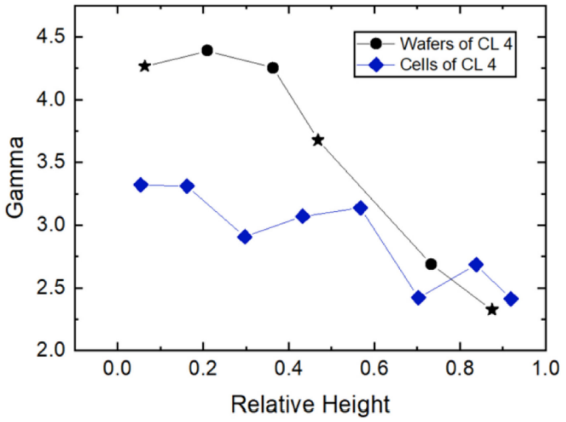


Figure D.2: γ as a function of the relative height in the brick, for wafers and cells in ingot CL 4. The star symbols correspond to the wafers shown in Fig. D.3.

the bottom wafer, whereas the other wafers consist of large areas with low γ values. This is especially the case for the top wafer which consists of large patches with γ values below 2. From corresponding lifetime maps shown on Figs. D.3(a)-(c), the low-γ patches on the top and middle wafers can be identified as areas with high dislocation densities. This suggests that the decrease in γ with brick height observed both for wafers and cells is caused by an increase in dislocation density. These results are corroborated by a recent study that has shown that the temperature coefficient of the lifetime is increasing toward the top of the ingot, due to the increase in low lifetime areas. This causes a decrease of γ [23].

B. Temperature Coefficient of the Short-Circuit Current

In Fig. D.4(a), where $\beta_{I\mathrm{sc}}$ is plotted as a function of the relative height, two different trends are observed for the two different cell architectures. Al-BSF cells (ingots CL 1 to 4) display an increasing $\beta_{I\mathrm{sc}}$ along the ingot height, while no trend is observed for the PERC. The latter has higher I_{sc} values, as can be seen in Fig. D.4(b), as expected for this cell architecture. The two cell types form two quasi-straight lines, suggesting a dependence of $\beta_{I\mathrm{sc}}$ on I_{sc}, as was already observed in previous studies [11, 19]. Two theoretical curves with fixed values for $df_{\mathrm{c}}/dT_{\mathrm{c}}$ are plotted, visualizing the dependence of $\beta_{I\mathrm{sc}}$ with I_{sc} [see (D.5)]. No correlation is observed between the data and the theoretical curves, suggesting that cells with lower I_{sc} values could have larger $df_{\mathrm{c}}/dT_{\mathrm{c}}$, and thus larger $\beta_{I\mathrm{sc}}$.

The four ingots with different compensation levels exhibit different average $\beta_{I\mathrm{sc}}$ values, with the largest found for CL 1. Compensated mc-Si solar cells were shown to possess favorable $\beta_{I\mathrm{sc}}$ values compared to polysilicon cells [14,24,25]. In this paper, the ingot with

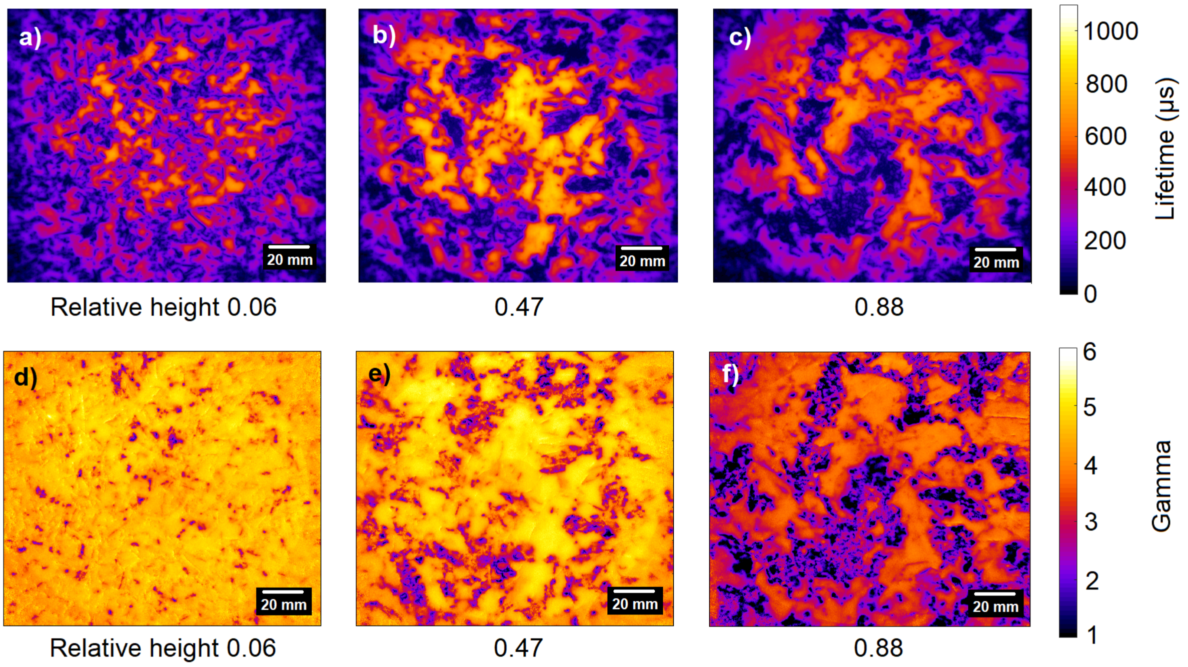


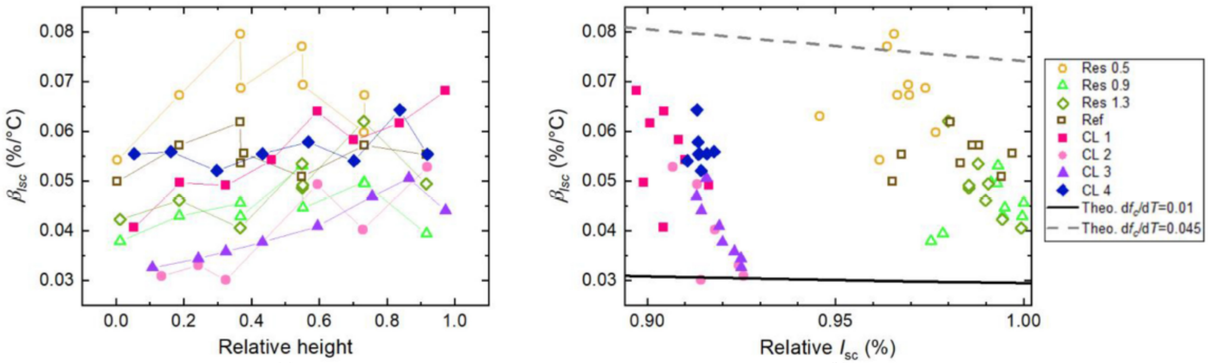
Figure D.3: Lifetime maps at 25 °C (a-c) and γ maps (d-f) of wafers from ingot CL 4 originating from different relative heights in the brick. The maps are obtained from PL imaging and are presented on the same color scale.

the lowest compensation levels (CL 1) shows the best temperature coefficients. Moreover, no distinct trend can be drawn between the different ingots. In conclusion, the compensation level does not have an impact on the temperature coefficients in this case.

The cells from ingot Res 0.5 show the largest $\beta_{I\mathrm{sc}}$ values and consequently (as a result of the sub-mentioned trend) the lowest I_{sc} values. It shows that lowering the bulk resistivity has a negative effect on the I_{sc} which turns out to be beneficial for the temperature coefficient. Several reasons could explain the decrease of I_{sc} such as free carrier absorption, or a less effective back surface field, or even an increased recombination velocity due to higher net doping.

C. Temperature Coefficient of the Fill Factor

The parameter β_{FF} depends heavily on the series resistance, as shown in (D.6). When investigating the dependence of this temperature coefficient with the relative height [see Fig. D.5(a)] we see that the Al-BSF cells with very similar bulk resistivities show very little variations. It is even more pronounced since these cells experienced relatively small variations in V_{oc} and FF, which explains why the data points for these ingots are highly condensed in Fig. D.5(b) and (c), where β_{FF} is plotted as a function of V_{oc} and FF, respectively. In addition, the Al-BSF cells have higher FF and lower V_{oc} values than the



(a) (b)

Figure D.4: $\beta_{I_{\mathrm{sc}}}$ as a function (a) of the relative height in the brick and (b) of the relative short-circuit current with two iso-$df_{\mathrm{c}}/dT_{\mathrm{c}}$ curves with values of 0.01 and 0.045, for the ingots defined in Table D.2.

PERC cells, which is explained by a reduced series resistance in the cell due to a simpler cell architecture.

On the contrary, the PERC cells show larger variations of V_{oc} and FF between the ingots. An increase of V_{oc} increases $\beta_{V_{\mathrm{oc}}}$ and FF_0, thus it increases β_{FF} [see (D.6)]. A lower bulk resistivity positively influences V_{oc}, which increases β_{FF}. Thus, the cells from ingot ESS 0.5 show the largest temperature coefficients, followed by ESS 0.9 and ESS 1.3. The reference ingot Ref exhibits lower values than ESS 1.3 even though the two ingots have similar resistivities. This seems to be the result of a slightly lower V_{oc}.

To study the isolated effect of the resistance on β_{FF}, the parameter φ is introduced, and it is defined as follows:

$$\varphi = \beta_{FF,\mathrm{exp}} - (1.02\, FF_0)\left(\beta_{V_{\mathrm{oc,exp}}} - 1/T_{\mathrm{c}}\right). \tag{D.9}$$

The experimental values of β_{FF} and $\beta_{V_{\mathrm{oc}}}$ were used to calculate φ. Meaning the series resistance term in (D.6) is the main part of this parameter, in addition to possible shunt resistance effects, which are not accounted for when calculating β_{FF}. This parameter is plotted against the cells' bulk resistivities in Fig. D.5(d). For the ingots with different resistivities (Res 0.5, 0.9, 1.3 and Ref), φ increases with decreasing bulk resistivity. Moreover, Al-BSF cells with similar bulk resistivities as PERC cells exhibit higher φ values, which is a direct sign of a lower series resistance for this cell architecture. In conclusion, a lower series resistance impacts positively β_{FF}, in accordance with previous results [26].

D. Temperature Coefficient of the Efficiency

The Al-BSF cells least sensitive to temperature variations are situated at the top of the ingot, as can be seen in Fig. D.6. This is explained by a decrease of the γ parameter

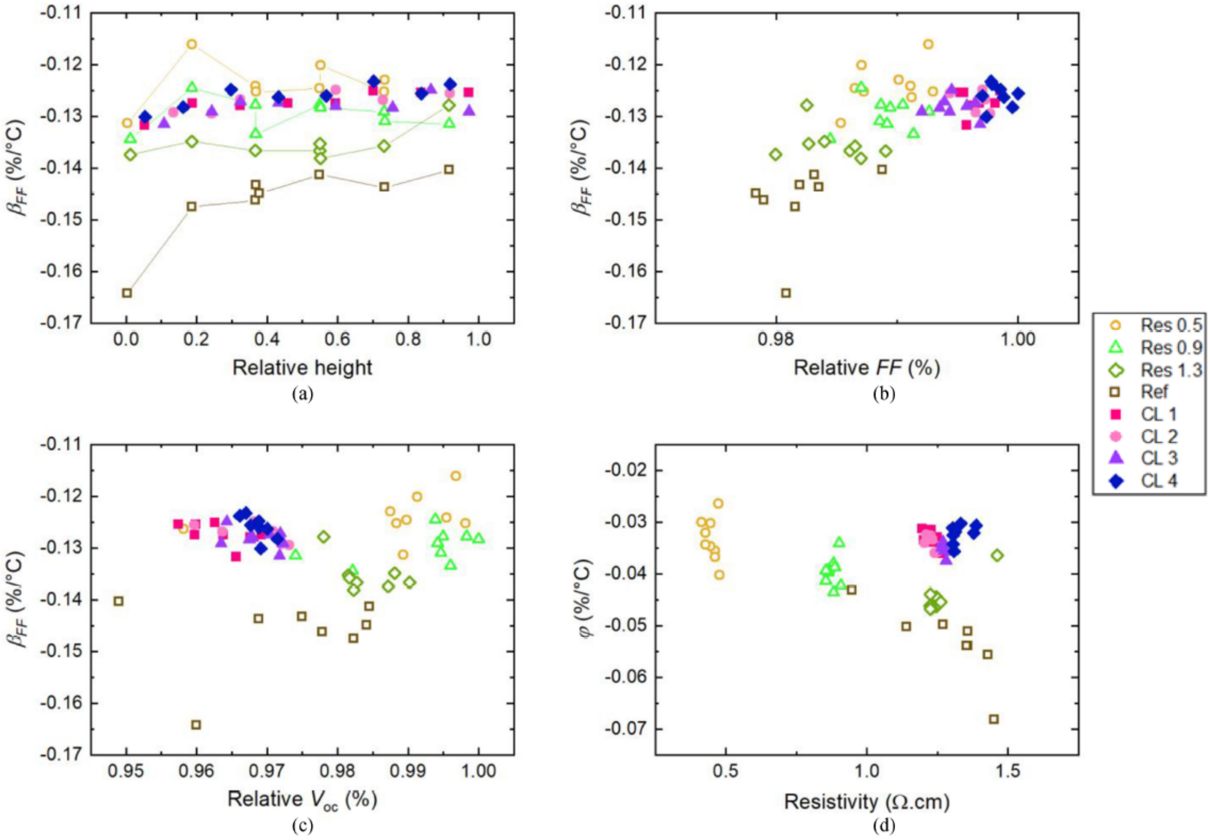


Figure D.5: β_{FF} as a function (a) of the relative height in the brick, (b) of the relative fill factor, and (c) of the relative open-circuit voltage. ϕ, as defined in Eq. D.9, as a function (d) of the bulk resistivity, calculated from the Scheil equation.

along the brick height, increasing $\beta_{V_{\mathrm{oc}}}$, and an increase of $\beta_{I\mathrm{sc}}$. No significant trend can be observed between the different ingots. Ingot CL 4 exhibits higher temperature coefficients for the three bottom cells, but the difference is not significant to draw any conclusion. This is confirmed in Fig. D.7, which shows β_{η} as a function of the compensation level [defined in (D.8)] for these cells. It can be pointed out that the compensation levels are not particularly high for our material (lower than 2 at the bottom of CL 4), yet these levels are representative of what is obtained when using this compensated feedstock (Elkem Solar Silicon). In addition, these cells have lower efficiencies than state-of-the-art cells. An effect of the compensation level on the temperature coefficient may be observed with high-performance devices.

The PERC cells in Fig. D.6 exhibit the smallest temperature sensitivities around the middle of the brick, due to $\beta_{V_{\mathrm{oc}}}$ which is also at its highest at the same position.

It can be observed that both cell types show relatively similar temperature coefficients even though PERC cells have significantly higher V_{oc} values. Al-BSF cells with lower series resistance experienced an improved β_{FF} which counterbalances the advantageous

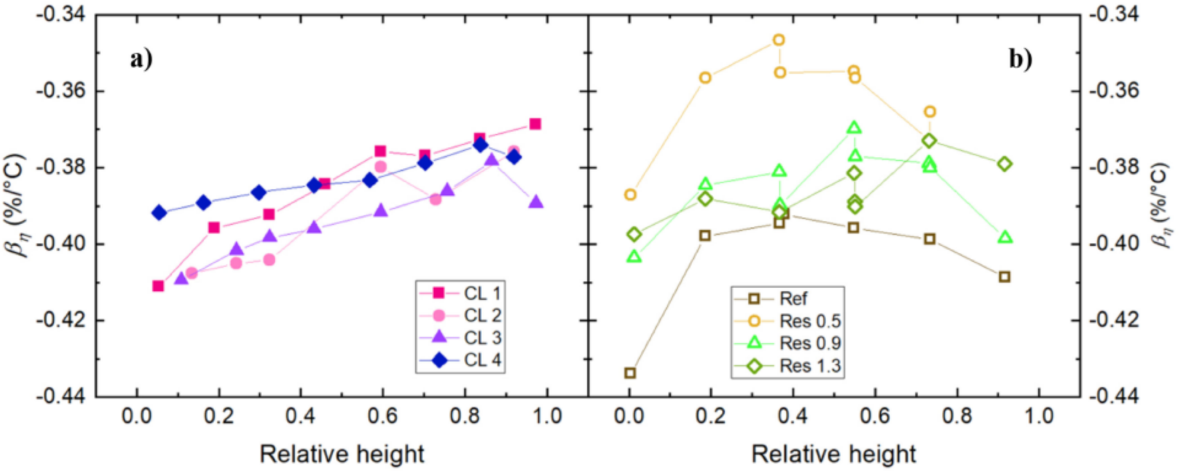


Figure D.6: β_η as a function of the relative height in the brick (a) for the Al-BSF cells and (b) for the PERC cells.

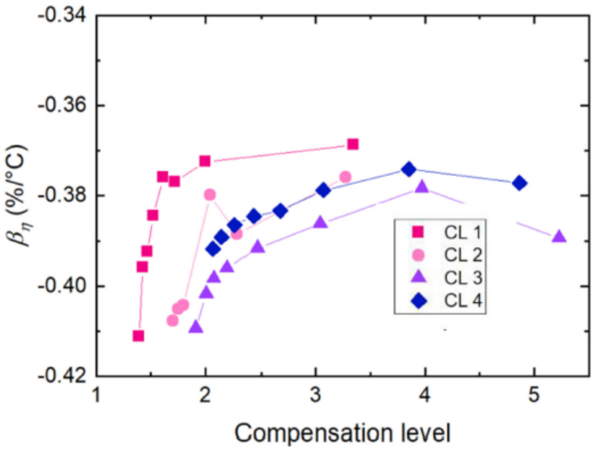


Figure D.7: β_η as a function of the compensation level for the Al-BSF cells.

high V_{oc} and thus $\beta_{V_{\mathrm{oc}}}$ of the PERC cells.

Ingot Res 0.5, which has the smallest bulk resistivity, shows the highest temperature coefficients along the whole brick. Advantageous $\beta_{I\mathrm{sc}}$ and β_{FF} values for this ingot explain the final reduced temperature sensitivity for this ingot. However, the average efficiency for this ingot is smaller than for the two other compensated ingots (Res 0.9 and 1.3). To examine if the lower efficiency at STC is counterbalanced by the reduced temperature sensitivity, Fig. D.8 shows the efficiencies at 25 and 70 °C for the cells in Res 0.5 and Res 1.3. We observe that the mean efficiency of the cells in the low-resistivity ingot is slightly higher than the one for Res 1.3. This means that solar cells made from ingot Res 0.5 will have higher power outputs at high temperatures than cells from Res 1.3. The crossing temperature for the average efficiencies of the two ingots is found to be 45 °C which means that at locations where the operating temperature of modules exceeds

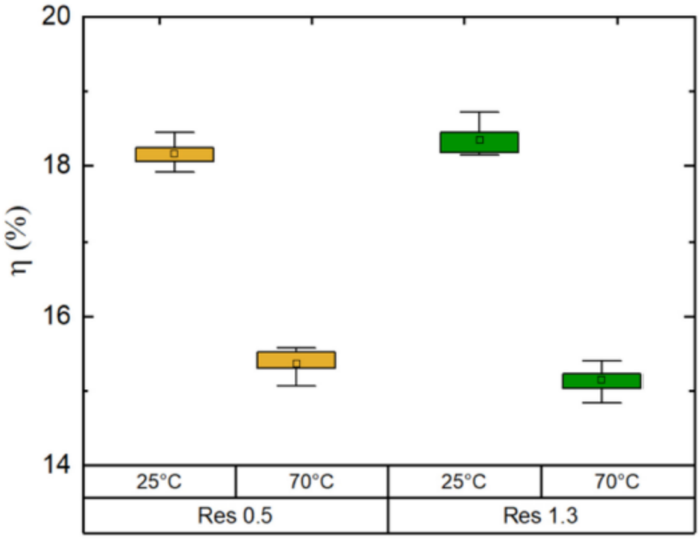


Figure D.8: Box plot of the measured efficiencies of the cells from RES 0.5 and Res 1.3 at STC (25 °C) and 70 °C.

the crossing temperature, the Res 0.5 cells will produce more energy [27]. For the same ingots but a different cell architecture (passivated emitter rear totally diffused cell), the opposite conclusion was reached, which shows the importance of the cell architecture for this technique [28].

D.V. General Discussion

The compensation level is not observed to affect the temperature coefficients at low levels. A problem of many studies is that compensated silicon was obtained by using UMG-Si which has large quality variations between producers. Comparing temperature coefficients of solar cells with large efficiency discrepancies should not be done. In this paper, various blend-in-ratios of an UMG-Si feedstock (Elkem Solar Silicon) were used without changing the efficiency (see Table D.2). This proves the relatively high quality of the used feedstock and enabled us to investigate only the effect of the compensation level without perturbing impurities. Dupré [26] predicted that when UMG-Si would achieve better material and chemical qualities, the gap between the temperature coefficients of solar cells made with this silicon and standard solar cells would vanish. Our study points to the same conclusion.

A previous study tried to engineer solar cells for hot climates by changing the bulk resistivity without success because of a too large drop in efficiency at low resistivities [28]. Here we have successfully managed this method by using PERC cells instead of PERCT cells. This was possible because PERC cells perform better than PERCT cells at low resistivities [29].

D.VI. Conclusion

In this paper, we have shown that dislocation clusters affect positively the temperature coefficient of the open-circuit voltage by decreasing the γ parameter. In addition, we have demonstrated that the compensation level does not influence the temperature sensitivity. Finally, we have shown that decreasing the targeted resistivity of an ingot can be beneficial for the solar cells' performances at high temperatures, depending on the cell architecture.

Acknowledgment

The authors would like to acknowledge the Australian Government through the Australian Renewable Energy Agency (ARENA, Project 2017/RNDO01).

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Paper E

How gettering affects the temperature sensitivity of the implied open circuit voltage of multicrystalline silicon wafers

Published as:
S. T. Kristensen, S. Nie, C. Berthod, R. Strandberg, J. O. Odden, and Z. Hameiri, "How gettering affects the temperature sensitivity of the implied open circuit voltage of multicrystalline silicon wafers", in: *Proceedings of the 46th IEEE Photovoltaic Specialists Conference*, pp. 0061-0067, 2019.
doi: 10.1109/PVSC40753.2019.8980880

How gettering affects the temperature sensitivity of the implied open circuit voltage of multicrystalline silicon wafers

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Abstract **— The temperature sensitivity of the open circuit voltage of a solar cell is mainly driven by changes in the intrinsic carrier concentration, but also by the temperature dependence of the limiting recombination mechanisms in the cell. This paper investigates the influence of recombination through metallic impurities on the temperature sensitivity of multicrystalline silicon wafers. Spatially resolved temperature dependent analysis is performed to evaluate the temperature sensitivity of wafers from different brick positions before and after being subjected to phosphorus diffusion gettering. Local spatial analysis is performed on intra-grain areas, dislocation clusters and grain boundaries. Large variations in temperature sensitivity is observed across the wafers both before and after gettering. The spatially resolved γ parameter is found to change with gettering, indicating that the gettering process alters the balance between different recombination mechanisms in the material. Features with low temperature sensitivity are observed across the wafers and correlated with dislocation clusters. The locations of these areas remain unchanged by the gettering process, suggesting that the cause for the low temperature sen-**

sitivity is not removed. Gettering is observed to have a complex effect on the temperature sensitivity of the dislocation clusters depending on the wafer position in the brick, with dislocations from the top wafer exhibiting lowest temperature sensitivity both before and after gettering.

E.I. Introduction

Silicon solar cells are usually characterized and optimized under standard test conditions (STC), defined as a global standard solar spectrum AM1.5G, an irradiance of 1000 W/m^2 and a cell temperature of 25 °C [1]. However, real operating temperatures can differ considerably from STC [2]. Temperature significantly affects the characteristics of photovoltaic (PV) devices, as has been known for decades [2–5]. Understanding the thermal behavior of a PV device under non-STC is therefore essential to accurately estimate the production of PV power plants and to optimize PV devices for different climatic conditions.

The thermal behavior of a solar cell is primarily determined by the temperature sensitivity of the open circuit voltage (V_{oc}) which accounts for approximately $80-90\,\%$ of the total temperature sensitivity of a reasonably good solar cell [6]. The V_{oc} generally decreases with increasing temperature due to a reduction of the band gap energy (E_{g}) which consequently increases the intrinsic carrier concentration (n_i) and the internal carrier recombination [6–8]. The temperature sensitivity of V_{oc} is usually quantified using the temperature coefficient ($\beta_{V_{\mathrm{oc}}}$). To the first-order approximation, and in absolute form, it is given as [9]

$$\beta_{V_{\mathrm{oc}}} = \frac{dV_{\mathrm{oc}}}{dT_{\mathrm{c}}} = -\frac{E_{\mathrm{g0}}/q - V_{\mathrm{oc}} + \gamma k T_{\mathrm{c}}/q}{T_{\mathrm{c}}}, \tag{E.1}$$

where E_{g0} denotes the semiconductor bandgap energy extrapolated to 0 K, q is the elementary charge, k is the Boltzmann constant, and T_{c} is the cell temperature. The parameter γ includes the temperature dependence of several parameters determining the dark saturation current, J_0, and therefore contains information about the dominant recombination mechanism in the material. According to Ref. [4], γ usually takes values between 1 and 4.

Eq. (E.1) predicts an approximately linear relationship between $\beta_{V_{\mathrm{oc}}}$ and the V_{oc} of the cell, implying that a cell with a high V_{oc} will have the inherent advantage of reduced temperature sensitivity. In addition, $\beta_{V_{\mathrm{oc}}}$ can be significantly influenced by the last term in Eq. (E.1) containing the parameter γ [2].

Previously, Berthod *et al.* studied the relationship between global $\beta_{V_{\mathrm{oc}}}$ values and brick height of compensated multicrystalline silicon (mc-Si) solar cells [10]. The authors found lower temperature sensitivity for cells from the top of the bricks despite low V_{oc} values observed for these cells. They suggested that it could be caused by an increased concentration of different crystal defects, typically found in the top of mc-Si ingots as a result of the directional solidification process. Recently, Eberle *et al.* reported increased temperature sensitivity of V_{oc} in contaminated regions of mc-Si cells but reduced temperature sensitivity for areas containing dislocation clusters [11]. This was further investigated by Eberle *et al.* in Ref. [12], reporting reduced temperature sensitivity of dislocation clusters of mc-Si wafers and cells. The authors suggested that it could be caused by the presence of impurities in the dislocation areas and thus Shockley-Read-Hall (SRH) recombination. These findings illustrate the impact of crystallographic defects on the temperature sensitivity of V_{oc} of mc-Si wafers and cells and highlight the importance of further studies to evaluate the varying influence of different defect types. Moreover, it shows the necessity of spatially resolved analysis for detailed investigation of the temperature sensitivity.

This work examines the influence of metallic impurities on the thermal behavior of V_{oc} of mc-Si wafers. Metallic impurities are detrimental limiting defects in *p*-type mc-Si in addition to dislocation clusters [13–15] and knowledge about their impact on the temperature sensitivity is therefore important. This is investigated by spatially evaluating the temperature sensitivity of mc-Si wafers before and after being subjected to phosphorus diffusion gettering (PDG), serving the purpose of altering the concentration of metallic impurities across the wafers [16].

E.II. Experimental Method

A. Sample Preparation

Wafers were cut from a high-performance compensated *p*-type mc-Si ingot tri-doped with boron, gallium and phosphorus. The ingot was made from a blend of compensated silicon [Elkem Solar Silicon® (ESS®)] and polysilicon with a blend-in-ratio of 70 % ESS® and resistivity of 0.9 Ω·cm. Eight 6" wafers were chosen from different positions in a central brick.

The wafers were processed in two steps: Step 1 (referred to as *ungettered*): The as-sawn wafers received saw damage etching, cleaning [17], and passivation with 75 nm silicon nitride (SiN_x) using an industrial plasma-enhanced chemical vapor deposition (PECVD) system (MAiA, Meyer Burger) at a deposition temperature of 400 °C [18]. Step 2 (referred to as *gettered*): The passivation from Step 1 was removed using hydrofluoric (HF) acid followed by a second clean. A conventional PDG [16] was performed by subjecting the wafers to a 45 min POCl_3 diffusion treatment with peak temperature of 850 °C resulting in a sheet resistance of 40 Ω·cm [19, 20]. The surface gettering layer was then removed by alkali etching and the wafers were re-passivated using an identical SiN_x process as in Step 1. The wafers were fully characterized after Step 1 and after Step 2.

B. Characterization and Analysis

The wafers were characterized using our novel temperature dependent photoluminescence (PL) imaging system [21], where PL images were acquired at 25 °C and 70 °C enabling mapping of the effective carrier lifetime (τ_{eff}), implied open circuit voltage (iV_{oc}), the temperature coefficient of iV_{oc} ($\beta_{iV_{\text{oc}}}$), and γ. The PL images were obtained at a photon flux of $1.2 \cdot 10^{17}\,\text{cm}^{-2}\text{s}^{-1}$, corresponding to an illumination intensity of approximately 0.5 Sun.

The PL images of the ungettered wafers were calibrated based on a temperature dependent photo-conductance (PC) signal measured on a region of the wafer during PL image acquisition. A detailed description of the calibration procedure can be found in Ref. [21]. The PL images of the gettered wafers were calibrated using a temperature dependent front detection PL-based system [22] to account for trapping observed for these wafers at relevant injection levels. The calibration was performed using a temperature and injection dependent τ_{eff} curve obtained by simultaneously measuring a PC signal on the wafer and collecting a PL signal emitted from the wafer. The τ_{eff} curve obtained from the quasi-steady-state (QSS) PL signal was then matched with the PC-based τ_{eff} curve at high injection. The wafers before and after gettering were therefore both calibrated using PC-based measurements.

From the calibrated PL images, absolute $\beta_{iV_{\text{oc}}}$ maps were obtained by applying to each pixel the following operation:

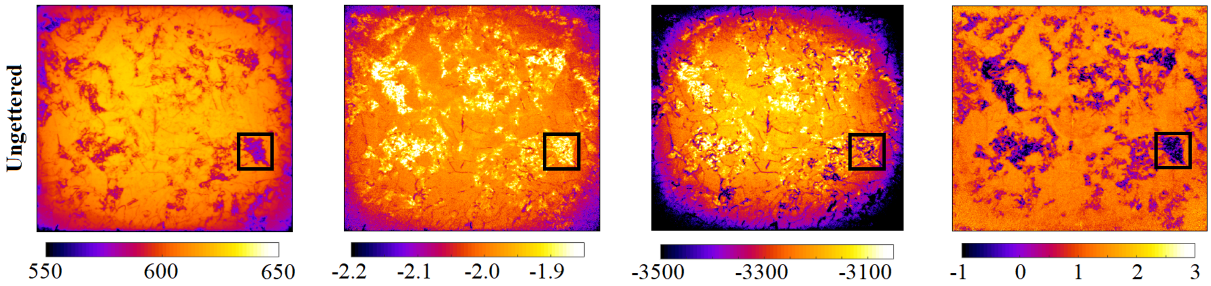
$$\beta_{iV_{\text{oc,abs},xy}} = \frac{iV_{\text{oc},T2,xy} - iV_{\text{oc},T1,xy}}{T_2 - T_1}. \tag{E.2}$$

Relative $\beta_{iV_{\text{oc}}}$ maps were obtained by normalizing each pixel with the local iV_{oc} at 25 °C. Finally, maps of the γ parameter were created by applying Eq. (E.1) to each pixel. Note that a circular heat stage (Sinton WCT-120TS) was used for imaging, causing an inhomogeneous wafer temperature outside of the heat stage [a circular feature can be observed in Fig. E.1(c)]. Therefore, only the area of the wafers with uniform temperature was used for further analysis.

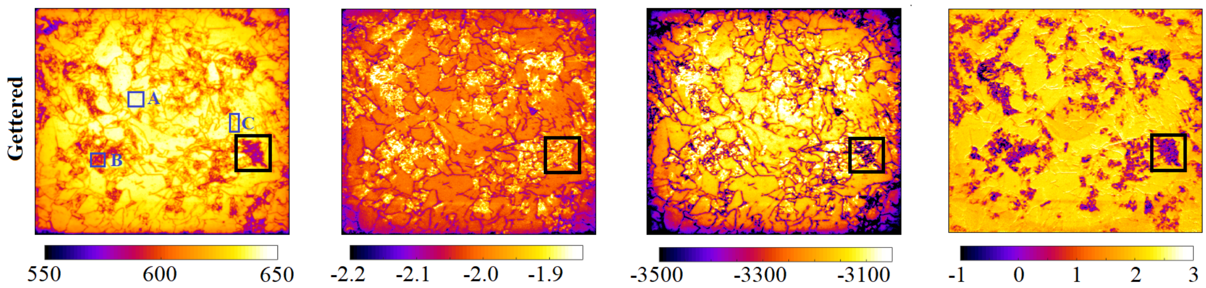
E.III. Results and Discussion

A. Effect of Gettering on the Temperature Sensitivity

A wafer from the top of the brick is chosen for in-depth analysis since it typically contains a higher impurity concentration compared to wafers from the middle of the brick and thus may be more effectively gettered [23, 24]. Figs. E.1(a) and (e) show images of iV_{oc} at 25 °C of a wafer from the top of the brick before and after gettering, respectively. Dislocations can be identified as dark clusters in the images where recombination active



(a) iV_{oc} (mV) (b) $\beta_{iV\mathrm{oc}}$ (mV K^{-1}) (c) $\beta_{iV\mathrm{oc}}$ (ppm K^{-1}) (d) γ



(e) iV_{oc} (mV) (f) $\beta_{iV\mathrm{oc}}$ (mV K^{-1}) (g) $\beta_{iV\mathrm{oc}}$ (ppm K^{-1}) (h) γ

Figure E.1: Images of iV_{oc} at 25 °C, absolute and relative $\beta_{iV_{\mathrm{oc}}}$ and γ of a wafer from the top of the brick before (a-d) and after (e-h) gettering. The black square marks a dislocation cluster of special interest. The letters A-C mark areas on the wafer of different crystal quality: (A) An intra-grain area, (B) a dislocation cluster, and (C) a grain boundary.

grain boundaries appear as dark lines. Comparing the two images, the gettering process is found to improve the quality of the intra-grain areas but to increase the recombination activity of the grain boundaries, consistent with results previously reported [23, 25]. The improvement of the intra-grain areas results from the ability of the gettering process to reduce the concentration of detrimental metallic impurities in these areas [16]. The activation of the grain boundaries has been suggested to result from metal decoration of the structures during the gettering process causing a change in recombination behavior [26–29]. It seems that the dislocation clusters are recombination active both before and after gettering.

Figs. E.1(b) and (f) show images of the absolute $\beta_{iV_{\mathrm{oc}}}$ before and after gettering, respectively. Large variations are found across the wafer both before and after PDG highlighting the importance of spatially resolved analysis. The temperature sensitivity of intra-grain areas does not seem to be significantly affected by the gettering process for this wafer. In contrast, the grain boundaries show a clear increase in temperature sensitivity after gettering, consistent with the expected correlation between material quality and $\beta_{iV_{\mathrm{oc}}}$ as predicted from Eq. (E.1). One interesting observation is that the areas across the wafer exhibiting low temperature sensitivity remain unchanged by the gettering process. Comparing Figs. E.1(b) and (f) to Figs. E.1(a) and (e), the low temperature sensitivity regions seem to be correlated with dislocation clusters: An unexpected observation since Eq. (E.1) predicts high temperature sensitivity when the iV_{oc} is low. This finding is in correlation with results reported by other recent studies [11, 12, 21, 30] and has been suggested to result from the presence of impurity atoms [12]. It should be noted that some dislocation clusters of wafers from other brick positions were observed to exhibit high absolute temperature sensitivity, however, all features with low temperature sensitivity could be correlated with dislocation clusters.

Similar trends can be found in Figs. E.1(c) and (g) showing images of the relative $\beta_{iV_{\mathrm{oc}}}$ before and after gettering, respectively. However, because the relative $\beta_{iV_{\mathrm{oc}}}$ is more strongly dependent on iV_{oc} compared to the absolute $\beta_{iV_{\mathrm{oc}}}$, intra-grain areas show a relatively larger improvement in temperature sensitivity after gettering compared to Fig. E.1(f). This effect also causes the grain boundaries to exhibit a more negative relative $\beta_{iV_{\mathrm{oc}}}$ after gettering. A region of interest (ROI) is identified on the wafer (black square), containing a dislocation cluster that shows low absolute temperature sensitivity (less negative absolute $\beta_{iV_{\mathrm{oc}}}$) but high relative temperature sensitivity (more negative relative $\beta_{iV_{\mathrm{oc}}}$). This illustrates the importance of the chosen representation of the temperature coefficient and how it can affect the conclusion drawn from the data if proper care is not taken.

Figs. E.1(d) and (h) show images of γ before and after gettering. Large variations are found across the wafer both before and after gettering, indicating that different recombination mechanisms dominate different regions of the wafer. Features with low (and in some cases even negative) γ values can be observed across the wafer and seem to be correlated with dislocation clusters by comparing with Figs. E.1(a) and (e). The locations of these features on the wafer remain the same before and after gettering. The gettering process is found to increase γ in most areas across the wafer.

To investigate the correlation between temperature sensitivity and crystal quality, Figs. E.2(a) and (b) show the absolute $\beta_{iV_{\mathrm{oc}}}$ and iV_{oc} of each pixel on the PL image of the wafer before and after gettering, respectively. Comparing the two figures, gettering is found to broaden the distribution towards higher iV_{oc} and more negative $\beta_{iV_{\mathrm{oc}}}$ suggesting that the gettering process generally improves the quality of parts of the wafer but increases the temperature sensitivity. Note that the medium quality regions exhibit both the lowest and the highest temperature sensitivity.

B. Temperature Sensitivity of Intra-grain Areas, Dislocations, and Grain Boundaries

To further investigate how gettering affects the temperature sensitivity of areas of different crystal quality, local spatial analysis is performed. Three different regions of the wafer

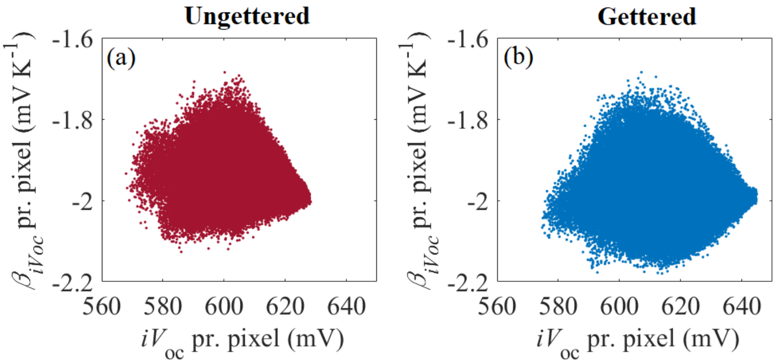


Figure E.2: Absolute $\beta_{iV_{\mathrm{oc}}}$ as a function of iV_{oc} for each pixel before and after gettering of a wafer from the top of the brick.

Table E.1: Crystal quality and average absolute $\beta_{iV_{\mathrm{oc}}}$ and γ before and after gettering for different regions on a top wafer.

Region	Crystal quality	$\beta_{iV_{\mathrm{oc}}}$(unget.) (mV K^{-1})	γ (unget.)	$\beta_{iV_{\mathrm{oc}}}$(gettered) (mV K^{-1})	γ (gettered)
A	Intra-grain	-1.98	1.50	-2.00	2.26
B	Dislocation	-1.91	-0.243	-1.95	0.313
C	Grain boundary	-1.98	1.29	-2.02	2.18
-	Global value	-1.96	0.840	-1.98	1.40

are examined, marked in Fig. E.1(e) with the letters A-C, indicating (A) an intra-grain area, (B) a dislocation cluster, and (C) an area containing grain boundaries.

Figs. E.3(a), (d) and (g), show the absolute $\beta_{iV_{\mathrm{oc}}}$ as a function of iV_{oc} for each pixel before and after gettering for Regions A-C. Corresponding histograms of absolute $\beta_{iV_{\mathrm{oc}}}$ are presented in Figs. E.3(b), (e) and (h), illustrating more clearly the distribution of the temperature sensitivity. Straight lines are inserted in the histograms indicating the average values of the distributions. An overview of the average values can be found in Tab. E.1.

From Fig. E.3(a), the intra-grain region is found to shift towards higher values of iV_{oc} after gettering, indicating a successful gettering of impurities from this region. Note that a similar behavior was observed for most intra-grain regions. The distribution of $\beta_{iV_{\mathrm{oc}}}$ [Figs. E.3(a) and (b)] is narrow and show a slight shift towards more negative $\beta_{iV_{\mathrm{oc}}}$ values, from an average value of $-1.98\,\mathrm{mV\,K^{-1}}$ to $-2.00\,\mathrm{mV\,K^{-1}}$. This suggests that removal of impurities initially present in this area did not have a significant effect on the temperature sensitivity.

From Figs. E.3(d) and (e), the dislocation cluster exhibits a broad distribution of $\beta_{iV_{\mathrm{oc}}}$ both before and after gettering and the gettering process is found to shift the distribution

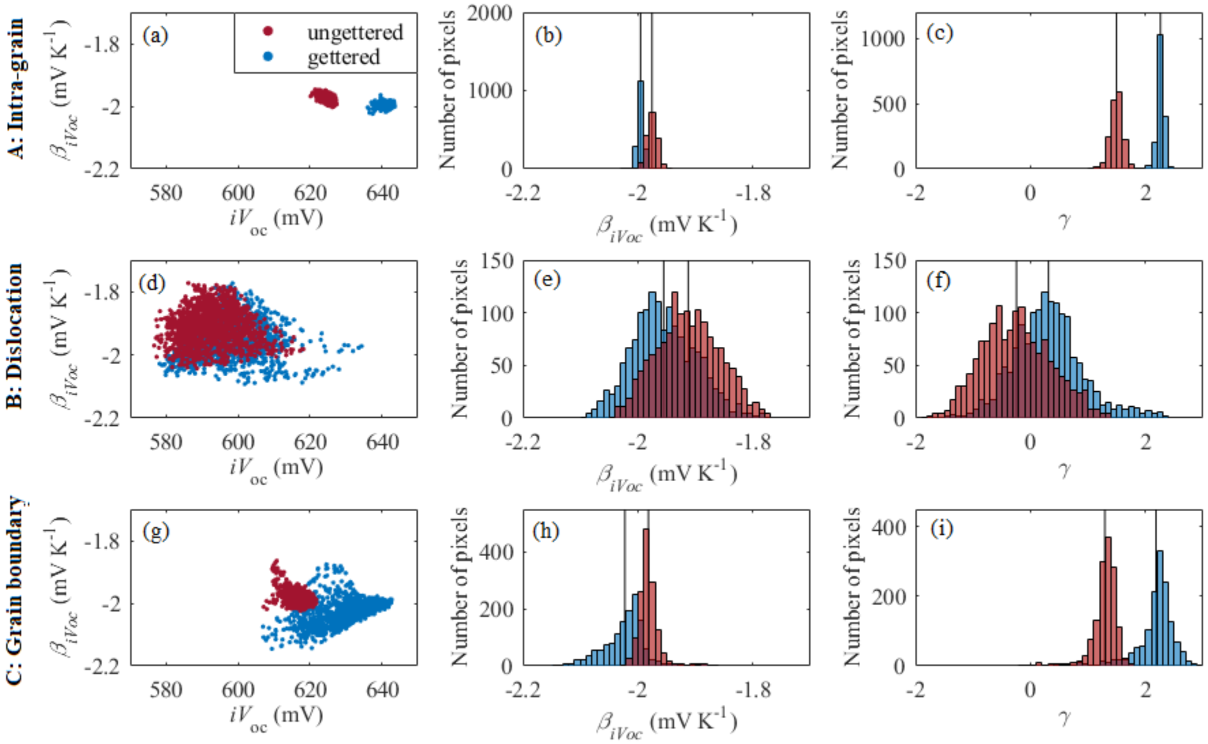


Figure E.3: Absolute $\beta_{iV_{\rm oc}}$ as a function of $iV_{\rm oc}$ for each pixel; and distribution of absolute $\beta_{iV_{\rm oc}}$, and γ in (A) an intra-grain area (a)-(c), (B) dislocation cluster (d)-(f), and (C) grain boundaries (g)-(i) before and after gettering. Straight lines indicate the average values of the $\beta_{iV_{\rm oc}}$ and γ distributions. The locations on the wafer are defined in Fig. E.1(e). Note that the number of pixels differ for the different regions.

to more negative $\beta_{iV_{\rm oc}}$ values. Note the tail of pixels in Fig. E.3(d) which is shifted towards higher $iV_{\rm oc}$ values after gettering. This is likely to be caused by intra-grain areas that were included in this ROI. The dislocation cluster exhibits a wide range of $\beta_{iV_{\rm oc}}$ including regions with the lowest $\beta_{iV_{\rm oc}}$. On average, the temperature sensitivity of this area is found to be the lowest compared to the other two ROIs both before and after gettering (see Tab. E.1).

Turning our attention to the grain boundary area, Figs. E.3(g) and (h) illustrate that the gettering process broadens the distribution of both $iV_{\rm oc}$ and $\beta_{iV_{\rm oc}}$. Furthermore, gettering is found to shift most of the pixels towards more negative $\beta_{iV_{\rm oc}}$ values. The large spread in pixel behavior is likely to arise from the combination of the actual grain boundary and near grain boundary areas which are included in the analyzed region. A long tail appears towards negative $\beta_{iV_{\rm oc}}$ values after gettering, likely to represent the actual grain boundary region. This is consistent with the observations made from the PL images [see Figs. E.1(b) and (f)].

When comparing the average $\beta_{iV_{\rm oc}}$ values of the Regions A-C (see Tab. E.1), the intra-grain area and grain boundary are found to exhibit very similar behavior. However, when investigating the corresponding distributions in these areas, large differences are found. The grain boundaries are found to exhibit a significantly broader peak towards negative $\beta_{iV_{\mathrm{oc}}}$ values, and the dislocation cluster consists of a tail both with low and high temperature sensitivity. The dislocation clusters are found to exhibit the lowest temperature sensitivity of the three areas both before and after gettering, indicating that the cause for the low temperature sensitivity is not removed by the gettering process. Several other regions of intra-grain areas, dislocations, and grain boundaries were examined on this wafer and were found to show similar distributions and changes in $\beta_{iV_{\mathrm{oc}}}$ with gettering, demonstrating that the selected regions can be considered representative of the different crystal areas across this wafer.

The distributions of γ parameters before and after gettering for the Regions A-C are presented in Figs. E.3(c), (f) and (i). Gettering is observed to shift the distributions to higher γ values for all areas indicating that the gettering process alters the balance between different recombination mechanisms in the material. A relatively large number of pixels in the dislocation cluster display negative γ values. The physical interpretation of this has not yet been determined but has been observed elsewhere in the literature [11, 31].

C. Influence of Brick Position

Multicrystalline silicon ingots typically contain large variations in concentration and composition of crystallographic defects along the ingot as a consequence of the quality of the feedstock and the directional solidification process [24, 32]. This can have a significant impact on the recombination activity of different crystal defects in the as-grown state and how they respond to gettering (see Refs. [23, 26]). It is therefore natural to investigate if this has an impact on the temperature sensitivity of different crystal defects, depending on the original position of the wafer in the brick. An example of this is given in Figs. E.4(a)-(d) which show the distribution of $\beta_{iV_{\mathrm{oc}}}$ of dislocation clusters of four wafers from different relative brick heights of 0.05, 0.34, 0.47, and 0.89, respectively. Average values of the distributions are marked on the figures. Broad distributions are observed for all dislocation clusters, and all distributions are found to shift towards more negative $\beta_{iV_{\mathrm{oc}}}$ values after gettering except for the bottom wafer (relative height 0.05) which exhibits an opposite behavior. This illustrates how brick position can influence the temperature sensitivity and gettering response of different crystal defects.

Comparing the dislocation clusters from the bottom and the top wafers (relative heights 0.05 and 0.89, respectively), the iV_{oc} improves significantly more with gettering for the bottom wafer (from 586 mV to 604 mV) compared to the top wafer (from 597 mV

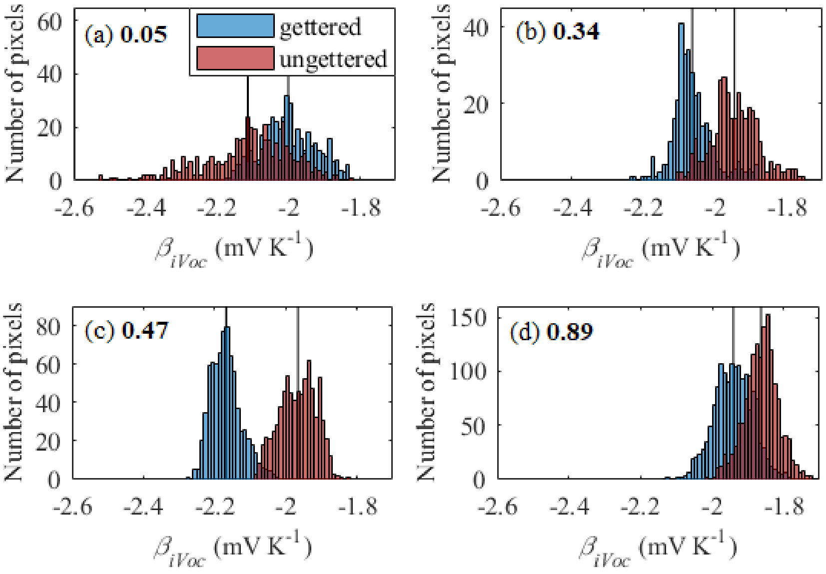


Figure E.4: Distribution of $\beta_{iV_{\mathrm{oc}}}$ values of dislocation clusters before and after gettering from four wafers from different brick positions corresponding to 0.05 (a), 0.34 (b), 0.47 (c), and 0.89 (d) of the full brick height. Average values of the distributions are marked with a straight line.

to 601 mV). This indicates that the gettering process was more successful in removing impurities from the dislocation cluster from the bottom wafer, improving the overall performance and therefore the temperature sensitivity. However, despite of comparable iV_{oc} values after gettering, the dislocation in the top wafer still shows the lowest temperature sensitivity compared to the other wafers. Other dislocations on the top wafer were examined and found to show similar behavior. This suggests that dislocation clusters on wafers from the top of a brick might have different properties which could be beneficial at elevated temperatures.

E.IV. Summary

In this study, the temperature sensitivity of the iV_{oc} of mc-Si wafers was investigated and the influence of gettering was evaluated. Large variations in $\beta_{iV_{\mathrm{oc}}}$ was observed across the wafers both before and after gettering. Gettering was found to change the γ parameter across the wafer, indicating that the process alters the balance between different recombination mechanisms in the material.

Local spatial analysis was performed to assess the temperature sensitivity of intra-grain areas, dislocation clusters, and grain boundaries. We observed that the gettering process increases the absolute temperature sensitivity of grain boundaries but does not significantly affect the intra-grain areas. Features with low absolute temperature sensitivity were identified across the wafers and could be correlated with dislocation clusters. The location of these areas remained unchanged by the gettering process, indicating that the cause for the low temperature sensitivity was not removed by the gettering process.

Gettering was observed to have a complex effect on the temperature sensitivity of the dislocation clusters depending on the wafer position in the brick. Dislocations from the top wafer exhibited the lowest temperature sensitivity both before and after gettering, suggesting that these dislocation clusters might have different properties which could be beneficial at elevated temperatures.

Acknowledgments

This work was supported by the Australian Government through Australian Renewable Energy Agency [ARENA; project 2017/RND001]. The views expressed herein are not necessarily the views of the Australian Government, and the Australian Government does not accept responsibility for any information or advice contained herein.

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Paper F

Photoluminescence-based spatially resolved temperature coefficient maps of silicon wafers and solar cells

Published as:
S. Nie, **S. T. Kristensen**, A. Gu, R. L. Chin, T. Trupke, and Z. Hameiri, "Photoluminescence-based spatially resolved temperature coefficient maps of silicon wafers and solar cells", *IEEE Journal of Photovoltaics*, vol. 10, no. 2, pp. 585-594, 2019.
doi: 10.1109/JPHOTOV.2019.2956261

Photoluminescence-based spatially resolved temperature coefficient maps of silicon wafers and solar cells

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Abstract — **In this paper, we present a method to obtain open circuit voltage images of silicon wafers and cells at different temperatures. The proposed method is then demonstrated by investigating the temperature coefficients of various regions across multi-crystalline silicon wafers and cells from different heights of two bricks with different dislocation densities. Interestingly, both low and high temperature coefficients are found in dislocated regions on the wafers. A large spread of temperature coefficient is observed at regions with similar performance at 298 K. Reduced temperature sensitivity is found to be correlated with increasing brick height and is exhibited by both wafers and cells. This may indicate that cells made from the top of the brick, although having higher defect concentration, actually suffer relatively less degradation in performance at higher temperatures.**

F.I. Introduction

Multi-crystalline silicon (mc-Si) solar cells have dominated the photovoltaic (PV) market over the past decade [1]. Similar to other commercialised solar cells, mc-Si solar cells are tested and optimised under standard test conditions (STC): A standard solar spectrum AM 1.5G, an irradiance of 1000 W/m^2 and a temperature of 298 K [2]. However, in the field, solar cell operating temperatures often deviate significantly from STC [3]. In order to allow PV users to accurately predict energy production and PV companies to optimise their cells for non-STC, temperature coefficients (TC), which quantify the impact of temperature on the electrical properties of the solar cells, are of particular importance.

It has long been known that temperature has a significant impact on the performance of silicon solar cells [4–12]. This is mainly due to the temperature dependence of the band-gap energy (E_g) [11]. Silicon features a reduction of E_g with increasing temperature, which causes an increased short-circuit current density (due to higher absorption) and a reduced open-circuit voltage V_OC [due to increasing intrinsic carrier concentration (n_i)] [5,13]. Green stated that the electron-hole concentration product, which depends on the type and magnitude of the recombination processes, is the key parameter determining V_OC, and thus, the temperature dependence of silicon solar cells [7]. For silicon solar cells, the temperature sensitivity of the efficiency mainly arises from the variation of V_OC with temperature [7]; understanding the thermal behavior of V_OC is therefore of high importance.

The absolute TC of the V_OC can be expressed as [5]

$$\mathrm{TC}\left(V_\mathrm{OC}\right)=\frac{dV_\mathrm{OC}}{dT}=-\frac{\frac{E_\mathrm{g0}}{q}-V_\mathrm{OC}+\frac{\gamma kT}{q}}{T}, \tag{F.1}$$

where E_g0 is the band gap energy of the semiconductor material extrapolated to 0 K, q is the elementary charge, k is the Boltzmann constant, T is the temperature, and γ represents the temperature dependences of several parameters determining the diode saturation current density J_0 [5,12]. The parameter γ also contains information regarding the dominant recombination mechanisms in the material [12]. Eq. (F.1) predicts a reduction in the absolute temperature sensitivity of V_OC with increasing V_OC. Moreover, it predicts an approximately linear reduction of V_OC with increasing temperature over a limited temperature range [7,12].

The temperature dependence of solar cells is normally reported as an average value for the entire cell [4,8,9,11,14,15]. This value is useful for the analysis of several factors that contribute to temperature dependence variations between different solar cells. For example, by combining experiment and simulation, Steinkemper *et al.* suggested that the temperature dependence of their investigated solar cells mainly originates from extrinsic recombination or surface recombination [11]. The study of Berthod *et al.* into TCs of compensated mc-Si solar cells identified variations in TCs for different cell positions along the bricks, with variations between aluminium back surface field (Al-BSF) and passivated emitter rear contact (PERC) cells due to differences in recombination mechanisms between the two cell structures [15].

There has been growing, but as-yet limited, research into the spatially resolved temperature dependence across wafers and solar cells [16–18]. Existing studies show a large variation in the temperature sensitivity across wafers and cells. Eberle *et al.* have shown increased temperature sensitivity, particularly for V_{OC}, at cell areas with a high concentration of impurities, such as the edge of the cells [17]. More recently, Eberle *et al.* conducted an in-depth investigation into the local temperature-dependent behaviour of mc-Si wafers and cells [18]. They identified a reduction in temperature sensitivity of V_{OC} in regions containing dislocation clusters. The investigation into the potential causes highlights the involvement of impurities, potentially leading to Shockley-Read-Hall (SRH) recombination [19, 20], which leads to a decrease in the temperature sensitivity of the dislocated regions. These studies highlight the importance of conducting further spatial analysis into the temperature dependence of solar cells.

In this work, we investigate the temperature sensitivity of wafers and cells fabricated from several positions along two industrially grown *p*-type mc-Si bricks with different dislocation densities [21]. We used our recently developed spatially resolved photoluminescence (PL) based system to measure various regions such as grain boundaries, dislocation clusters and intra-grain regions. The results are correlated with the TCs of PERC cells fabricated using sister wafers in an industrial production line.

F.II. Experimental Method

A. Sample Preparation

Fourteen wafers from two industrially grown *p*-type boron-doped mc-Si centre bricks are used (produced in ~ 2015), seven from each brick. Of the seven wafers obtained from each brick, two originate from near the top of the brick, two from near the bottom and the remaining three wafers from positions in between. One brick has a high dislocation density, while the second brick has a low dislocation density. The exact dislocation density is determined using the algorithm implemented in our commercial PL imaging tool (BT Imaging, LIS-R3) [21]. The resistivity of the wafers varies between 1.5 and $2.2\,\Omega\cdot\mathrm{cm}$. The wafers were saw-damage etched (final thickness: $185 \pm 10\,\mu\mathrm{m}$) before undergoing a phosphorus-based gettering process [22, 23]. After etching off the diffused layer, the wafers were recleaned before undergoing silicon nitride (SiN_x) passivation (75 nm) using an industrial plasma-enhanced chemical vapour deposition system (MAiA, Meyer Burger) [24]. Please note that wafers were not fired or annealed. Fourteen solar cells made from sister wafers are also included in the study. The cells were fabricated in an industrial PERC production line [21].

The samples are studied using our recently developed temperature dependent PL imaging system described below. The PL images are acquired at temperatures from 298 K to 343 K under 0.5 Sun illumination (the highest light intensity that currently can

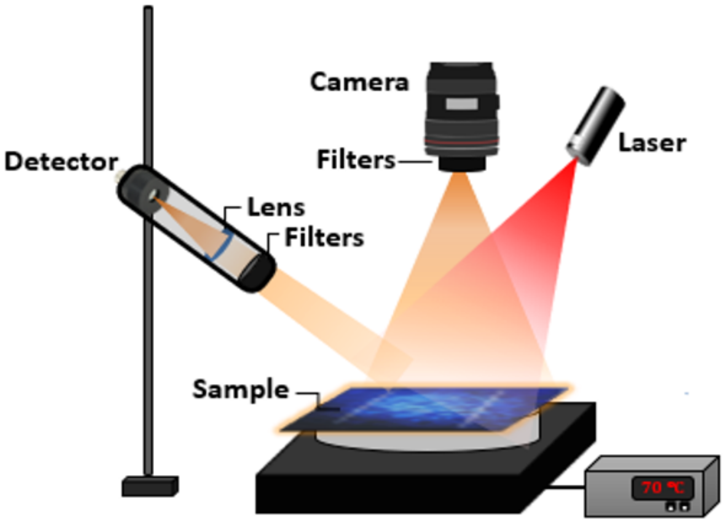

Figure F.1: Schematic of the experimental setup (not to scale).

be achieved for 6-inch samples with our setup). The relative PL images are then calibrated and converted into implied-V_{OC} (iV_{OC}) images using front detection quasi-steady-state (QSS) PL measurements (see below and in Refs. [25] and [26]) conducted under identical conditions to those used during the PL imaging. In order to test the validity of our method, the current-voltage (I-V) characteristics of the cells are measured at the same temperature range (298 K to 343 K) using a Wavelabs I-V tester (model SINUS-220).

B. Experimental Setup

Fig. F.1 shows a schematic of the PL-based measurement system used to obtain effective lifetime (τ_{eff}) and iV_{OC} images of wafers and cells at different temperatures. The system consists of a silicon charge-coupled device (CCD) camera and an 808 nm diode laser. Optical filters (long pass filters 950 nm and 850 nm, and a short pass filter 1000 nm) are placed in front of the camera to avoid detection of any reflected excitation light. A circular (diameter of 15 cm) temperature-controlled stage (Sinton Instruments WCT-120 TS) is used to heat the wafers and cells to higher temperatures [27]. The wafer temperatures are measured by a k-type thermocouple in direct contact with a similar sample.

The obtained PL images are then calibrated using the QSS-PL front detection method described in Refs. [25] and [26]. The PL emission from a selected region is focussed into a PL detector (InGaAs photodiode) with a lens. A customised filter set is attached to the lens to ensure the detection of only the band-to-band PL emission from the samples. A second photodiode is used to monitor the incident photon flux during measurements. Both photodiodes are connected to low-noise pre-amplifiers. In addition, a photoconductance (PC) signal from a defined region of the wafer is recorded by an inductive coil in the

Sinton WCT-120TS to improve the accuracy of the calibration procedure.

All signals are recorded with a data acquisition card that is connected to a computer. An additional flash is used when higher injection levels are required. The primary advantage of this setup is that it enables the determination of absolute τ_{eff} and iV_{OC} values for both metallised and non-metallised samples (in contrast to using only PC-based measurements [16, 27]). Moreover, this method is resilient to the effects of trapping and depletion region modulation (DRM) [28, 29].

C. Data Analysis Procedure

The conversion from relative PL counts to τ_{eff} and iV_{OC} maps is based on the relationship between the emitted PL intensity and the excess carrier density (Δn) at each pixel which is described by [30]:

$$\mathrm{PL}_{xy}(T) = A_i(T)B(T)\left(N_{\text{dop}} + \Delta n_{xy}(T)\right)\Delta n_{xy}(T), \tag{F.2}$$

where PL_{xy} is the PL intensity at pixel (x, y), A_i is a calibration constant that depends on the specific sample and system [30]. A_i can be found either by matching the PC and PL measurement at high injection level (only for wafers) or using the self-consistent method (for both wafers and cells) [30, 31]. B is the radiative recombination coefficient [33, 34] and N_{dop} is the bulk dopant density.

In this study, the calibration of the constant A_i for PL imaging is performed using temperature-dependent QSS-PL measurements of τ_{eff} obtained from the illuminated surface of the sample. Using the determined A_i, $\tau_{\text{eff},xy}$ can be calculated using:

$$\tau_{\text{eff},xy}(T) = \frac{\left(-N_{\text{dop}} + \sqrt{{N_{\text{dop}}}^2 - 4\left(\frac{\mathrm{PL}_{xy}(T)}{A_i(T)B(T)}\right)}\right)}{2G}, \tag{F.3}$$

where G is the generation rate considering the photon flux of the illumination source, the wafer reflectance and its thickness. $iV_{\text{OC},xy}$ is calculated using:

$$iV_{\text{OC},xy}(T) = \frac{kT}{q}\ln\left(\frac{\mathrm{PL}_{xy}(T)}{A_i(T)B(T)n_i(T)^2}\right). \tag{F.4}$$

The band gap energy model of Passler [35] combined with the effective hole mass parameterisation of Couderc *et al.* [36] are used to determine n_i. The subsequent local absolute $\mathrm{TC}(iV_{\text{OC},xy})$ is obtained from calibrated PL images taken at different temperatures via:

$$\mathrm{TC}\left(iV_{\text{OC},xy}\right) = \frac{iV_{\text{OC},xy}\left(T_2\right) - iV_{\text{OC},xy}\left(T_1\right)}{T_2 - T_1}, \tag{F.5}$$

where T_1 is 298 K and T_2 is 343 K. Eq. (F.5) simplifies the determination of TC, as it uses only two temperatures. We have tested this simplification by taking six measurements

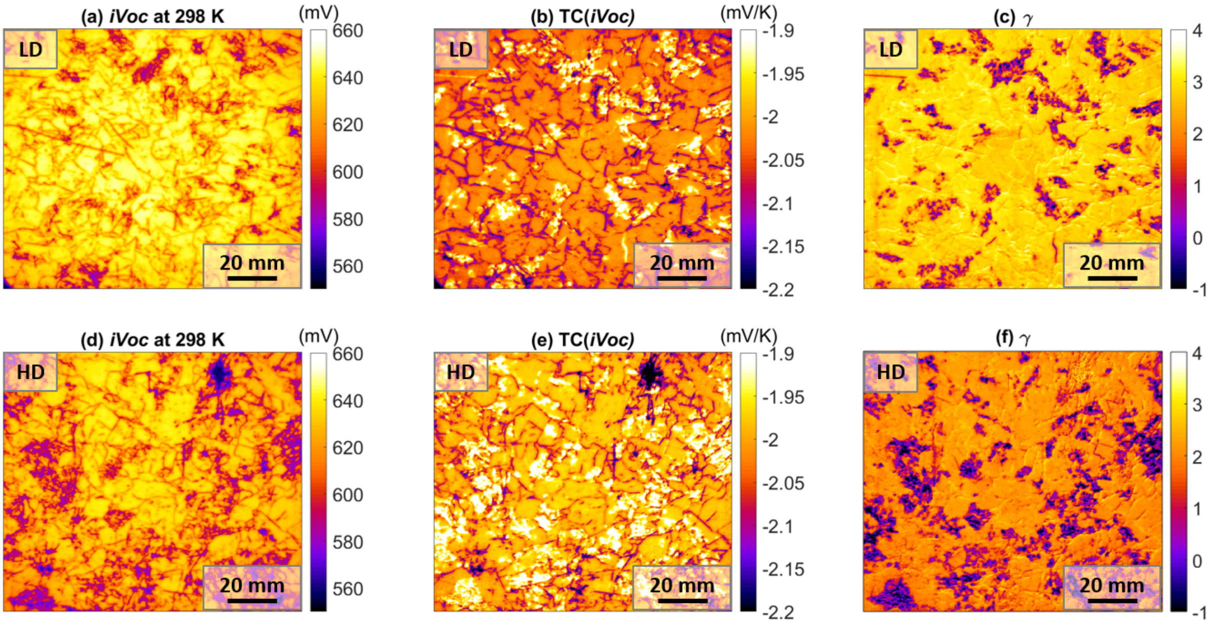

Figure F.2: Spatially resolved iV_{OC} at 298 K (a, d), TC(iV_{OC}) (b, e) and γ (c, f) of two wafers with low (a-c) and high (d-f) dislocation densities under 0.5 Sun illumination. Note that these images were cropped to present only the regions of interest.

between 298 K and 343 K at 10 K intervals. A linear reduction of iV_{OC} with increasing temperature is observed in this temperature range. A good agreement ($\sim 2\,\%$) is found between the comparison between the TC obtained from Eq. (F.5) and the TC obtained from the slope of the linear fit, thus confirming the validity of the simplified approach of Eq. (F.5).

F.III. Results and Discussion

A. Spatially Resolved Mapping

An example of the various parameter images obtained by the proposed method is depicted in Fig. F.2. Two wafers from the middle of each brick are compared [resistivity: $1.8 \pm 0.1\,\Omega{\cdot}\mathrm{cm}$; high and low dislocation densities]. Figs. F.2(a) and (d) show iV_{OC} maps at 298 K. As expected, lower iV_{OC} values are observed in areas with dislocation clusters (appear as dark clusters in the PL images) and grain boundaries (dark lines). The calculated average iV_{OC} of the highly dislocated (HD) wafer is 611 ± 3 mV, which is 15 mV ($\sim 2.5\,\%$) lower than the average iV_{OC} of the lowly dislocated (LD) wafer (626 ± 3 mV).

Images of TC(iV_{OC}) are displayed in Figs. F.2(b) and (e). A large variation of TC(iV_{OC}) across the wafers is observed. The data show that TC(iV_{OC}) is more negative in grain boundaries and some dislocation clusters, indicating a larger reduction of iV_{OC} with increasing temperature in these regions compared to other areas across the

Table F.1: Implied-V_{OC}, TC(implied-V_{OC}) of a highly dislocated cell from the middle of the brick.

PL-based	iV_{OC} at 298 K	TC(iV_{OC})
method	627 mV	-1.87 mV/K
I-*V*	V_{OC} at 298 K	TC(V_{OC})
measurement	625 mV	-1.89 mV/K

wafer. The majority of the dislocation clusters show lower temperature sensitivity. This observation contradicts the common belief that the temperature sensitivity is expected to increase with decreasing iV_{OC} [4,12]. Previous studies have observed only low temperature sensitivity of dislocation clusters [17,18]. However, in this study, dislocated regions of two tested bricks show both high and low temperature sensitivities. This discrepancy could possibly be explained by differences in the processing procedure for the investigated wafers.

Figs. F.2(c) and (f) present γ maps calculated by applying Eq. (F.1) to each pixel [17, 18]. There is a clear difference between the two bricks, with global values of 2.29 for the LD wafer and 1.35 for the HD wafer. Lower γ values (even negative), consequently reduced J_0 [17], are observed at dislocation clusters, explaining the more uniform γ distribution across the LD wafer (and larger average γ). The source for the interesting (and unexpected) negative γ is discussed in Refs. [14,18,37]. Dupré *et al.* explained that global negative γ values of cells are mostly due to an increase of external radiative efficiency (detailed explanation regarding external radiative efficiency can be found in Ref. [38]) at open circuit of these cells with temperature [14]. However, the physics behind this negative γ is still unclear and requires further investigation.

To assess the validity of our method, we compare cell measurements obtained using our proposed method with cell measurements obtained using the established *I*-*V* technique [15,39–41]. Fig. F.3 illustrates the iV_{OC} map of one of the PERC cells originating from the middle of the HD brick [sister cell of the wafer of Figs. F.2(d)-(f)] and its corresponding TC(iV_{OC}) map under 0.5 Sun illumination. Note that a circular heat stage is used for the PL imaging, causing a circular pattern. Only the middle region is used for subsequent analysis. The local values are harmonically averaged and compared with the results obtained from global *I*-*V* measurements (using a Wavelab *I*-*V* tester) for the same solar cell. The harmonic average is used as it provides a better estimation of the material quality for predicting cell performance [42,43]. Table F.1 summarises the results. Excellent agreement with relative deviations in the range of 1 % is found between the two measurements.

By comparing iV_{OC} maps with TC(iV_{OC}) maps of the cells, the regions near the con-

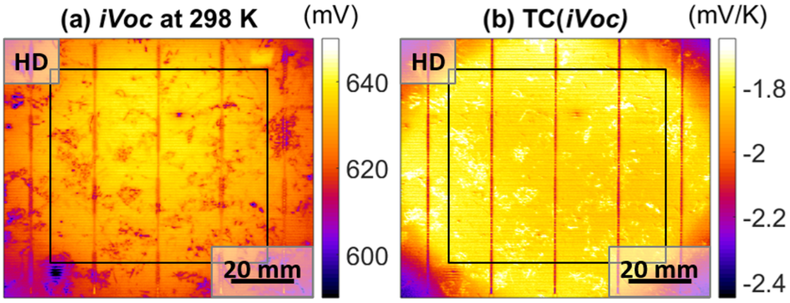

Figure F.3: (a) Spatially resolved iV_{OC} at 298 K and (b) TC(iV_{OC}) of a PERC cell originating from the middle of the highly dislocated brick under 0.5 Sun illumination.

tacts (especially busbars) show higher temperature sensitivity, as expected from the higher recombination in these areas in comparison with the well passivated regions between the contacts. Reduced temperature sensitivity regions are found to be correlated with dislocated areas. Comparing the cell with the wafer, the temperature sensitive regions across the sister wafer (such as grain boundaries and some dislocation clusters [Figs. F.2(d) and (e)]) are not as easily identified on the cell maps [Figs. F.3(a) and (b)]. The difference can be explained by the lateral conduction over the cell and the incomplete fabrication process of the wafers, particularly the lack of firing. This hypothesis requires further investigation and will be studied in our future work.

B. Impact of Brick Height

Fig. F.4(a) shows the harmonically averaged iV_{OC} at 298 K extracted from calibrated PL images of the wafers from both the HD and LD bricks. As expected, the LD brick has high iV_{OC} values compared to the HD brick. For both bricks, the highest iV_{OC} is observed in the middle of the brick; the iV_{OC} declines gradually towards the bottom and top of the brick. This trend follows the variation of material quality with brick height, where the top and bottom of the brick contains a higher impurities concentration due to segregation from the liquid-to-solid phase and diffusion from the crucible [44, 45]. A similar trend has been observed in Ref. [45]. The global V_{OC} values of the sister cells measured using a temperature dependent I-V tester are presented in Fig. F.4(b). The variation of V_{OC} along the brick is less obvious compared to the wafers, however, the V_{OC} of top and bottom cells are still lower than those of the more central cells. The cells exhibit higher voltage values compared to the sister wafers; this is more pronounced for bottom cells. This can be explained by the lack firing of the wafers, a process which often passivates large fractions of the grain boundaries [45].

Fig. F.4(c) shows the average TC(iV_{OC}) values extracted from calibrated PL images of the wafers and global TC(V_{OC}) values for the cells as a function of brick height. The

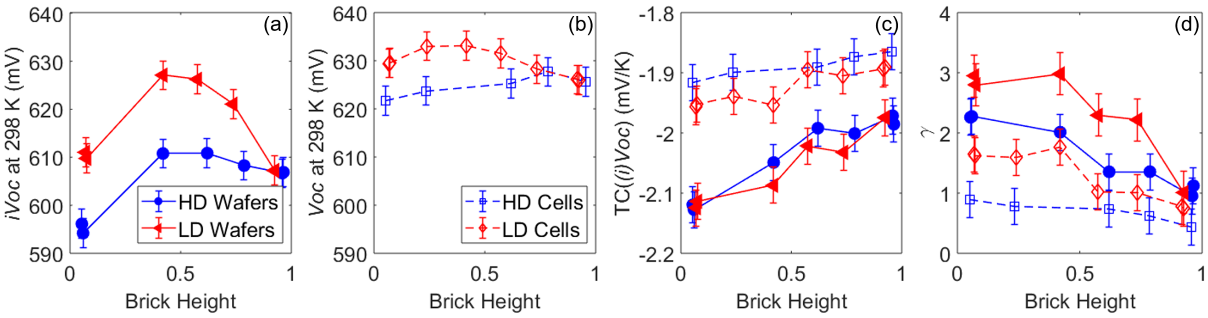

Figure F.4: Global results of wafers and sister cells with low and high dislocation densities as a function of brick height under 0.5 Sun illumination: (a) iV_{OC} at 298 K, (b) V_{OC} at 298 K, (c) TC(iV_{OC}) and TC(V_{OC}) and (d) γ.

TC(iV_{OC}) values of the investigated wafers are found to be less negative with increasing brick height (from -2.15 mV/K to -1.95 mV/K), although, the top wafers show reduced iV_{OC} values. The improved TCs of the top wafers can be explained by an increasing TC(τ_{eff}) towards the top of the brick, as discussed in Ref. [41]. Moreover, the increasing density of dislocation clusters showing low temperature sensitivity with increasing brick height (see Fig. F.7) could also contribute to the low temperature sensitivity towards top of the brick. This is likely due to increased concentration of impurities that causes low temperature sensitivity [18].

The cells exhibit a similar trend, with a lower temperature sensitivity and less variation along the brick. This is in agreement with previous studies presented in Refs. [15, 40, 41].

There is no clear difference (when considering the measurement uncertainty as represented by the error bars) in the global temperature sensitivity between the two bricks (for both wafers and cells). We cannot confidently pinpoint the impact of dislocation density on the global TC values since dislocation clusters show both high and low TC(iV_{OC}) as demonstrated in Fig. F.2.

Fig. F.4(d) shows the average γ values of the cells and wafers [calculated using Eq. (F.1)] as a function of brick height. Like the cells, the wafers exhibit a decreasing γ with increasing brick height. Berthod *et al.* observed a similar trend on compensated materials [15]. Interestingly, the wafers exhibit larger γ values compared to the cells and stronger variation along the brick, indicating a change of the limiting recombination mechanism from bottom to top of the brick.

Fig. F.5 shows the pixel-level TC(iV_{OC}) as a function of iV_{OC} at 298 K under 0.5 Sun illumination. The colour represents the data density normalised to unity (‘1’ represents the highest density). For all the measured wafers, as expected theoretically from Eq. (F.1), the temperature sensitivity tends to decrease with increasing iV_{OC}. However, it is very interesting to observe that regions with similar iV_{OC} (at 298 K) show a large spread, up

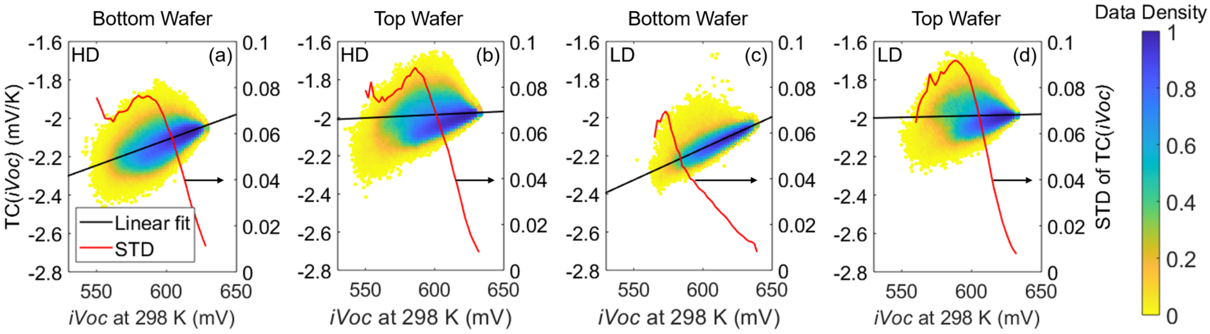

Figure F.5: Density scatter plot of TC(iV_{OC}) as a function of iV_{OC} at 298 K of highly dislocated wafers and lowly dislocated wafers from bottom and top of the bricks under 0.5 Sun illumination with the line of best linear fit (black) and TC(iV_{OC}) standard deviation (red) overlay. The standard deviation shown is for iV_{OC} bins of 2 mV.

to 40 %, in TC(iV_{OC}), showing that temperature sensitivity can only be well understood by spatially resolved measurements.

The spread of TC(iV_{OC}) across the wafers in the iV_{OC} domain is quantitatively determined as standard deviation (STD) of TC(iV_{OC}) at different iV_{OC} bins. For all wafers, low STD occurs at high iV_{OC}, while the medium to low iV_{OC} range shows high STD. A shift of TC(iV_{OC}) towards less negative values is noticeable for the top wafers. This is consistent with our observation that the average temperature sensitivity reduces with increasing brick height.

A linear fit of TC(iV_{OC}) as a function of iV_{OC} at 298 K is also included in Fig. F.5. A clear trend of reduced TC for increasing iV_{OC} is observed for the bottom wafers of both bricks. However, no clear trend can be observed for the top wafers due to the larger spread of TC across these wafers at medium to low iV_{OC} range (as indicated by the larger STD values).

The slope of the linear fit, representing the change of TC as a function of iV_{OC}, as a function of brick height is shown in Fig. F.6. It seems the slope of the fits decreases with increasing brick height, indicating a reduction in the TC variation across the wafers closer to the top of the brick. These results suggest that some disadvantages associated with mc-Si wafers originating from the top of the brick, such as a higher defect concentration resulting in lower performance at room temperature [44, 45], is weakened at higher temperatures.

Fig. F.7 presents maps of iV_{OC} at 298 K, TC(iV_{OC}), and the resulting γ of two wafers originating from the bottom (a-c) and top (d-f) of the HD brick. As expected, small grains and a large fraction of grain boundaries can be observed in the bottom wafer. It seems that for the bottom wafer, almost all the low-quality regions (grain boundaries and dislocated regions) show a higher temperature sensitivity compared to the intra-grain

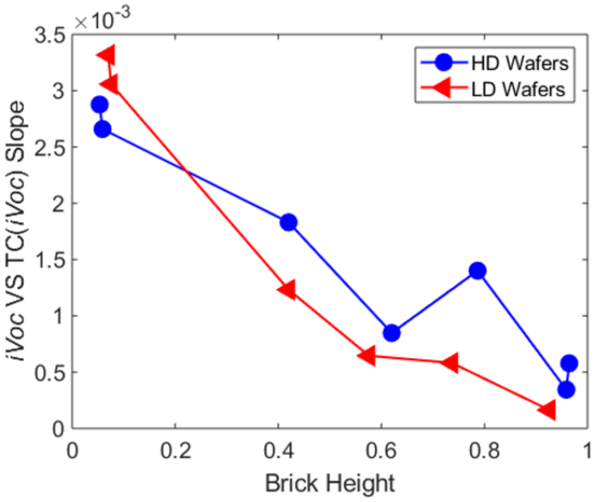

Figure F.6: Variation of TC with iV_{OC} at 298 K (slope of linear fit) as a function of brick height.

Table F.2: iV_{OC}, TC, and γ of different ROIs across a highly dislocated wafer from the top of the brick.

	iV_{OC} (mV)	TC(iV_{OC}) (mV/K)	γ
ROI (a)	584	-2.14	2.00
ROI (b)	580	-1.95	-0.32
ROI (c)	594	-1.95	0.19

regions. In contrast, the difference between these regions appears less significant in the top wafer, where most of the dislocation clusters show a low temperature sensitivity. In general, it seems that wafers from the top of the brick are less sensitive to temperature variations compared to wafers from the bottom (see global TC values in Fig. F.4). This could be attributed to the impact of a higher density of grain boundaries and different impurities in the lower wafer. It is also possible that the dislocations are decorated by different impurities with different impacts on the temperature sensitivity of the wafers. This will be discussed in the next section.

C. TC(iV_{OC}) of Dislocation Clusters

To investigate the source of the large variation in the TC(iV_{OC}) of dislocation clusters, dislocated areas with different TCs were selected for further investigation. Three different regions of interest (ROI) are defined [as shown in Figs. F.7(d) to (f)]. Table F.2 summarises the obtained parameters for these regions.

All three ROIs are low-quality regions containing dislocation clusters. ROIs (a) and (b) have a similar iV_{OC} at 298 K, but very different TC; whereas ROIs (b) and (c) have

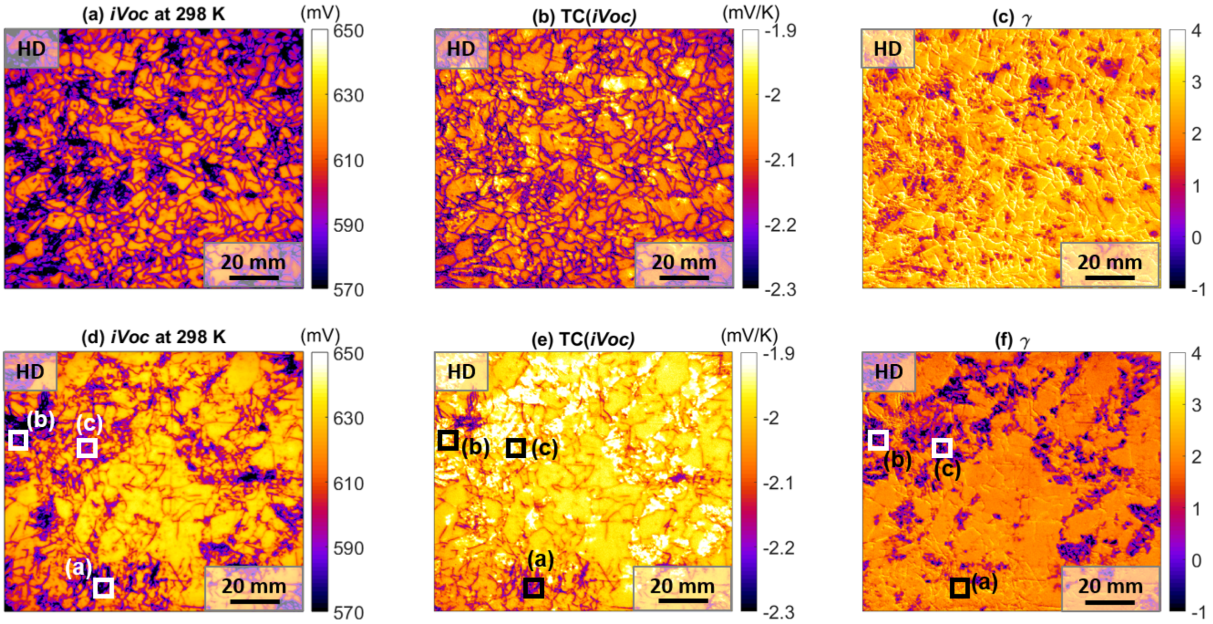

Figure F.7: Spatially resolved iV_{OC} at 298 K, TC (iV_{OC}) and γ of two highly dislocated wafers from the bottom (a-c) and the top (d-f) of the brick under 0.5 Sun illumination. Note that these images were cropped to present only the regions of interest. (The corresponding temperature-dependent τ_{eff} images are given in Appendix A).

a similar TC, but different iV_{OC}. The γ values of ROIs (b) and (c) are much smaller than one (and even negative), while for ROI (a) $\gamma = 2$, indicating that different dominant recombination mechanisms limit the performance of these three regions.

We examined these regions by micro-PL (μPL) spectroscopy [46]. Fig. F.8 shows the PL spectra of ROIs (a) and (c) at an actual sample temperature of 122 ± 7 K (the actual sample temperature is obtained by modelling the band to band (BB) peak [47]). Low temperatures are chosen for the investigation, as defect-peaks are strongly temperature-quenched and therefore more noticeable at lower temperatures. The four dislocation-related lines are labelled as D1 (0.812 eV), D2 (0.875 eV), D3 (0.934 eV), and D4 (1.000 eV) [48]. D1, D3 and D4 can be identified in both regions, indicating that both regions are highly dislocated.

To distinguish between these regions, temperature-dependent μ-PL measurements are performed at a wide temperature range from 127 K to 302 K. An example is shown in Fig. F.9 for ROI (c). The D1 peak is dominant at medium- to high-temperatures, while D3 and D4 cannot be observed above 240 K. Each defect peak is fitted using the Voigt function [49]. Since the D1 peak can be observed across the entire temperature range (even at high temperatures), we extract the activation energies (E_{a}) of D1-associated defects at both ROIs [50, 51] by using an Arrhenius plot (Fig. F.10) to fit the spectrally integrated defect PL.

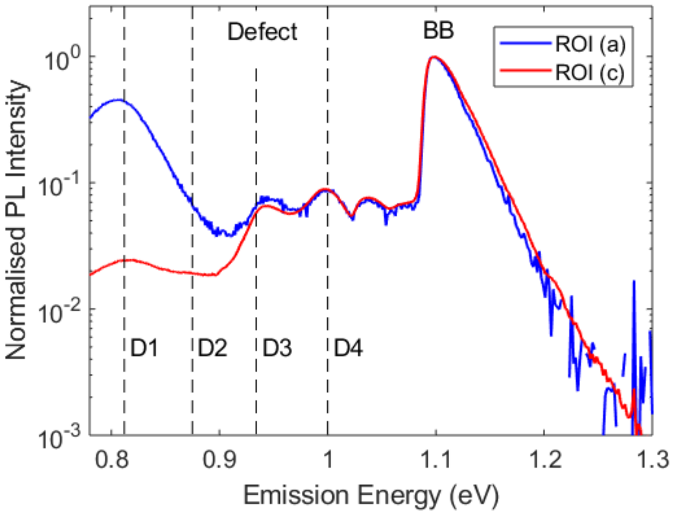

Figure F.8: PL spectra of ROIs (a) and (c) of a highly dislocated wafer from the top of the brick at 122 ± 7 K (actual sample temperature) under 20 Suns.

In order to extract E_a of the D1-associated defects, the spectrally integrated $\mathrm{PL}_\mathrm{defect}(T,\Delta n)$ is fitted to the equation below (the derivation of this equation is given in Appendix B) [52]:

$$\mathrm{PL}_\mathrm{defect}\,(T,\Delta n) = \frac{\mathrm{PL}_0}{1+\frac{C}{\Delta n(T)}T^{1.5}\exp\left[-\frac{E_\mathrm{a}}{kT}\right]} \tag{F.6}$$

where PL_0 and C are positive constants. PL_0 represents the $\mathrm{PL}_\mathrm{defect}$ as the temperature approached 0 K. $\Delta n(T)$ is calculated relatively using the spectrally integrated BB PL and the ionised acceptors (N_A^-) [53] as $\Delta n(T) \propto [\mathrm{PL}_\mathrm{BB}(T)]\,/\,\left[B(T)^* N_A^-(T))\right]$. The measurement is assumed to be at low injection based on the extrapolated lifetime curves. This assumption is also confirmed using a PC1D simulation [54] of the sample using the maximum observed bulk lifetime of 30 μs, yielding a maximum excess carrier density that is only twice the doping density. This assumption should become even more valid at lower temperatures, as the lifetime decreases with decreasing temperature. For ROI (c), similar to Ref. [55], the measurement cannot be fitted at low temperatures. The reason for that has not been provided in Ref. [55] although it is stated that this type of behavior seems not to be an effect characteristic of dislocation clusters.

The two different extracted values of E_a are 75 ± 2.3 meV for ROI (a) and 130 ± 2.9 meV for ROI (c). It may indicate that different impurities occupy these two regions. Compared to ROI (a), ROI (c) shows a stronger reduction of $\mathrm{PL}_\mathrm{defect}$ with increasing temperature (Fig. F.10), indicating that recombination strongly decreases with temperature. This suppresses the effect of the temperature dependence of n_i which reduces the magnitude of the decrease of iV_OC with increasing temperature. As a result, the temperature sensitivity at ROI (c) is lower.

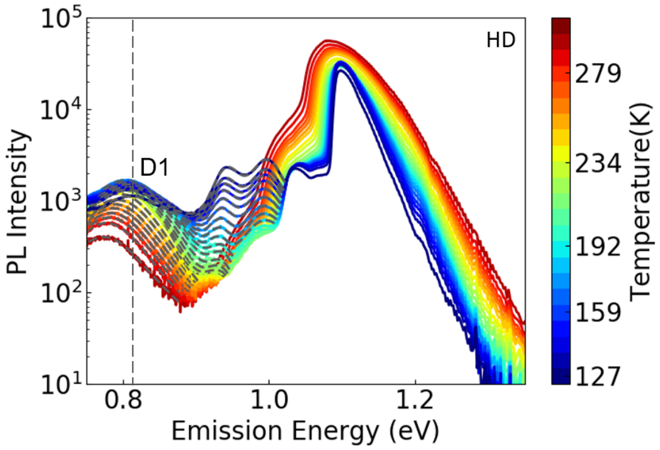

Figure F.9: PL spectra of ROI (c) at a sample temperature range from 127 K to 302 K under 20 Suns.

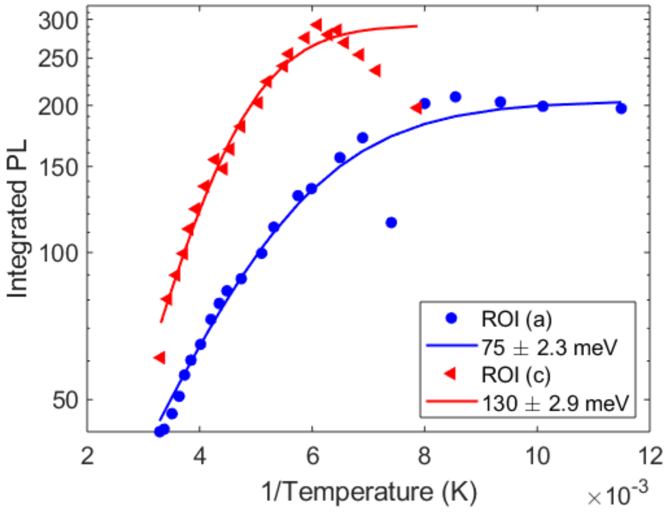

Figure F.10: Arrhenius plot of ROI (a) and (c) with the best fit.

F.IV. Conclusions

We presented a method for measuring temperature dependent iV_{OC} images on metallised and non-metallised samples without the impact of trapping and DRM, by combining PL imaging and QSS-PL front detection measurements. This spatially resolved measurement allows for assessing both local and global temperature characteristics of wafers and cells, providing more information regarding the material properties than conventional global measurements.

The TCs of wafers and cells from different brick heights with different dislocation densities were studied. The local results demonstrate that dislocated areas on wafers show both high and low temperature sensitivity. Moreover, γ is found to exhibit low values (even negative) in areas of dislocation clusters with low temperature sensitivity.

Global TC(iV_{OC}) values of the investigated wafers and cells are found to be less negative with increasing brick height. Furthermore, the wafers from the top of the bricks show less variability in TC(iV_{OC}) as a function of iV_{OC} compared to the rest of the wafers. This is due to a larger spread of TC(iV_{OC}) which is particularly evident at a medium to low iV_{OC} range observed for the top wafers. This suggests that cells made from wafers from the top of the brick will perform relatively better at higher temperatures. μ-PL was performed at dislocated regions with different TC values. E_a is found to be 130 ± 2.9 meV and 75 ± 2.3 meV for the dislocation clusters with low and high temperature sensitivity, respectively, may indicate that different impurities occupy these two regions thereby resulting in different TC values.

This work highlights the importance of studying TC values with spatial resolution. Future applications of this method could involve optimisation of solar cell and wafer performance under non-STC.

Appendix A

The τ_{eff} images of two wafers originating from the bottom and top of the HD brick at 298 K and 343 K are shown in Figs. F.11 and F.12. Please note these two images correspond with the wafers shown in Fig. F.7.

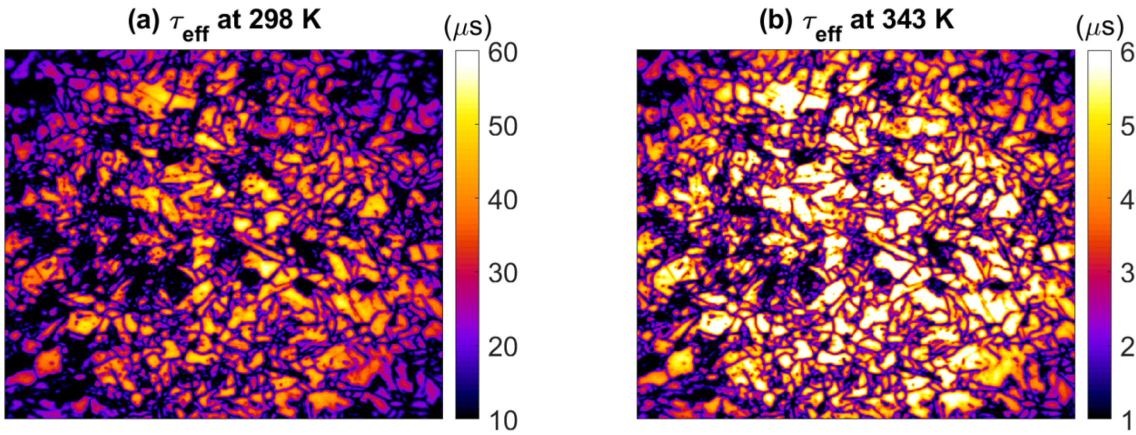

Figure F.11: Spatially resolved τ_{eff} of a wafer from the bottom of the highly dislocated brick under 0.5 Sun illumination at (a) 298 K and (b) 343 K. Note that these images were cropped to present only the regions of interest.

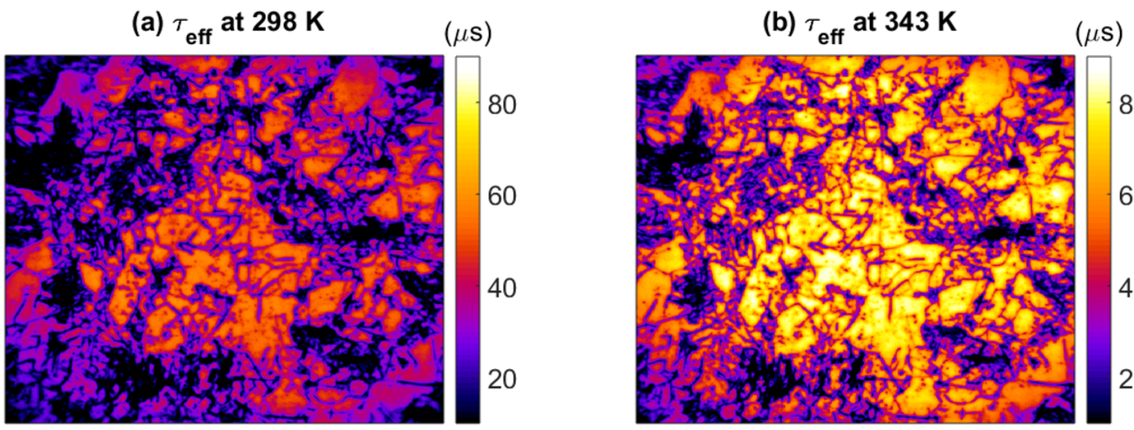

Figure F.12: Spatially resolved τ_{eff} of a wafer from the top of the highly dislocated brick under 0.5 Sun illumination at (a) 298 K and (b) 343 K. Note that these images were cropped to present only the regions of interest.

Appendix B

The activation energy is extracted based on Ref. [52] as the recombination mechanism in this study for the defect PL is donor-acceptor pair recombination [a blue-shift (2-3 meV) of the defect peaks is observed as the light intensity (carrier injection) is increased]. The equation for donor-acceptor pair recombination rate (U_{DAP}) for a p-type semiconductor can be expressed as:

$$U_{\text{DAP}} = \frac{pN_{\text{defect}}C_{p2}t'}{\left(p + p'_{\frac{3}{2}}\right)C_{p2} + t'}, \tag{F.7}$$

where N_{defect} is the defect density, C_{p2} is the capture probability of holes to the acceptors when the donor-acceptor is in the charge state of TWO, t' is the interlevel transition rate between donor and acceptor levels, $p'_{\frac{3}{2}}$ is a carrier density term containing the acceptor energy level and p is the hole concentration.

Assuming $\left(p + p'_{\frac{3}{2}}\right)C_{p2} \gg t'$, Eq. (F.7) can be re-arranged as:

$$U_{\text{DAP}} = \frac{N_{\text{defect}}t'}{\left(1 + \frac{p'_{\frac{3}{2}}}{p}\right)} \tag{F.8}$$

where $p'_{\frac{3}{2}}$ is given by

$$p'_{\frac{3}{2}} = CT^{1.5}e^{-\frac{E_a}{kT}} \tag{F.9}$$

By combing Eqs. (F.8) and (F.9), Eq. (F.6) is obtained and can be used to determine the activation energy.

Acknowledgement

This work was supported by the Australian Government through Australian Renewable Energy Agency [ARENA; project 2017/RND001]. The views expressed herein are not necessarily the views of the Australian Government, and the Australian Government does not accept responsibility for any information or advice contained herein.

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Paper G

Temperature coefficients of crystal defects in multicrystalline silicon wafers

Published as:

S. T. Kristensen, S. Nie, C. Berthod, R. Strandberg, J. O. Odden, and Z. Hameiri, ”Temperature coefficients of crystal defects in multicrystalline silicon wafers”, *IEEE Journal of Photovoltaics*, vol. 10, no. 2, pp. 449-457, 2020.

doi: 10.1109/JPHOTOV.2020.2968111

Temperature coefficients of crystal defects in multicrystalline silicon wafers

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Abstract **— This article investigates the influence of crystallographic defects on the temperature sensitivity of multicrystalline silicon wafers. The thermal characteristics of the implied open circuit voltage is assessed since it determines most of the total temperature sensitivity of the material. Spatially resolved temperature dependent analysis is performed on wafers from various brick positions; intragrain regions, grain boundaries, and dislocation clusters are examined. The crystal regions are studied before and after subjecting the wafers to phosphorus gettering, aiming to alter the metallic impurity concentration in various regions across the wafers. Most intragrain regions and grain boundaries are found to show similar thermal characteristics before gettering. The gettering process has no substantial effect on the temperature sensitivity of intragrain regions, whereas it increases the sensitivity of most grain boundaries. Dislocation clusters exhibit both highest and lowest temperature sensitivities compared with other crystal regions before and after gettering. Images of the recombination parameter γ are created and related to the temperature sensitivity of the Shockley-Read-Hall (SRH) lifetime of the impurities in the material. The results suggest that most intragrain regions and grain boundaries are limited by SRH centers with a modest lifetime**

temperature sensitivity in the studied temperature range. Dislocation clusters are found to contain recombination centers with an effective lifetime that has a beneficial temperature sensitivity. The gettering process is observed to alter the composition of the recombination centers in the dislocation clusters, resulting in an SRH lifetime with an even more favorable temperature sensitivity for most clusters.

G.I. Introduction

Solar cells are usually characterized and optimized under standard test conditions (STC), defined as a global standard solar spectrum AM1.5G, an irradiance of $1000\,\mathrm{W/m^2}$ and a cell temperature of $25\,^\circ\mathrm{C}$ [1]. However, real operating temperatures can differ considerably from STC depending on the climate at the location of the installed device [2–4].

The characteristics of solar cells are significantly influenced by the operating temperature as has been studied for decades [4–7]. This causes the performance of most cell types to decrease linearly with increasing temperature [4]. Understanding the performance of solar cells under non-STC is therefore essential to accurately forecast the power production of photovoltaic (PV) installations and to optimize solar cells for different climatic conditions.

The temperature dependence of a solar cell is mainly determined by the temperature sensitivity of the open circuit voltage (V_{oc}). It accounts for approximately $80-90\,\%$ of the total temperature sensitivity of a device which is not constrained by resistance or other fill factor losses [8]. The V_{oc} decreases with increasing temperature due to a reduction of the band gap energy (E_{g}) which consequently increases the intrinsic carrier concentration (n_i) [8–10].

The temperature sensitivity of the V_{oc} can be quantified using the temperature coefficient ($\beta_{V_{\mathrm{oc}}}$) which is a measure of the rate of change in V_{oc} with temperature. In absolute form, and to the first-order approximation, it is given as [11]

$$\beta_{V_{\mathrm{oc}}} = \frac{dV_{\mathrm{oc}}}{dT_{\mathrm{c}}} = -\frac{E_{\mathrm{g0}}/q - V_{\mathrm{oc}} + \gamma k T_{\mathrm{c}}/q}{T_{\mathrm{c}}} \tag{G.1}$$

where E_{g0} denotes the semiconductor bandgap energy extrapolated to $0\,\mathrm{K}$, q is the elementary charge, k is the Boltzmann constant, and T_{c} is the cell temperature. The parameter γ includes the temperature dependence of several parameters determining the dark saturation current, J_0. It can be correlated to physical quantities through [12]

$$\gamma = 1 - \frac{d\ln ERE_{\mathrm{oc}}}{d\ln T_{\mathrm{c}}} + \left(2\frac{d\ln E_{\mathrm{g}}}{d\ln T_{\mathrm{c}}} - \frac{d\ln J_{\mathrm{sc,1sun}}}{d\ln T_{\mathrm{c}}}\right) \tag{G.2}$$

where ERE_{oc} denotes the external radiative efficiency at open circuit condition and $J_{\mathrm{sc,1sun}}$ is the short circuit current density at 1 Sun. The ERE is defined as “the fraction of total dark saturation current in the device that results in radiative emission from the device" [13]. Eq. (G.2) is mainly determined by the first two terms, meaning that γ contains information about the dominant recombination mechanism in the material. According to Ref. [6], γ usually takes values between 1 and 4 but other, including negative values, have been observed experimentally in recent studies [14–17].

From Eq. (G.1), an approximately linear relationship is predicted between the temperature sensitivity and the material quality. This indicates that a cell with a high V_{oc} will have the inherent advantage of reduced temperature sensitivity. However, $\beta_{V_{\mathrm{oc}}}$ can be significantly influenced by the last term in Eq. (G.1) containing the γ parameter [12]. As an example, it accounted for up to 10 % of the $\beta_{V_{\mathrm{oc}}}$ for the cells mentioned in Ref. [12].

In recent years, increased attention has been given to the influence of crystallographic defects on the temperature sensitivity of silicon wafers and solar cells [14, 16–20]. Eberle *et al.* reported increased temperature sensitivity of V_{oc} in contaminated regions of multicrystalline silicon (mc-Si) cells, but reduced temperature sensitivity for areas containing dislocation clusters [14]. This was further investigated by Eberle *et al.* in a following study, reporting reduced temperature sensitivity of dislocation clusters of mc-Si wafers and cells [18]. The authors suggested that it could be caused by the presence of impurities in the clusters and thus impacted by Shockley-Read-Hall (SRH) recombination. Additionally, more recent studies have reported reduced temperature sensitivity in some dislocation clusters of mc-Si wafers and cells and identified advantageous thermal behavior of wafers originating from the top of the bricks [16,17,19–21]. These findings illustrate the importance of further studies to evaluate the varying influence of different defect types on the temperature sensitivity of V_{oc}.

This study investigates the influence of crystal defects on the temperature sensitivity of mc-Si wafers. The temperature coefficient of the implied V_{oc} ($\beta_{iV_{\mathrm{oc}}}$) is assessed for intra-grain regions, grain boundaries, and dislocation clusters on wafers from various brick positions. The crystal areas are examined before and after being subjected to phosphorus diffusion gettering (PDG) which is known to alter the concentration of metallic impurities across the wafers [22–26], thus, enabling an investigation of how the temperature sensitivity is influenced by metallic impurities.

G.II. Experimental Method

A. Sample Preparation

The wafers were fabricated from a high-performance (HP) *p*-type mc-Si ingot, tri-doped with boron, gallium and phosphorus. The ingot was produced from a blend of compensated silicon [Elkem Solar Silicon® (ESS®)] and polysilicon with a blend-in-ratio of 70 %

ESS® and targeted resistivity of 0.9 Ω·cm (produced in 2015). Doping and resistivity profiles of the ingot can be found in Ref. [27]. Seven 6” wafers were then chosen from a central brick, originating from different positions from the bottom to the top of the brick.

The wafers were processed in two steps: Step 1 (referred to as *ungettered*): The as-sawn wafers received saw damage etching (final thicknesses: $194\,\mu\text{m} \pm 7\,\mu\text{m}$), cleaning [28], and passivation with 75 nm silicon nitride (SiN_x) using an industrial plasma-enhanced chemical vapor deposition (PECVD) system (MAiA, Meyer Burger) at a deposition temperature of 400 °C [29]. Step 2 (referred to as *gettered*): The passivation from Step 1 was removed using hydrofluoric (HF) acid followed by a second clean. A conventional PDG [26] was performed by subjecting the wafers to a 45 min POCl_3 diffusion treatment with a peak temperature of 850 °C resulting in a sheet resistance of approximately 40 Ω·cm [30, 31]. The surface gettering layer was then removed by alkali etching and the wafers were re-passivated using an identical SiN_x process as in Step 1. The wafers were fully characterized after Step 1 and after Step 2 in order to study the effect of the PDG process.

B. Characterization

The wafers were characterized using our novel temperature dependent photoluminescence (PL) imaging system [32], enabling acquisition of PL images at elevated temperatures, and subsequently, calibration of the acquired images into spatially resolved maps of effective carrier lifetime (τ_{eff}), implied V_{oc} (iV_{oc}), $\beta_{iV_{\text{oc}}}$, and γ. The PL images were obtained at a photon flux of $1.2 \cdot 10^{17}\,\text{cm}^{-2}\text{s}^{-1}$, corresponding to an illumination intensity of approximately 0.5 Sun (the highest that can be achieved with our current setup). The images were acquired at 25 °C and 70 °C. These two temperatures are assumed to give a valid representation of the temperature dependence of iV_{oc}, since mc-Si cell parameters usually vary linearly with temperature for normal operating temperatures [8]. The validity of this assumption was confirmed by obtaining PL images of one wafer at temperatures ranging from 25 °C to 70 °C in steps of 10 °C.

The PL images of the ungettered wafers were calibrated using a temperature dependent photo-conductance (PC) signal directly measured on a region of the wafer during the PL image acquisition. A detailed description of the calibration procedure can be found in Ref. [32]. The PL images of the gettered wafers were calibrated using a novel temperature dependent PL-based detection to account for trapping observed for these wafers at relevant injection levels [33]. The calibration was performed using injection dependent τ_{eff} curves obtained by simultaneously measuring PC and PL signals on the wafer. First, the τ_{eff} curves were matched at high injection (as the PC signal is not impacted by traps at high injection), then the PL images were calibrated using the PL-based τ_{eff}. A detailed description of the calibration procedure can be found in Ref. [20]. The wafers before and after gettering were, therefore, both calibrated using PC-based measurements enabling a meaningful comparison. A sensitivity function was implemented to account for the local sensitivity profile of the PC sensor (measured according to Ref. [34]). Additionally, the doping densities from Ref. [27] and the mobility model for compensated Si were implemented in the calibration [35]. The temperature dependence of the surface recombination is assumed be negligible in the studied temperature range following Ref. [36]. After the elevated temperature measurements, τ_{eff} curves of the samples were obtained at 25 °C using a Sinton WCT-120 (Sinton Instruments) to ensure that no permanent annealing effects occurred.

C. Analysis

Examples of calibrated PL images are given in Figs. G.1(a) and (b) showing spatially resolved iV_{oc} at 25 °C before and after gettering. An image of absolute $\beta_{iV_{\text{oc}}}$ can be obtained from the calibrated iV_{oc} image by applying

$$\beta_{iV_{\text{oc,abs},xy}} = \frac{iV_{\text{oc},T2,xy} - iV_{\text{oc},T1,xy}}{T_2 - T_1}, \tag{G.3}$$

to each pixel, as is illustrated in Figs. G.1(d) and (e). Images of relative $\beta_{iV_{\text{oc}}}$ can be obtained by normalizing each pixel with the local iV_{oc} at 25 °C (not shown). Finally, maps of γ can be created by applying Eq. (G.1) to each pixel [see for example Figs. G.5(b) and (c)]. A circular heat stage (Sinton WCT-120TS, diameter of 150 mm) was used for imaging, causing both inhomogeneous wafer temperature and reflection outside of the heat stage. Therefore, only the areas with uniform temperature and reflection are used for further analysis. Different regions were selected on each wafer containing either intra-grain regions, grain boundaries, or dislocation clusters, to study the temperature sensitivity before and after PDG. Several regions of the same crystal type were investigated on each wafer to monitor the representativeness of the results. Examples of the selected regions of interest (ROIs) for (A) an intra-grain region, (B) a dislocation cluster, and (C) a grain boundary are illustrated by squares in Fig. G.1(b). Note that the actual ROI C is chosen so that only one grain boundary is selected and is therefore smaller than shown in the figure.

G.III. Results and Discussion

A. Spatially Resolved Temperature Sensitivity

To illustrate some general temperature related characteristics, Fig. G.1 presents spatially resolved images of iV_{oc} at 25 °C and $\beta_{iV_{\text{oc}}}$ of a wafer from the middle of the brick before

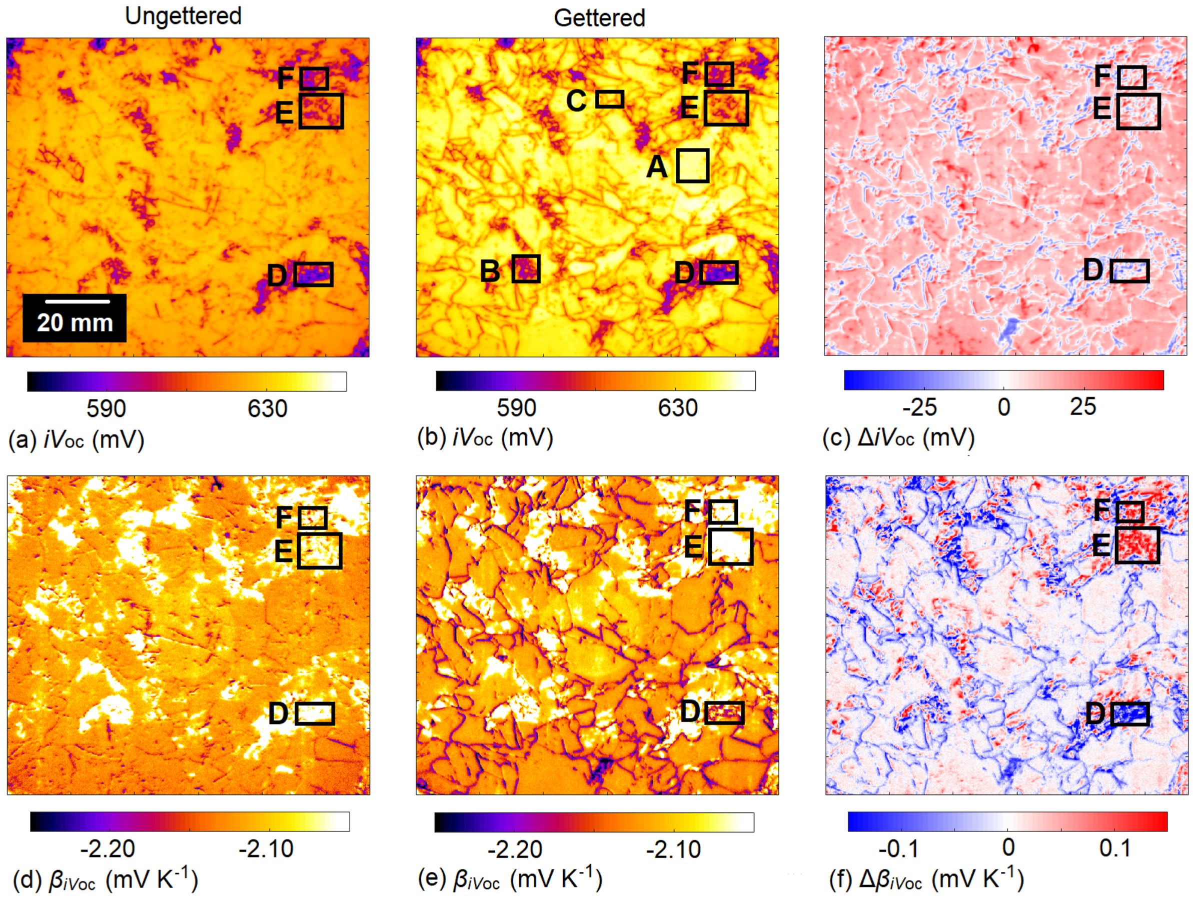

Figure G.1: Spatially resolved images of iV_{oc} at 25 °C and $\beta_{iV_{\mathrm{oc}}}$ before (a,d) and after (b,e) gettering for a wafer from the middle of the brick, and spatially resolved images of ΔiV_{oc} (c) and $\Delta\beta_{iV_{\mathrm{oc}}}$ (f).

and after PDG. Recombination active grain boundaries appear as dark lines in the images and dislocations appear as dark clusters. Figs. G.1(a) and (b) show images of iV_{oc} of the wafer before and after PDG, respectively. In the ungettered state, the intra-grain regions and most grain boundaries are found to exhibit similar material quality. Dislocation clusters appear recombination active in this state, as also reported in Ref. [23]. After PDG, the quality of the intra-grain regions is improved, suggesting that PDG is successful in reducing the concentration of detrimental metallic impurities in these areas. Similar observations have been made in Refs. [22, 26]. The recombination activity of most of the grain boundaries increases with gettering, similar to what has been reported by for example Refs. [22, 23, 37]. The activation and increased recombination strength of grain boundaries during PDG has been suggested to result from metal decoration of the structures causing a change in recombination behavior [24, 37–39]. Dislocations continue to be recombination active after gettering.

To illustrate further the variations in iV_{oc} observed across the wafer, an image of the change in iV_{oc} is created by applying $\Delta iV_{\text{oc}} = iV_{\text{oc}}(\text{gettered}) - iV_{\text{oc}}(\text{ungettered})$ to each pixel. This is shown in Fig. G.1(c). The improvement of the intra-grain regions and the reduced quality of the grain boundaries are clearly visible. Additionally, Fig. G.1(c) illustrates how several dislocation clusters experience increased recombination strength from PDG, similar to observations made in Ref. [23].

Turning our attention to the temperature sensitivity, spatially resolved images of $\beta_{iV_{\text{oc}}}$ are presented in Figs. G.1(d) and (e) for the wafer before and after PDG, respectively. The intra-grain regions and grain boundaries are found to show a similar thermal behavior in the ungettered state. From Fig. G.1(d), features with low temperature sensitivity (bright areas) can be observed across the wafer [see for example ROIs D-F]. Comparing the images of iV_{oc} and $\beta_{iV_{\text{oc}}}$, the bright features can be correlated with dislocation clusters. The relationship between dislocation clusters and low temperature sensitivity has been observed experimentally in recent studies [14, 16, 18–20, 32]; however, note that a region with low iV_{oc} is theoretically expected to show high temperature sensitivity for a constant γ, following Eq. (G.1).

After PDG, the temperature sensitivity of the intra-grain regions is not substantially affected despite of the increase in material quality. This will be assessed further in Sec. G.III.B. The grain boundaries are found to exhibit increased temperature sensitivity after gettering as a result of the direct relationship between material quality and temperature coefficients presented in Eq. (G.1). Features with low temperature sensitivity (bright areas) can be observed across the wafer and correlated with dislocation clusters, similar to the observations in the ungettered state. Since this observation applies both before and after PDG, it suggests that the cause for the low temperature sensitivity is not removed by the gettering process. Although most dislocation clusters show low temperature sensitivity, there are also some that exhibit high temperature sensitivity. This is illustrated by ROIs D-F, highlighted on all images in Fig. G.1. All three dislocation clusters exhibit lower temperature sensitivity compared to the rest of the wafer before gettering [Fig. G.1(d)]. However, after gettering, ROI D displays higher temperature sensitivity, while ROIs E and F remain as low temperature sensitivity regions [Fig. G.1(e)]. Similar observations have been made for non-compensated p-type Si wafers treated by similar gettering and passivation processes [20], suggesting that our results can be generalized to non-compensated mc-Si.

To illustrate further the different responses to gettering across the wafer, a map of the change in $\beta_{iV_{\text{oc}}}$ is created by applying $\Delta\beta_{iV_{\text{oc}}} = \beta_{iV_{\text{oc}}}(\text{gettered}) - \beta_{iV_{\text{oc}}}(\text{ungettered})$ to each pixel, as shown in Fig. G.1(f). Fig. G.1(f) clearly illustrates the increased temperature sensitivity of the grain boundaries and the small altering of the intra-grain regions. Perhaps surprisingly, the dislocation clusters, and even parts of clusters, show very different changes in $\beta_{iV_{\mathrm{oc}}}$. Both relatively large increase and decrease in temperature sensitivity can be observed across the wafer, as indicated by the ROIs D-F. The root cause of this will be investigated further in Secs. G.III.D and G.III.E.

It should be noted that further processing, such as firing and metallization, may have a large impact on the temperature sensitivity due to hydrogenation from the SiN_x and modified lateral conduction in the sample [20]. However, studies have shown beneficial $\beta_{iV_{\mathrm{oc}}}$ values in dislocation clusters both before and after firing and metallization [18, 20].

B. Intra-grain Regions

Fig. G.1 clearly illustrates the varying gettering response of different regions. Additionally, literature has shown that brick position can have a significant impact on the recombination activity of different crystal defects in the as-grown state and, consequently, how they respond to gettering [23, 26]. A detailed investigation of intra-grain regions, grain boundaries, and dislocation clusters, and the position of the wafer in the brick, is therefore presented.

Five intra-grain regions are randomly selected on each wafer following the procedure described in Sec. G.II.C, and the average temperature sensitivity of the different regions is assessed. This is illustrated in Fig. G.2(a) showing the variations in average iV_{oc} at 25 °C in each selected region as a function of the relative brick height before and after gettering. The error bars denote the minimum and maximum average values. The average iV_{oc} is found to increase for most of the wafers as a result of the gettering process, however, this increase is most prominent in the bottom and towards the top of the brick. It suggests that PDG is effective in removing metallic impurities from the intra-grain regions, especially for wafers from these brick locations, similar to observations made in Refs. [22, 26]. This is likely to be caused by the higher concentration of impurities typically found in the bottom and towards the top of a mc-Si brick, thus, enabling more effectful gettering. The higher concentration of impurities is typically a result of segregation during solidification and in-diffusion of impurities from the crucible [40, 41].

Fig. G.2(d) shows average $\beta_{iV_{\mathrm{oc}}}$ values of the selected intra-grain regions as a function of brick height before and after gettering. The variation in average temperature sensitivity on each wafer is found to be relatively small, however, some variations are observed along the brick. There is no clear indication that removing metallic impurities from the intra-grain areas improves the temperature sensitivity.

An illustration of the distribution of $\beta_{iV_{\mathrm{oc}}}$ values in the intra-grain regions before and after gettering is presented in Figs. G.3(a), (d) and (g). It shows $\beta_{iV_{\mathrm{oc}}}$ as a function of iV_{oc} at 25 °C for each pixel in selected intra-grain areas from wafers from the bottom, middle and top of the brick. Lines are inserted in the figure to illustrate the theoretical

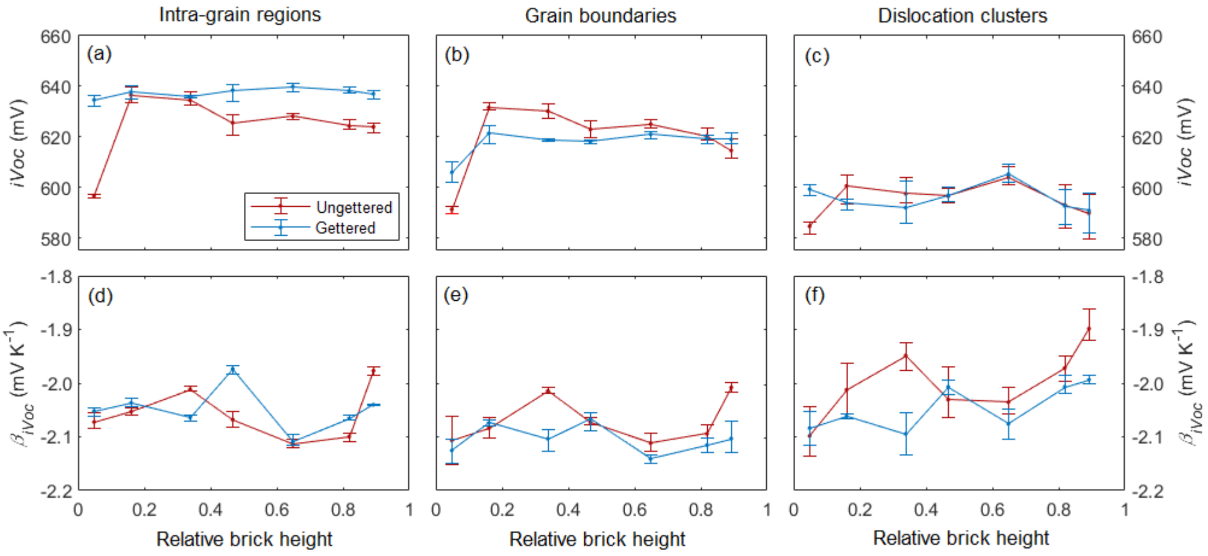

Figure G.2: Average iV_{oc} at 25 °C and $\beta_{iV_{\mathrm{oc}}}$ values of selected intra-grain regions, grain boundaries and dislocation clusters as a function of relative brick height before and after gettering. The error bars denote minimum and maximum average values in the selected areas.

relationship between temperature sensitivity and material quality for constant γ values, calculated from Eq. (G.1). The spread in $\beta_{iV_{\mathrm{oc}}}$ and iV_{oc} within each region is found to be relatively small (note that the number of pixels in each selected area is in the same range as the dislocation clusters for the respective brick positions [500-800 pixels, see Fig. G.3(c) for comparison]. The temperature sensitivity is not substantially affected by the gettering process even though the regions experience increased iV_{oc} values. All intra-grain regions show an increased iV_{oc} as a result of gettering. The shift in $\beta_{iV_{\mathrm{oc}}}$ and iV_{oc} follows the iso-γ line for the middle wafer. The intra-grain regions on the wafers from the bottom and the top of the brick shift towards higher γ values. This difference observed for various brick positions could be caused by the higher concentration of metallic impurities in the bottom and top of the brick, resulting in a more substantial altering of the recombination processes in these regions. Interestingly, all intra-grain regions take values near the same theoretical line given by $\gamma = 3$ after gettering.

C. Grain Boundaries

Figs. G.2(b) and (e) show average values of iV_{oc} at 25 °C and $\beta_{iV_{\mathrm{oc}}}$ of five randomly selected grain boundaries on each wafer as a function of brick height before and after gettering. The average iV_{oc} values are comparable with intra-grain regions before gettering. This is consistent with observations made in Fig. G.1(a) where most grain boundaries and intra-grain areas were found to display similar material quality. After gettering, the

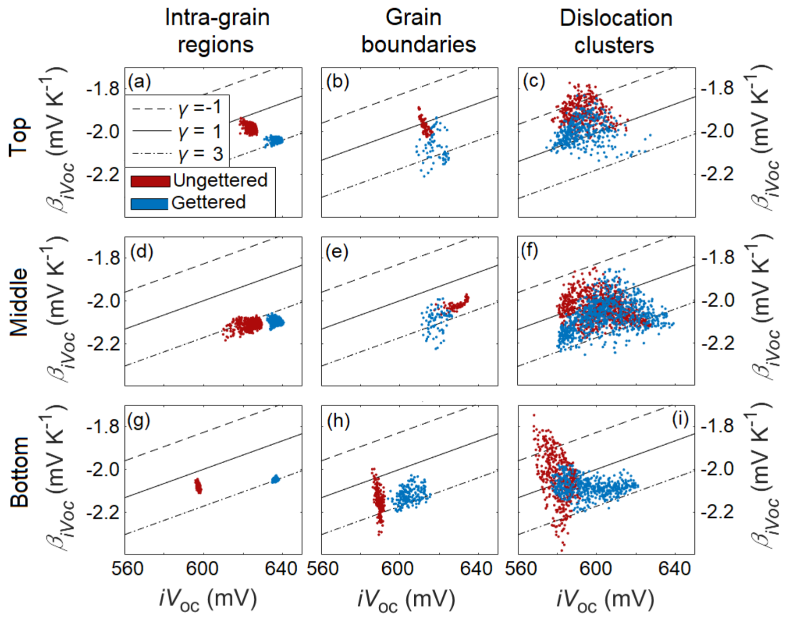

Figure G.3: Pixel resolution of $\beta_{iV_{\mathrm{oc}}}$ as a function of iV_{oc} at 25 °C in an intra-grain region, grain boundary and dislocation cluster from wafers from the bottom, middle, and top of the brick.

average iV_{oc} values of the grain boundaries decrease for wafers from the middle of the brick. The decrease in material quality is likely to result from metal decoration of the grain boundaries [22–24, 37–39]. The bottom wafer experiences an increase in average iV_{oc} after gettering. By assessing the corresponding PL images, the grain boundaries of this wafer were found to be recombination active both in the ungettered and gettered state. Similar observations have been made in Ref. [22] for an industrial HP mc-Si brick. The average $\beta_{iV_{\mathrm{oc}}}$ decreases (more negative) for most brick positions in agreement with the direct relationship between material quality and temperature coefficients for constant γ, presented in Eq. (G.1). The two bottom wafers show no significant change in $\beta_{iV_{\mathrm{oc}}}$ since the grain boundaries are already recombination active in the ungettered state. Comparing to intra-grain regions, the temperature sensitivity of grain boundaries is higher after gettering for most brick positions.

An illustration of the distribution of $\beta_{iV_{\mathrm{oc}}}$ values in the grain boundaries before and after gettering is given in Figs. G.3(b), (e) and (h). They show $\beta_{iV_{\mathrm{oc}}}$ as a function of iV_{oc} at 25 °C for each pixel in selected grain boundaries on wafers from the bottom, middle and top of the brick. The gettering process is found to significantly scatter $\beta_{iV_{\mathrm{oc}}}$ and iV_{oc}. The middle and top wafers show a clear increase in temperature sensitivity and additionally, a shift in γ. The bottom wafer shows relatively high temperature sensitivity both before and after gettering despite of an improvement in iV_{oc}. The gettering response of the grain boundaries varies for the different brick positions; however, it is worth noticing that the gettering process shifts the pixel values towards an iso-γ line with $\gamma = 3$. This observation is similar to the γ values found for intra-grain regions after gettering despite of different $\beta_{iV_{\mathrm{oc}}}$ values found for the two crystal types. This will be discussed further in Sec. G.III.E.

D. Dislocation Clusters

Figs. G.2(c) and (f) show average iV_{oc} at 25 °C and $\beta_{iV_{\mathrm{oc}}}$ values of five randomly selected dislocation clusters as a function of brick height before and after gettering. The spread in average values of both iV_{oc} and $\beta_{iV_{\mathrm{oc}}}$ is considerably larger than for intra-grain regions and grain boundaries. This is consistent with observations from Fig. G.1 illustrating how different dislocation clusters can exhibit significant variations in temperature sensitivity before and after gettering, even across individual wafers. As expected, the average iV_{oc} values are substantially lower than the ones found for both intra-grain regions and grain boundaries before and after gettering, indicating recombination active dislocation clusters in both states. For some clusters and brick positions, iV_{oc} is not significantly influenced by PDG; but the temperature sensitivity increases. It is worth noticing that dislocation clusters show considerably lower average temperature sensitivity towards the top of the brick compared to the intra-grain areas and grain boundaries. This suggests that dislocation clusters from the top of the brick have unique properties which make a temperature increase less detrimental to the performance.

Figs. G.3(c), (f), and (i) illustrate $\beta_{iV_{\mathrm{oc}}}$ as a function of iV_{oc} at 25 °C for each pixel within selected regions on wafers from the bottom, middle, and top of the brick. Each dislocation cluster is found to show a large spread in the values of iV_{oc} and $\beta_{iV_{\mathrm{oc}}}$, both before and after gettering, compared to the intra-grain regions and grain boundaries. Interestingly, some pixels in the dislocation clusters show very low temperature sensitivity compared to the other crystal regions. Additionally, the top wafer clearly shows a lower sensitivity compared to clusters from other brick positions. The distribution of $\beta_{iV_{\mathrm{oc}}}$ values in the selected dislocation clusters is shifted towards higher temperature sensitivity by PDG. The shifts do not follow the theoretical iso-γ lines. It should be stressed that other dislocation clusters might be affected differently by PDG.

From results presented so far, dislocations show a complex response to gettering and a complex thermal behavior. Nonetheless, the regions across the wafers with low temperature sensitivity can still be correlated with dislocation clusters both before and after gettering. It is therefore interesting to investigate further the properties that characterize clusters showing low temperature sensitivity and distinguish them from clusters displaying increased sensitivity. This is done by revisiting Fig. G.1, presenting spatially resolved images of iV_{oc} and $\Delta\beta_{iV_{\mathrm{oc}}}$ for the wafer originating from the middle of the brick. Three ROIs are marked on the wafer (D-F), highlighting three dislocation clusters with different

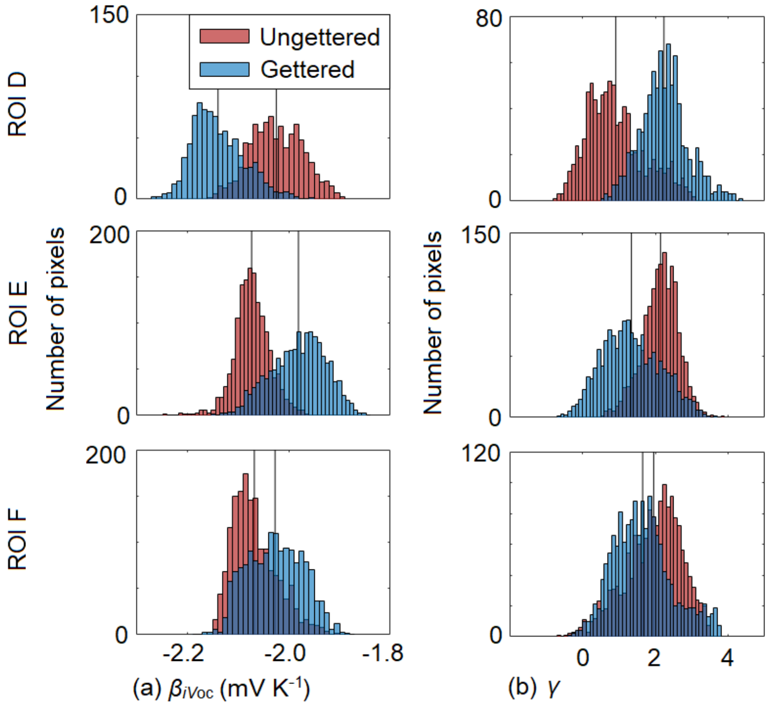

Figure G.4: Distribution of β_{iV_oc} (a) and γ (b) of three dislocation clusters marked by ROIs D-F on Fig. G.1. Average values are indicated by black lines in the histograms.

responses to gettering. ROI D exhibits increased temperature sensitivity after PGD, while ROIs E and F exhibit reduced sensitivity. The actual distributions of β_{iV_oc} and γ values in the clusters before and after gettering are presented in Figs. G.4(a) and (b). Average values are indicated by black lines in the histograms and summarized in Table G.1. All dislocation clusters experience a shift in γ as a result of the gettering process; however, ROIs E and F experience a decrease in γ, where the opposite is observed for ROI D. This implies that the gettering process alters the composition of recombination mechanisms in the clusters, but in various ways depending on the cluster type. From Eq. (G.1), a high γ value contributes to increasing the temperature sensitivity and vice versa. The limiting recombination mechanism therefore becomes more temperature sensitive for ROI D and less sensitive for ROIs E and F as a result of PDG. The physical implications of an increase and decrease in γ will be discussed further in Sec. G.III.E. It is worth noticing that even though some dislocation clusters become more temperature sensitive after gettering, as illustrated in blue in Fig. G.1(e), the temperature sensitivity can still be lower compared to other crystal areas on the wafer.

E. Mapping of Limiting Recombination Mechanisms

Figs. G.1-G.4 illustrate how variations in temperature sensitivity can be observed across wafers and for different brick positions. The temperature sensitivity depends on several

Table G.1: Average γ values of ROIs D-F on a wafer from the middle of the brick before and after gettering.

Processing	ROI D	ROI E	ROI F
Ungettered	0.91	2.14	1.95
Gettered	2.24	1.34	1.65

factors as described in Eq. (G.1), but the material dependent variability is captured by the parameters iV_{oc} and γ. In order to understand the underlaying mechanisms causing varying temperature sensitivity, the γ parameter is assessed in further detail.

To correlate actual γ values with physical quantities, we make the following observations: First, Eq. (G.1) indicates that a low γ value will contribute to lowering the temperature sensitivity, and vice versa. Secondly, we make use of Ref. [4], where Dupré *et al.* compute γ values for different scenarios. These values should not be understood as limits, but as reference points for interpretation. The authors suggest $\gamma \approx 3$ for a material which is limited by SRH recombination in the bulk and at the surface and with carrier lifetime and surface recombination velocities assumed to be independent of temperature. This implies that, for a material which is limited by SRH recombination in the bulk and at the surface, $\gamma < 3$ is equivalent to an effective SRH lifetime that increases with increasing temperature. The actual γ value can then be related to the rate by which the lifetime is increasing. This rate is determined by the energy level of the defect states (E_{t}) and the capture cross sections of electrons (σ_n) and holes (σ_p) [42–44]. It should be noted that other parameters, such as injection level, could influence as well.

Spatially resolved images of γ for wafers from the bottom, middle, and top of the brick are shown before gettering [Figs. G.5(b), (f), and (j)] and after gettering [Figs. G.5(c), (g) and (k)]. Note that a non-uniformity can be observed in the bottom right corner of Fig. G.5(j) originating from a slight non-uniform temperature encountered during the measurement of the ungettered wafer at 70 °C (it should be stressed that this has not been observed for other measurements). The non-uniformity was found to be localized and only the unaffected part of the wafer is used for analysis. Large variations in γ are found across the wafers, especially noticeable for the middle and top wafers. If comparing with corresponding iV_{oc} images [Figs. G.5(a), (e), and (i)], the various crystal regions can be correlated to γ values. Intra-grain regions exhibit a relatively uniform γ value across individual wafers and take a common value around $\gamma = 3$ after gettering, similar to observations from Fig. G.3. Following our previous discussion, this γ value implies that the intra-grain regions are limited by SRH recombination centers with an effective lifetime that is independent of temperature or has a modest temperature sensitivity in the studied temperature range. Such a temperature dependence characterizes, for example,

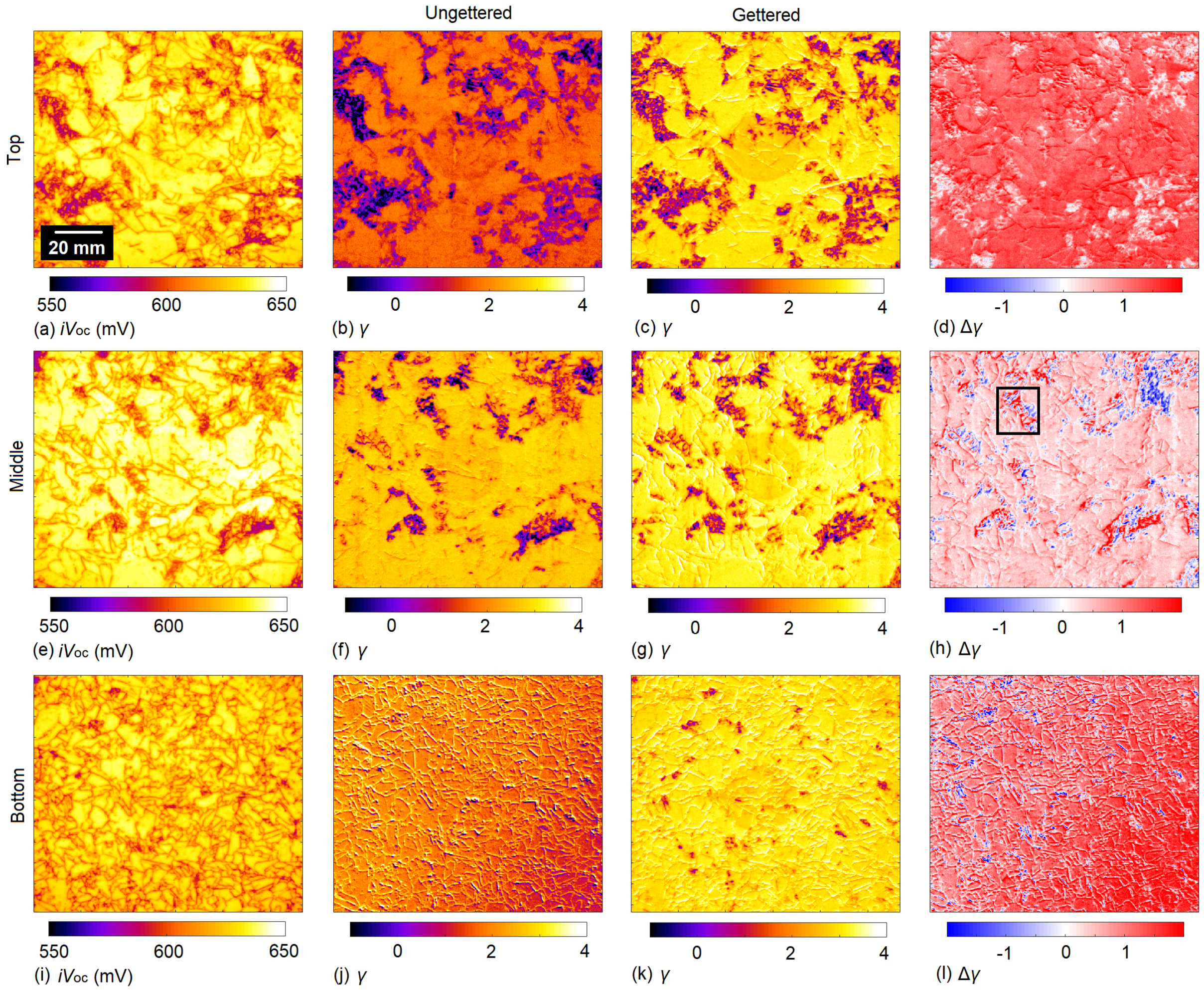

Figure G.5: Images of iV_{oc} at 25 °C after gettering, γ before and after gettering, and $\Delta\gamma$ for wafers from (a-d) the top, (e-h) middle, and (i-l) bottom of the brick.

interstitial iron [18,45,46] suggesting that this SRH center could be limiting the intra-grain regions.

Grain boundaries cannot easily be distinguished from intra-grain regions in the ungettered nor gettered states, except for the bottom wafer. This suggests that grain boundaries and intra-grain regions are limited by the same type of recombination in the middle and top wafers, or by different SRH centers resulting in a similar temperature dependence. Grain boundaries have been observed to show a higher concentration of iron after gettering [24], supporting this hypothesis. Note however, that the intra-grain regions and grain boundaries show very different iV_{oc} and $\beta_{iV_{\mathrm{oc}}}$ values after gettering [see Figs. G.2(a) and (b)] indicating different characteristics of the limiting recombination mechanism at the two locations. One possible explanation could be that the two crystallographic groups contain different concentrations of the same SRH center. The visibility of the grain boundaries in the bottom wafer before gettering indicates that this case is characterized by different types of recombination compared to the other wafers in the ungettered state. The γ parameter could be influenced by in-diffused impurities from the crucible during solidification. This hypothesis is supported by the very low iV_{oc} values encountered for this wafer.

Features with low, and in some cases negative, γ values can be observed across both the ungettered and gettered wafers and correlated with dislocation clusters when compared with the iV_{oc} images. The low γ values observed in dislocation clusters indicate that the clusters contain SRH centers with an effective lifetime that has an especially beneficial temperature sensitivity. Examples of such SRH centers could be copper [47], aluminum [48], molybdenum [45, 49], titanium [50] and chromium-related defects [18, 51].

To illustrate more clearly how PDG affects the various crystal regions, images of $\Delta\gamma$ are calculated by applying $\Delta\gamma = \gamma(\text{gettered}) - \gamma(\text{ungettered})$ to each pixel. Local variations in γ indicate a change in the limiting recombination type caused by a local redistribution of recombination centers. For $\Delta\gamma < 0$, the redistribution results in a combined recombination rate which becomes less temperature sensitive, and vice versa. Images of $\Delta\gamma$ of wafers from the top, middle, and bottom of the brick can be seen in Figs. G.5(d), (h), and (l). It is clearly visible that γ of intra-grain regions is increased by PDG for all the wafers, however, only a modest change is observed for the middle wafer. The common reaction to PDG by the bottom and top wafer could be caused by the higher concentration of impurities present in these parts of the brick before gettering as a result of in-diffusion from the crucible in the bottom of the brick and segregation of impurities towards the top of the brick. Since the wafers exhibit $\Delta\gamma > 0$, the lifetime of the impurities which are removed by the gettering process have a lower temperature sensitivity than the ones remaining. Dislocation clusters mainly exhibit $\Delta\gamma < 0$; however, some clusters show both a high increase and decrease in γ [see the ROI marked in Fig. G.5(h) as an example]. The variation in γ indicates a rearrangement of recombination centers in clusters. For most dislocation clusters, this rearrangement results in limiting recombination centers yielding a more beneficial temperature sensitivity.

The reduced temperature sensitivity found for most dislocation clusters, compared to intra-grain areas and grain boundaries, indicates that the presence of dislocation clusters may contribute to a beneficial temperature sensitivity of the overall cell performance. Hence, despite their detrimental effect on cell performance, the presence of dislocation clusters might have less harmful effects when the operating temperatures are high.

G.IV. Summary

The temperature sensitivity of crystallographic defects in mc-Si wafers has been investigated. Spatially resolved temperature dependent analysis has been performed on mc-Si wafers from different brick positions; and intra-grain regions, grain boundaries, and dislocation clusters were examined before and after subjecting the wafers to a phosphorus diffusion gettering. Both intra-grain regions and grain boundaries were found to show similar thermal characteristics before gettering. The gettering process had no substantial effect on the temperature sensitivity of intra-grain regions but increased the sensitivity of most grain boundaries. Dislocation clusters were observed to exhibit both highest and lowest temperature sensitivity compared to other crystal regions.

Images of the recombination parameter γ were created and related to the temperature sensitivity of the local effective lifetime of the SRH centers in the material. The results suggest that most intra-grain regions and grain boundaries are limited by SRH centers with a modest lifetime temperature sensitivity in the studied temperature range such as interstitial iron. Dislocation clusters were found to contain SRH centers with an effective lifetime that has a beneficial temperature sensitivity. The gettering process was found to alter the composition of recombination centers in the clusters, resulting in a SRH lifetime with a more favorable temperature sensitivity for most clusters.

Acknowledgments

This work was supported by the Australian Government through Australian Renewable Energy Agency (ARENA; project 2017/RND001). The views expressed herein are not necessarily the views of the Australian Government, and the Australian Government does not accept responsibility for any information or advice contained herein. The authors thank the Solar Industry Research Facility (SIRF) team at UNSW for samples fabrication.

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Paper H

Improved temperature coefficient modeling through the recombination parameter γ

Submitted as:

S. T. Kristensen, A. S. Garcia, S. Nie, Z. Hameiri, and R. Strandberg, "Improved temperature coefficient modeling through the recombination parameter γ", in: *Proceedings of the 47th IEEE Photovoltaic Specialists Conference*, *in press*, 2020.