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PSIM-Based Hardware and Software Design of an Inverter-Fed Permanent Magnet Synchronous Motor

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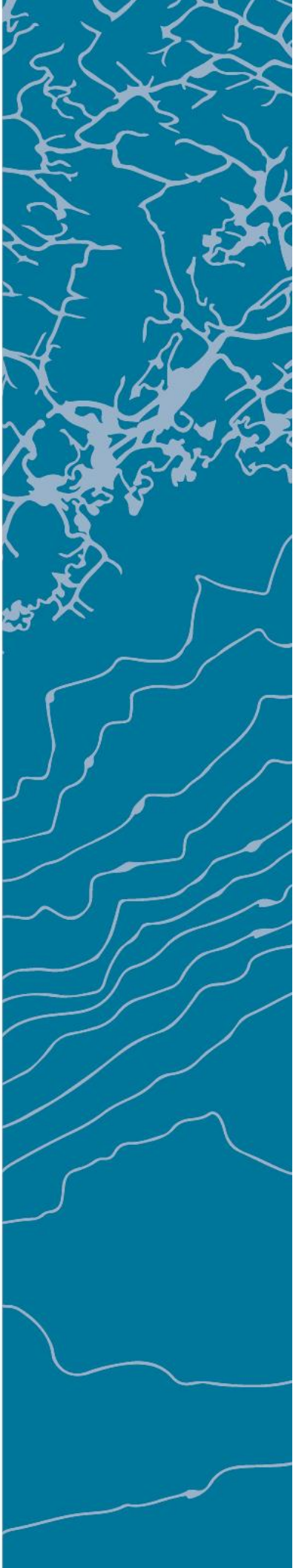

Abstract

The purpose of this research is to design a PSIM based controller for an inverter-fed Permanent Magnet Synchronous Motor (PMSM). The dimensioning and assembly of the controller are presented. The control algorithm used for the PMSM is Field Oriented Control (FOC). The report includes the theory of the control algorithm and its design. A PSIM based model is designed with the dimensioned components to analyse the behaviour of the controller. The model gives the opportunity of tuning the controller and verifying it with simulations. The model is then converted to be SimCoder compatible, enabling the simulation to be generated into a code. A Digital Signal Processing (DSP) development board is provided by Powersim Inc. The generated code is imported to the DSP, enabling it to run the controller. Similar behaviour is observed when comparing the test results with the simulations. When simulating the controller with the PMSM, all reference speeds are reached with a maximum deviation of $\pm 0.42\%$. Using PSIM proved to be an intuitive and educational way of designing the motor controller.

Preface

For this master's thesis, we would like to express our greatest gratitude to van Khang Huynh for his knowledge, time, guidance, and assistance. We would also like to thank Milad Golzar and Flekkefjord Elektro AS for their guidance and time in the field of electronics and components dimensioning. A special thanks to Steve Schading and Karl-Berge Rød for providing us with the necessary equipment, technical information, and assistance for this project.

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1 Introduction

Permanent Magnet Synchronous Motors (PMSMs) have been widely used in traction, robotics, and automotive applications due to the advancements and price drop of permanent magnet (PM) materials [1]. Furthermore, it is effective in renewable energy applications such as wind turbines [2] and fuel cell vehicles [3]. PMSMs are starting to make an appearance in Full Electrical Vehicles (FEVs). The United States Environmental Protection Agency (EPA) reports that Tesla model 3 is using PMSMs instead of induction motors [4]. Some of the advantages of such changes in FEVs include a higher range of efficiency, high torque and power per volume, compact design, and low maintenance cost [5]. In general, the PM technology of the motor results in a smooth torque production, which makes it suitable in high-performance applications [6].

Power electronics play a significant role in the performance of electric motors. Advances in power semiconductor devices, converter topologies, simulation methods, and control technologies have led to substantial progress in power electronics in recent years [7]. Control technologies play a particularly big role regarding AC drives. Vector control or Field Oriented Control (FOC) is one of the essential innovations in AC motors which makes it possible to enhance control performance further [8]. According to Bose, applications such as machine tools, servos, robotics and transportation drives are using the control method. He also states that FOC will be universal for electric drives in the future [7].

This thesis describes a software and hardware controller design of an inverter-fed PMSM. This includes dimensioning, purchasing and assembling the necessary electrical components of the control design. The thesis presents the simulation design needed for verification, and the control algorithm needed to run the PMSM. The control algorithm is converted into a code which is imported into a Digital Signal Processor (DSP). This makes it possible to run the control system through the DSP.

1.1 Motivation

The purpose of this work is to find a convenient and intuitive way of designing and running a PMSM. PSIM is a simulation software specifically designed for electric drives and power electronics and has been proven effective for research purposes. Both Sira-Ramírez and Donsión uses the software to verify their control schemes [9] [10]. Furthermore, PSIM is able to run motors with its SimCoder module coupled with DSP boards. Morkoç et al. implements this method to run a PMSM with a controller designed in PSIM and imported into a High Voltage Motor Control-PFC Kit [11]. Similar software is provided by Opal-Rt Technologies and Dspace, both of which is used for academic and commercial use. However, the software is in a higher price range than PSIM. In addition, PSIM introduces a more educational approach for the control design with the DSP development board and open system design, as opposed to the more fully assembled controllers provided by Opal-Rt and dSpace.

PSIM seems to be a good choice for designing and learning the theory of a motor controller due to its educational approach in the software design and low price. This research investigates the use of PSIM further by designing a PSIM based PMSM controller and importing it into a DSP development board, both provided by Powersim Inc. Furthermore, the hardware of the controller is designed from the ground up as

opposed to purchasing it fully assembled. This makes it possible to to study and learn the principles of the controller while building it.

1.2 Problem Statement

The purpose of this thesis is to design a PSIM based controller of an inverter-fed PMSM and investigate its behaviour. The main focus will be on power electronics, simulation, and control theory. The project outputs and requirements are summarised below.

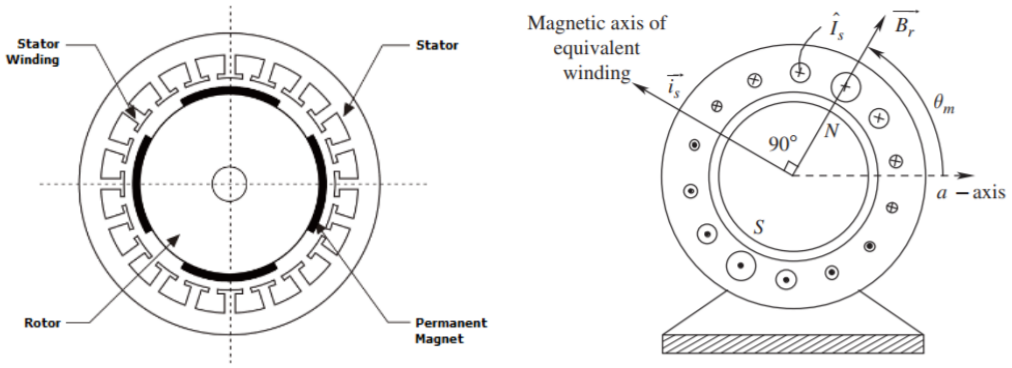
1. Determine the dimensions of the electric components needed to build a frequency converter by using data sheets and simulation. The converter should be able to run a 2 kW PMSM. Compare the simulation results with the rated values of the PMSM to verify the components before purchase.
2. Create a PSIM based model of the frequency converter and the FOC design. Implement all the selected components in the model and tune the controller to run the PMSM.
3. Convert the model to make it compatible with SimCoder. In SimCoder, use the code generation function to obtain the code needed to run the control algorithm.
4. Assemble the dimensioned components. This includes the design of Printed Circuit Boards (PCBs) and soldering the necessary electronic components on the PCBs and veroboards.
5. Import the code into Code Composer Studio (CCS) to run the frequency converter through the DSP development board.
6. Run the selected Frequency converter with the designed controller through the DSP development board. Investigate the signals of the hardware and compare them with the simulation results.

1.3 Report Outline

The structure of the thesis is as follows. Section 2 presents an overview of the theory and behaviour of the motor. In addition, it addresses and discusses the different PMSMs and some of the control theories. Section 3 presents the choice of components for the frequency converter. Section 4 discusses PSIM based model of the frequency converter and its control algorithm. Also, it describes the FOC theory along with the PSIM based model to get a better understanding of the correlation between theory and simulation. Section 5 shows the SimCoder conversion, while Section 6 describes the DSP development board and the necessary software needed to run the hardware. Section 7 presents the hardware and test setups. Section 8 shows the results of the thesis and Section 9 discusses the results. Finally, Section 10 presents a conclusion for the report.

2 Permanent Magnet Synchronous Motor

Figure 1(a) shows the cross-section of a PMSM and illustrates the rotor, stator, permanent magnets, and stator windings. The permanent magnets and windings are on the rotor and the stator respectively. The illustration in Figure 1(b) shows a two pole PMSM.



(a) Main Components (b) Windings and Magnetic Axis

Figure 1: PMSM Illustration [12] [6]

The motor torque of the motor is generated as a result of the relation between the magnetic field in the stator windings and the permanent magnets. The motor will generate maximum torque when the angle between the magnetic fields is 90°. Figure 1(b) illustrates this. The space vectors of the magnets on the rotor $\vec{B}_r$ and the stator winding current $\vec{i_s}$ are perpendicular to each other. The space vectors represent the peak of the magnetic field distribution and its position [6]. The windings in which the current $\hat{I}_s$ is flowing through are sinusoidal distributed. θ_m indicates the angle of the rotor flux density $\vec{B}_r$ with respect to the a-axis. When the windings are as illustrated in Figure 1(b), the rotor will run in a counterclockwise direction. The mathematical expression of $\vec{i_s}$ is shown in (1) and (2) [6].

$$\vec{i_s}(t) = \hat{I}_s(t) \angle \theta_{i_s}(t) \tag{1}$$

where:

$$\theta_{i_s}(t) = \theta_m(t) + 90° \tag{2}$$

The motor generates maximum torque when $\vec{i_s}$ is (leading) perpendicular to $\vec{B}_r$. Regulating the $\vec{i_s}$ to maintain the 90° lead to $\vec{B}_r$ makes it possible to control the torque of the motor [6].

2.1 Permanent Magnet Motors Overview

Figure 2 shows an overview of permanent magnet machines. The two main permanent magnet electric machines are Permanent Magnet DC (PMDC) and Permanent Magnet AC (PMAC) machines. The PMDC

machines are conventional DC commutator machines where permanent magnets replaces the field windings. As a result, the commutator and brushes and its surrounding problems (brush wear and high inertia) still apply [13].

The PMAC machine operates without both the commutator and the brushes and thus removing its challenges. They are synchronous machines which means that the AC excitation frequency is synchronous with the rotational speed. The difference between the trapezoidal type (Brushless DC (BLDC) motor) and the sinusoidal type (PMSM motor) is the stator winding distribution. In the trapezoidal type, the back-EMF voltage waveform will be trapezoidal. Similarly, the Sinusoidal type back-EMF will have a sinusoidal waveform. BLDC motors are easily controlled. However, the present torque ripples of the motors make it inadequate for high-performance applications [13].

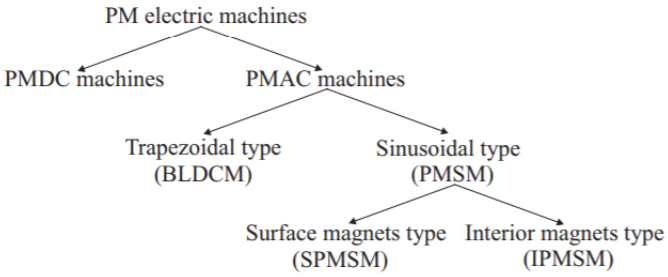


Figure 2: Permanent Magnet Motors [13]

Figure 3 shows two types of PMSMs. The Surface Permanent Magnet Synchronous Motor (SPMSM), where the magnets are at the surface of the rotor and the Interior Permanent Magnet Synchronous motor (IPMSM) where the magnets are inside the rotor [13]. IPMSMs are usually used in wide speed range applications. The SPMSMs are typically used for for constant speed and servo applications systems [14] [15] [16].

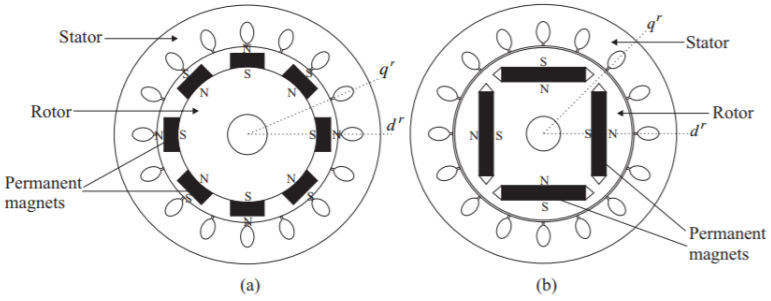


Figure 3: SPMSM (a) and IPMSM (b)

2.1.1 Induction Motor Comparison

Induction motors are known as the "workhorses" of the industry and are the most used electrical machines [17]. There is, however, a trend shift in motor usage. The absence of rotor windings in PMSMs make it

more efficient than induction motors due to the reduction of copper loss. In addition, it is possible to design PMSMs with lower weight and volume compared to the induction motors. Furthermore, the high torque to inertia ratio makes it more suitable for high-performance applications [13]. One of the drawbacks of the PMSM motor has been the need of Variable Frequency Drives (VFD) to control the motor. VFDs are often used to increase the efficiency in induction motors [18]. Up until this point, the complex control system and VFD requirements prevented the use of PMSM in some applications. That said, new VFDs are available with inbuilt controllers as a standard feature, making it more attractive for use in industry [18].

2.2 PMSM Control Methods

V/f control and FOC are the main techniques applied for speed control in PMSM [13]. This section presents a brief explanation and discussion of the two methods.

2.2.1 V/f Control

Figure 4 shows the system diagram of V/f control. The main purpose of the technique is to control the frequency and the voltage of the PMSM simultaneously. The input frequency will regulate the speed. However, the change of frequency results in impedance change, which can lead to a decrease or increase of current and damage the PMSM. Regulating the voltage and frequency at the same time to maintain a constant ratio avoids such complications [19][20].

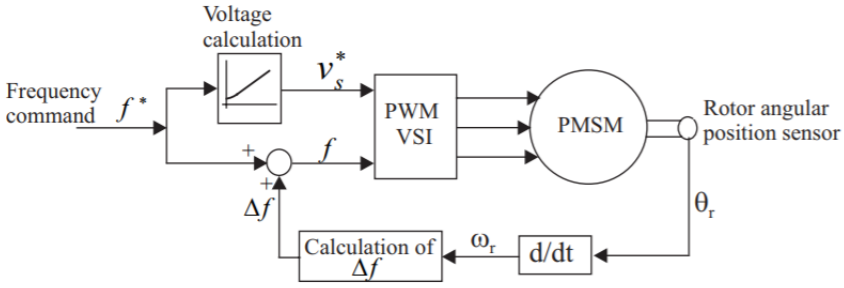


Figure 4: V/f Control System

The ratio between the voltage and frequency are expressed in (3).

$$\frac{V}{f} = k = \text{Constant} \tag{3}$$

where:

V = Input PMSM voltage $[V]$

f = Input PMSM frequency $[Hz]$

k = Voltage to frequency ratio $[\frac{V}{Hz}]$

A closed-loop system is necessary for the PMSM to be synchronous at all time. Obtaining the rotor position of the PMSM will lead to synchronisation between AC excitation frequency and rotor frequency [13]. The position of the rotor θ_r is differentiated to obtain the speed of the motor. Furthermore, a comparison between the calculated motor frequency Δf and the reference frequency signal $f*$ makes it possible to adjust the frequency f and the voltage V_s*. The Pulse Width Modulation (PWM) and Voltage Source Inversion (VSI) generate the signals.

2.2.2 Field Oriented Control

Figure 5 shows a FOC design. FOC is a more complex control method with a more mathematical based approach than the V/f control. The controller uses current feedback and transformation techniques to control the torque of the PMSM [13]. The speed controller generates the torque demand T_e* which is sent to the torque controller. The torque controller uses its input to generate output voltage signals $V_{qs}^{s^*}$ and $V_{ds}^{s^*}$ which are processed further in the PWM and VSI. As a result, the PMSM input signals are a regulated three-phase current with a desired frequency. The measured phase currents i_{as} and i_{bs} are feedback for the torque controller. Also, the rotor angular position θ_r is measured and implemented in the torque controller. The motor speed feedback ω_r is the derivative of the measured angular position. The speed is compared with the desired speed ω_r* and sent into the speed controller. The torque controller includes a current controller and reference frame transformations which are explained more detailed in Section 4.4.

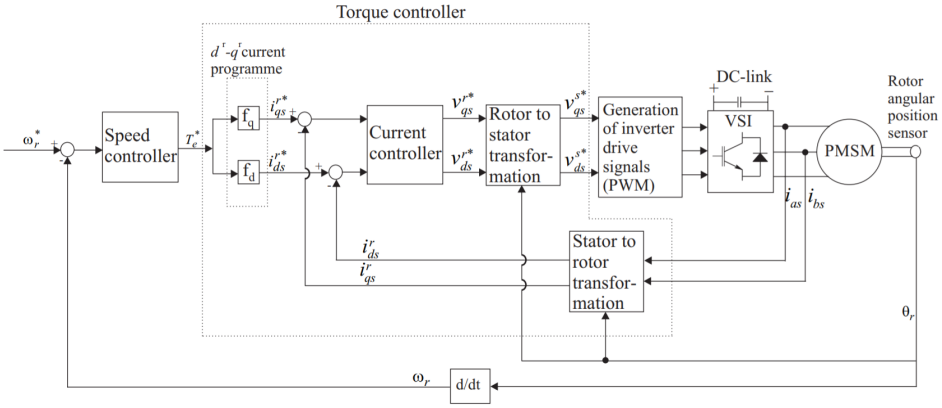


Figure 5: Field Oriented Control

Each control method has its preferred field of application. The simplicity, low cost and stability of the V/f method makes it attractive to the industry for low-performance applications such as pumps and fans. In contrast to V/f control, FOC is able to control electric drives with dynamic behaviour due to its current control. As a result, motors in high-performance applications typically uses FOC [19].

3 Choice of Components

This section describes the frequency converter hardware. Furthermore, it describes the considerations and methods taken into account in the dimensioning process. Figure 6 shows an overview over the design. A three-phase power supplies the frequency converter (1). The rectifier (2) converts the AC power into to DC power. The filter (3) are implemented smoothen the DC power. The inverter (4) will convert the DC power back to AC power. However, the PSIM based control design (5) which is imported into the DSP (6) regulates the frequency of the inverter output power through the gate driver (7). Measuring the input current (8) and speed of the motor (9) is required for the controller to work. The change in frequency in the inverter output voltage results in a change of speed in the motor (10).

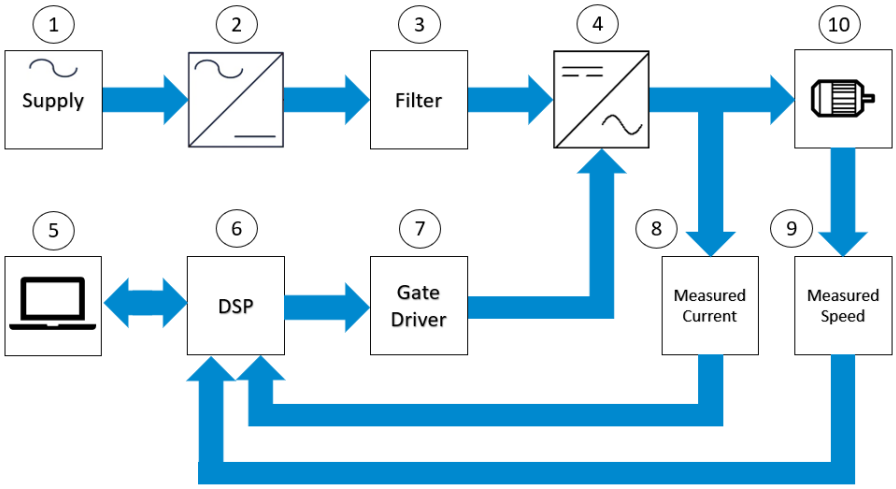


Figure 6: Block Diagram of the System

3.1 Rectifier

The rectifier converts the AC voltage into DC voltage. Figure 7 shows the rectifier. The maximum voltage and maximum current of the rectifier were taken into account when dimensioning the component. The data sheet of the rectifier is available in [A.1].

Figure 7: Rectifier [21]

3.2 Filter

Figure 8 shows the simulation designed for filter dimensioning. The capacitor and inductor attenuates the output signal of the rectifier. The capacitor will reduce the voltage ripple and the inductance will smoothen the current from the rectifier. The design includes a three-phase voltage source AC_source, rectifier, resistance R, inductor L, and capacitor C. The 100 Ω, 0.1 μF snubber limits $\frac{dv}{dt}$ and $\frac{di}{dt}$, to protect the components [22].

The DC bus capacitor C initially has no voltage across it. Therefore, the instant the voltage source is applied to the system, a large current flows through rectifier to charge the capacitor [23]. This current is referred to as Inrush Current Peak (ICP). A 10 Ω Negative Temperature Coefficient (NTC) thermistors R_NTC is implemented to reduce the ICP. The current probe, voltage sensor, and voltage probe measures the results of the simulation.

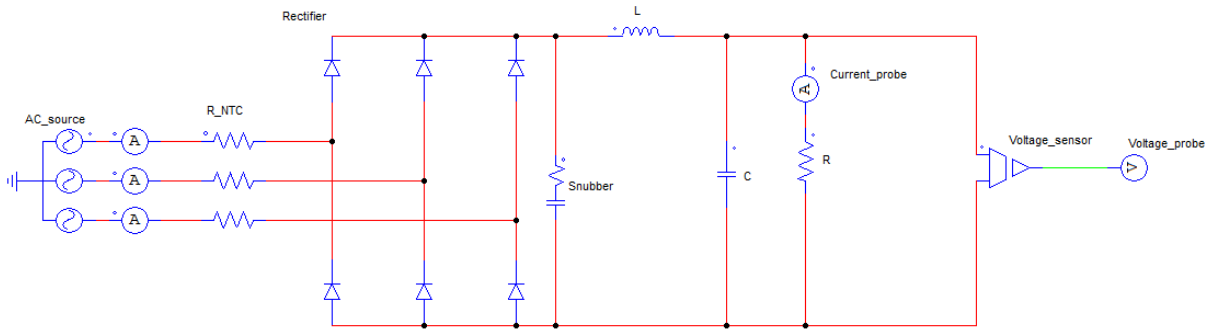


Figure 8: Filter Test Circuit

The voltage and current ripple of the filter based on the simulation results are calculated with (4) [24].

$$\text{Percentage of voltage ripple} = \frac{\text{rms value of ripple}}{\text{Average DC output}} \cdot 100 = \frac{sin(45°) \cdot \frac{V_{max} - V_{min}}{2}}{V_o} \cdot 100 \tag{4}$$

where:

V_{max} = Maximum output voltage [V]

V_{min} = Minimum output voltage [V]

V_o = Average output voltage [V]

The 3900 μH inductor in the simulation design smoothens the current. Table 1 shows the results of the simulations completed to determine the capacitor values. The NTC thermistors are not active at this stage.

Simulation	Capacitor [μF]	Inductor [μH]	Voltage Ripple [%]	ICP [A]
1	200	3900	1.99	116.37
2	600	3900	0.60	210.18
3	1000	3900	0.34	276.97

Table 1: Simulation Results

The results illustrate the correlation between the capacitance, voltage ripple, and the ICP. The higher the capacitance, the lower voltage ripple. However, the ICP increases with the capacitance. A capacitance of 1000 μF is selected further due to its low voltage ripple.

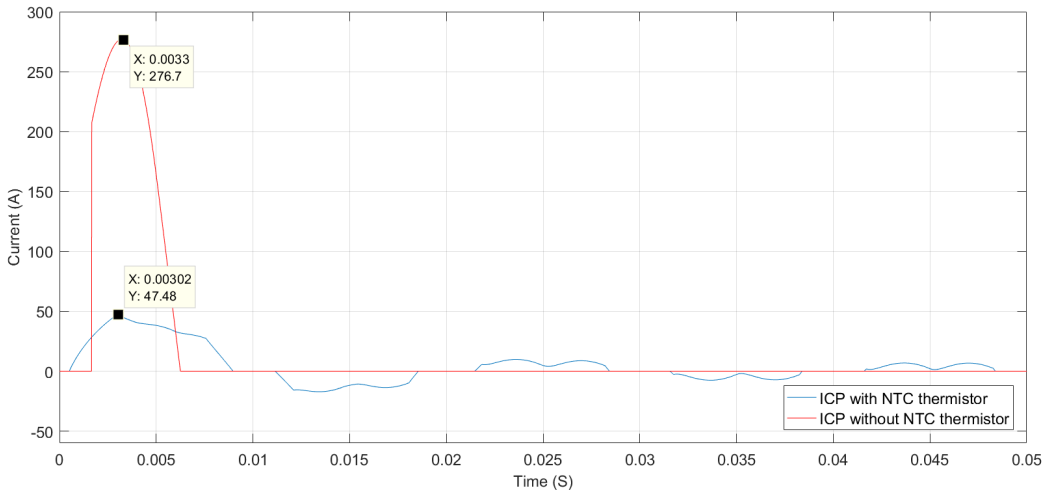


Figure 9: ICP with and without NTC Thermistors

Figure 9 illustrates the effect of the implemented NTC thermistors. The NTCs reduces the ICP from 276.7 A to 47.48 A in addition to removing the output voltage peak of 1081 V entirely. Furthermore, it reduces the time to reach steady state condition. Figure 10 shows the voltage behaviour with and without the NTCs.

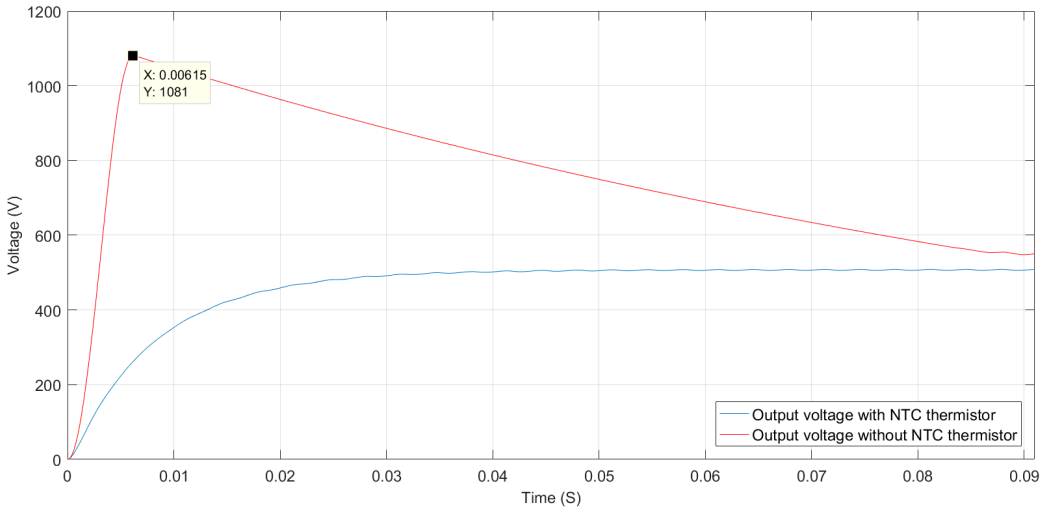


Figure 10: Output Voltage with and without NTC Thermistors

The resistance of the NTC thermistor will decrease as the temperature rise. As a result, the thermistor will have a constant high temperature when running the motor for a longer period of time, which will lead to a power loss. Implementation of a bypass circuit for the NTC thermistor avoids this power loss. Figure 11 shows the bypass circuit. When current flows through the relay coil, the current will go from Re_A to Re_B, which will bypass the NTC thermistor. A 12 V supply is connected to the circuit. The relay will activate the bypass circuit when current flows through the coil. However, no current flows through until the NPN transistor is active. The NTC bypass relay signal activates the transistor and thus letting current flow through the coil. This activates the bypass circuit. The resistors R1, R2 and R3 adjusts the current flowing through the circuit.

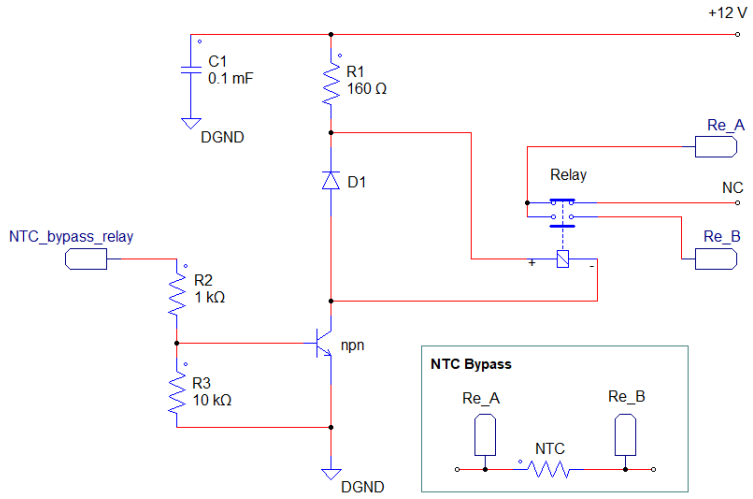


Figure 11: Relay Bypass Circuit

3.3 Inverter and Gate Driver

Figure 12 shows a typical inverter. The selected Insulated-Gate Bipolar Transistor (IGBT) inverter is able to handle higher voltage and power ratings than the MOSFET transistor [6]. The implemented gate driver shown in Figure 13 is able to operate the IGBTs from the control board. In addition, the gate driver is in the same gate driver-family as recommended by Infineon [25]. The data sheets for the inverter and gate driver are shown in [A.4] and [A.5].

Figure 12: Inverter [25]

Figure 13: Gate Driver for the Inverter [26]

An integrated bootstrap circuit is needed in the gate driver to run the high IGBT. Figure 14 shows a bootstrap circuit. Figure 15 illustrates the collector, gate, and emitter on an IGBT. The gate terminal voltage needs to be positive with respect to the emitter to open an IGBT. Considering that the low IGBT $M2$ and the low voltage supply is referenced to the same ground, the gate terminal voltage will be positive with respect to the emitter on the low IGBT. However, this is not always the case with the high IGBT $M1$. When $M2$ is open and $M1$ is closed, the emitter voltage point may be floating and not referenced to the system ground. To take this into account, a bootstrap circuit is implemented. The bootstrap diode D conducts and charges the capacitor C when $M2$ is open and $M1$ closed. C will charge up to approximately the low voltage supply potential. When $M1$ is open and $M2$ closed, the high side circuitry will be supplied by C, ensuring that the gate terminal voltage will be positive with respect to the emitter [27].

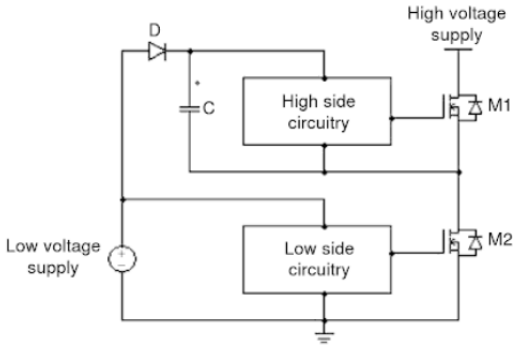


Figure 14: Bootstrap Circuit [27]

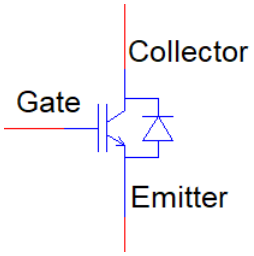


Figure 15: IGBT Illustration

3.4 Cooling Element

Under switching conditions, the inverter may reach temperatures up to 150°C. In addition, the temperature under the maximum current condition is 175°C. Such high temperatures will cause a power dissipation of 50 W on the inverter [A.4].

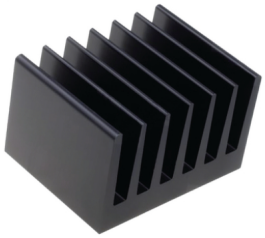


Figure 16: Cooling Element for the Inverter [28]

Mounting a cooling element on the inverter reduces power dissipation. Figure 16 shows the selected cooling element. The thermal resistance of the element is 1.5 $\frac{K}{W}$, meaning that a power dissipation of 50 W will heat the cooling element up to 75°C [28]. The calculation are shown in (5).

$$1.5\ \frac{K}{W} \cdot 50\ W = 1.5\ \frac{^{\circ}C}{W} \cdot 50\ W = 75^{\circ}C \tag{5}$$

3.5 Current Sensors

Measuring the current going into the PMSM is crucial for controlling purposes. The frequency converter includes two current sensors. The control design calculates the current of the third phase current. The sensors has a nominal current of 6 A. However, they generate a proportional voltage of $2.5 \pm 0.625\ V$ as an output signal. The current sensor needs to be calibrated to take this into account. Figure 17 shows the selected sensor.

Figure 17: Current Sensor [29]

3.6 Hardware Setup

Table 2 shows the selected hardware parameters. Note that the data sheets defines the voltage as VDC, VAC, or V. The table presents the parameters the same way as the data sheets. The inductor, capacitor, and Negative Temperature Coefficient (NTC) thermistor are dimensioned with the help of PSIM simulations. The remaining parameters are obtained from the data sheets.

Component	$\mathbf{V_{max,c}}$	$\mathbf{V_{max,p}}$	$\mathbf{I_{max,c}}$	$\mathbf{I_{max,p}}$	$\mathbf{I_n}$	**L**	**C**	$\mathbf{R_e}$	$\mathbf{R_t}$
Rectifier	600	725	25	360	-	-	-	-	-
Inductor	760	-	8	-	-	3.9	-	-	-
Capacitor	400	440	3.38	-	-	-	1000	-	-
Inverter	600	-	10	20	-	-	-	-	-
Gate Driver	600	-	-	-	-	-	-	-	-
Cooling Element	-	-	-	-	-	-	-	-	1.5
Current Sensor	600	-	-	-	6	-	-	-	-
Snubber	1000	-	12	20	-	-	0.1	100	-
NTC Thermistor	-	-	-	-	-	-	-	10	-

Table 2: Components for the Frequency Converter [A]

where:

$V_{max,c}$ = Maximum continuous voltage $[V]$

$V_{max,p}$ = Maximum peak voltage $[V]$

$I_{max,c}$ = Maximum continuous current $[A]$

$I_{max,p}$ = Maximum peak current $[A]$

I_n = Nominal current $[A]$

L = Inductance $[mH]$

C = Capacitance $[\mu F]$

R_e = Electrical resistance $[\Omega]$

R_t = Thermal resistance $[\frac{K}{W}]$

4 Simulation Design

This section introduces the simulation design of the frequency converter. In addition, it describes the simulation process and the function of the components.

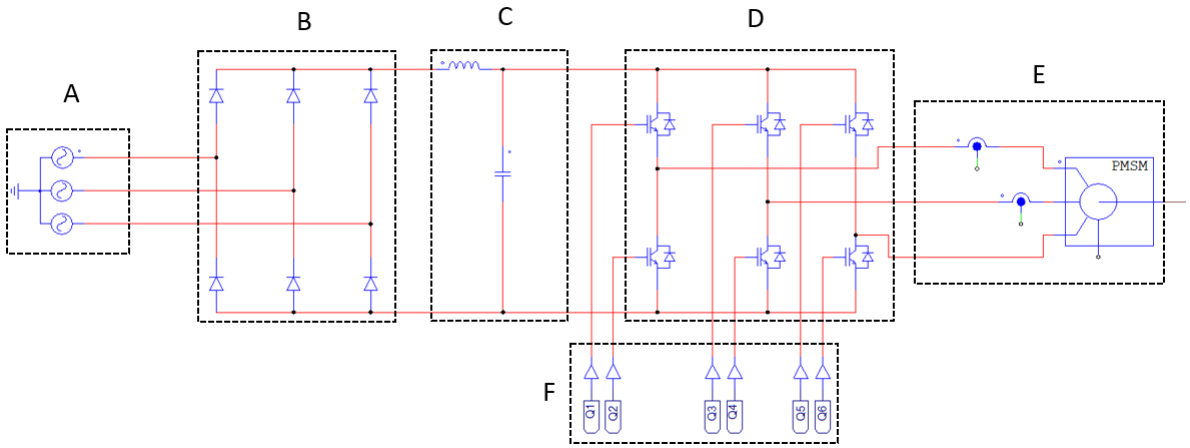


Figure 18: Overview of Frequency Converter

Figure 18 shows an overview of a frequency converter. A three-phase AC power source (A) supplies the converter. The rectifier (B) converts the voltage from AC to DC. Furthermore, the inductor and capacitor attenuates the voltage (C). The inverter (D) uses six IGBTs to convert the DC signal into an AC signal and sends it into the PMSM (E). The FOC (F) controls the frequency of the inverter (more on this in Section 4.4).

4.1 Rectifier

The purpose of the rectifier is to convert the input voltage from AC to DC. The diodes processes a three-phase voltage input to convert the waveform to one constant polarity at its output. The rectifier output voltage is calculated in (6).

$$V_{out} = \frac{3 \cdot \sqrt{3} \cdot \sqrt{2}}{\pi} \cdot V_{in} \approx 2.34 \cdot V_{in} \tag{6}$$

where:

V_{out} = Output voltage of rectifier (rms) [V]

V_{in} = Input voltage of rectifier (rms) [V]

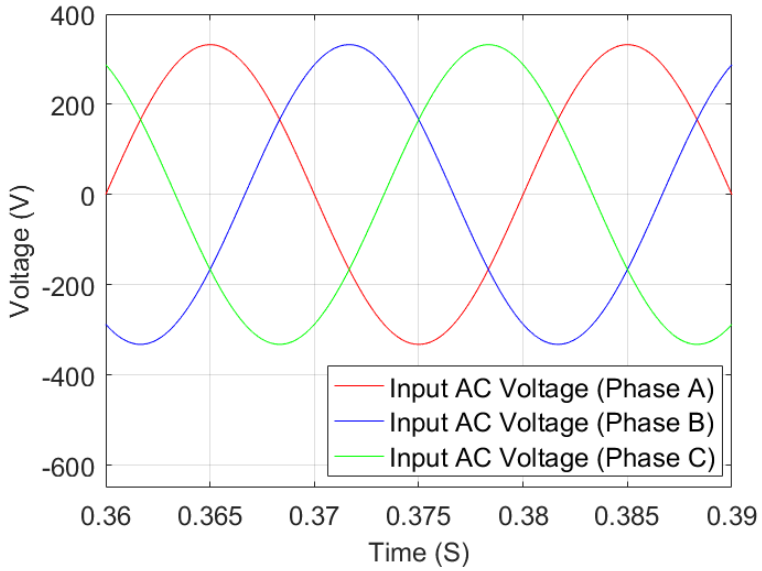


Figure 19: Input AC Voltage of Rectifier

A simple PSIM model of a rectifier is designed to illustrate its behaviour. Figure 19 shows a 230 V_{rms} rectifier input AC voltage. Furthermore, Figure 20 shows the DC output voltage of the rectifier. The simulations show that a filter is necessary to smoothen the voltage to make it more stable.

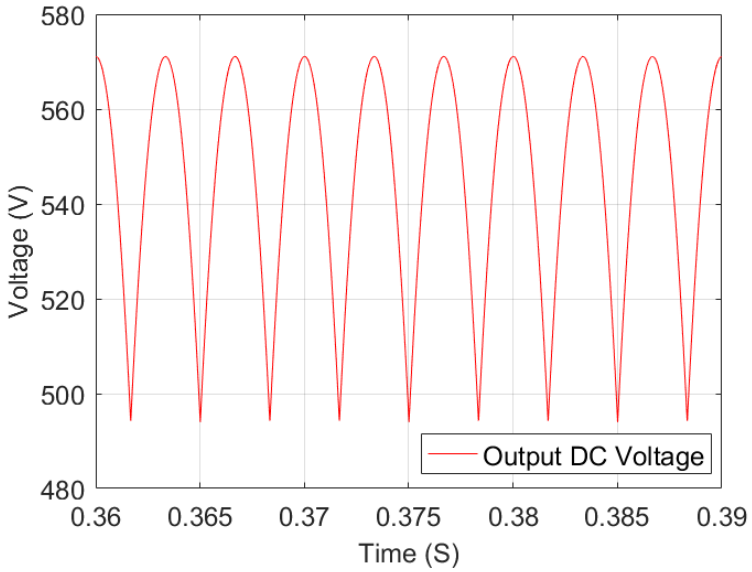


Figure 20: Output DC Voltage of Rectifier

4.2 Filter

The inductor smoothens the current ripple, and the capacitor reduces the voltage ripple. Figure 21 shows the unfiltered and filtered voltage DC signal. The graphs illustrate a more stable DC voltage when processed by the filter.

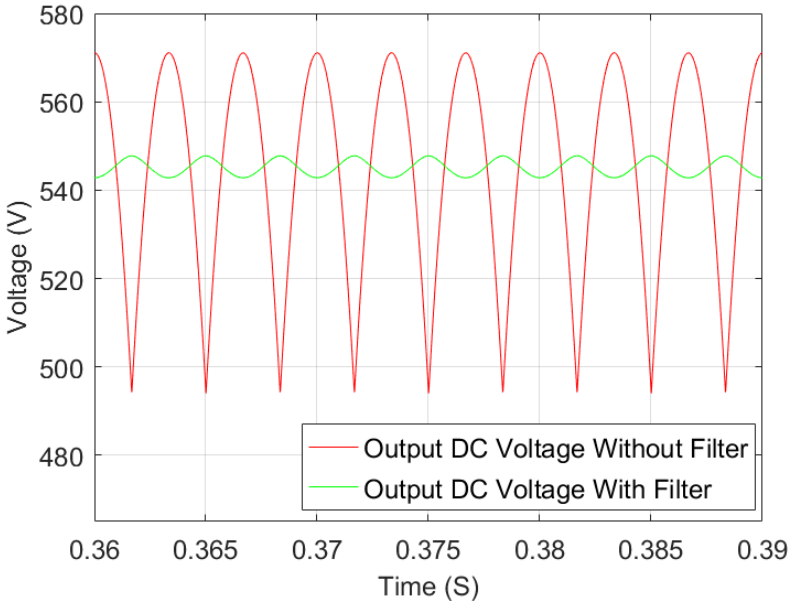


Figure 21: Output DC Voltage Filter and Rectifier

4.3 Motor

The selected motor for the control design is a surface mounted PMSM (SPMSM) which is provided by ABB (BSM100N-2250). The motor has an integrated encoder which gives the possibility to determine angular position and speed of the motor. The graph shown in Figure 22 indicates the rated condition for 160 V, 320 V, 565 V and 650 V applied to the motor. However, the DC voltage of the frequency converter is 545 V under rated conditions.

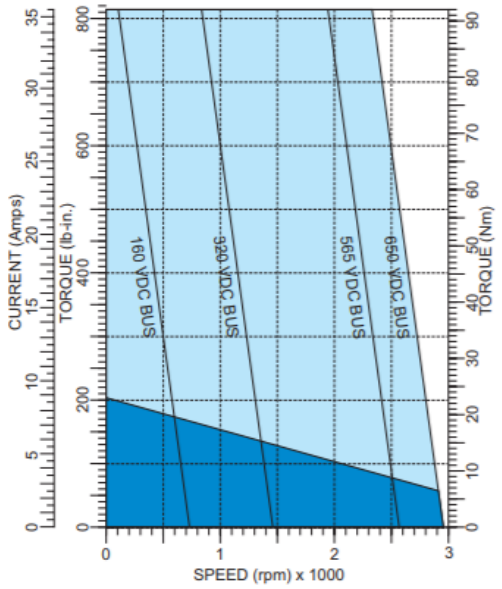


Figure 22: Rated Condition Graph for BSM100N-2250 [A.12]

Estimation techniques makes it possible to obtain the rated conditions of the motor at 545 V. All the slopes (160 VDC BUS - 650 VDC BUS) shown above are equal. This is calculated in [D.1] with (7).

$$m = \frac{\tau_{max} - \tau_{min}}{n_{max} - n_{min}} \tag{7}$$

where:

m = Slope $[\frac{Nm}{rpm}]$

τ_{max} = Maximum torque [Nm]

τ_{min} = Minimum torque [Nm]

n_{max} = Maximum speed [rpm]

n_{min} = Minimum speed [rpm]

The no-load speed is obtained with (8).

$$n_{no-load} = \frac{V_{DC}}{K_e} \cdot 1000 \tag{8}$$

where:

$n_{no-load}$ = No-load speed [rpm]

V_{DC} = Input voltage [V]

K_e = Voltage constant $[\frac{Vpk}{krpm}]$

Combining (7) and (8) enables the calculation of an additional curve which represents the continuous operation border of the 545 VDC BUS frequency converter. Figure 23 shows the new curve with 545 V supply. The rated torque and speed are at the point of intersection of the continuous operation border and the 545 V curve.

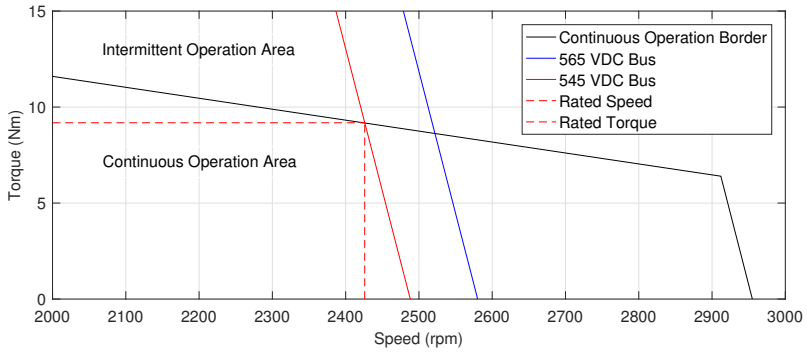


Figure 23: Rated Conditions for 545 VDC Bus

The rated current is calculated with (9) once the rated torque is known.

$$I_r = \frac{\tau_r}{K_\tau} \tag{9}$$

where:

I_r = Rated current [A]

τ_r = Rated torque [Nm]

K_τ = Torque constant $[\frac{Nm}{A}]$

Furthermore, the rated speed and rated torque makes it possible to obtain the rated power with (10).

$$P_r = \omega_r \cdot \tau_r \tag{10}$$

where:

P_r = Rated power [W]

ω_r = Rated speed $[\frac{rad}{s}]$

τ_r = Rated torque [Nm]

Table 3 shows the calculated rated parameters of the motor with the designed frequency converter.

Parameter	Value	Unit	Description
V_{DC}	545	V	Input voltage
P_r	2.332	kW	Rated power
τ_r	9.18	Nm	Rated torque
I_r	3.59	A	Rated current
ω_r	254.05	$\frac{rad}{s}$	Rated motor speed
ω_{max}	260.65	$\frac{rad}{s}$	Maximum motor speed

Table 3: Motor Parameters with 545 V_{DC} Input [A.12]

4.4 Motor Controller

Figure 24 shows an overview of the controllers designed in PSIM. This section describes the principles of FOC and the simulation controller design.

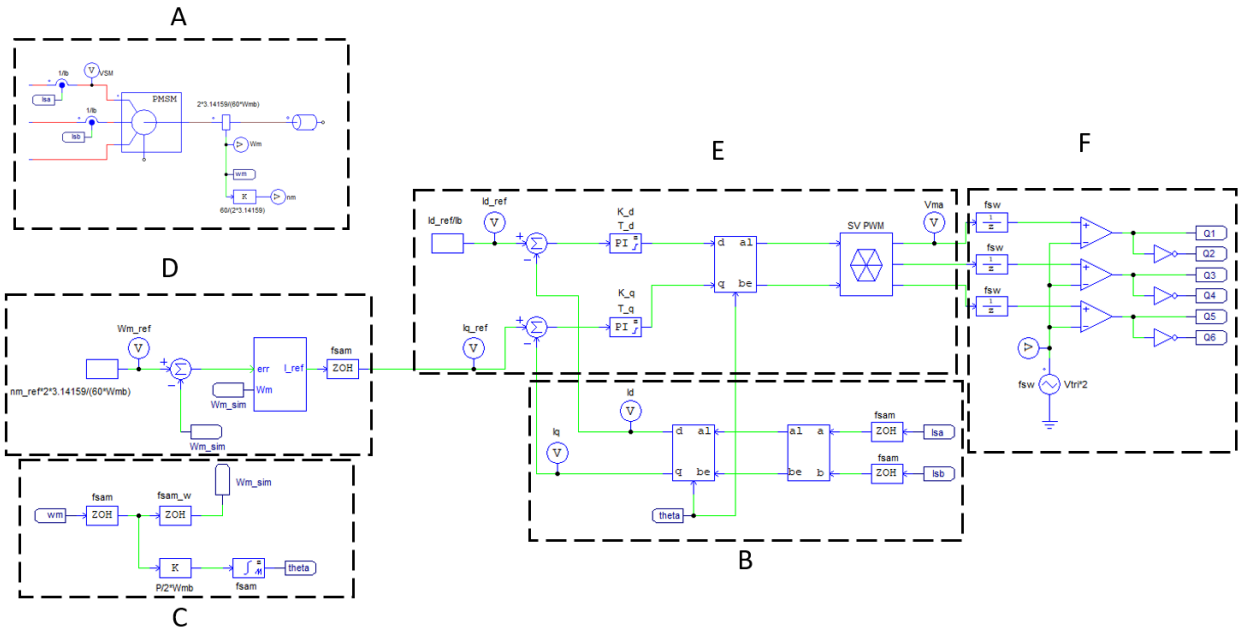


Figure 24: Controllers in PSIM

Measuring the speed and input current of the motor (A) makes it possible to control the motor. The Clarke and Park transformation (B) transforms the reference frame of the current. (C) converts the motor speed into electric angle. Furthermore, (D) converts the reference motor speed into an equivalent current. The PI controllers in (E) regulate the current. (F) creates a PWM signal from the regulated current and sends it into the inverter. Thus regulating the input frequency of the PMSM motor.

4.4.1 Measuring Motor Data

Figure 25 shows the sensors and gain blocks used for obtaining the rotational speed of the motor. The design obtains the speed in both rpm and $\frac{rad}{s}$ values.

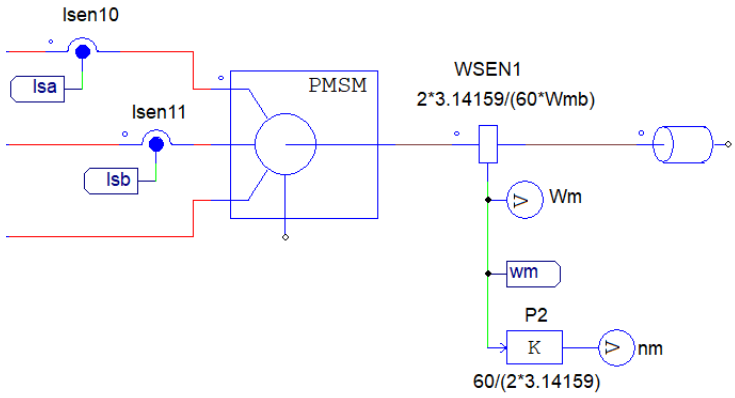


Figure 25: Obtaining the Motor Speed

$WSEN1$ registers the motor speed in $\frac{rad}{s}$. Furthermore, the gain $P2$ converts the motor speed from $\frac{rad}{s}$ to rpm. The correlation between rpm and $\frac{rad}{s}$ is shown in (11).

$$\omega_m = \frac{2\pi \cdot n}{60} \tag{11}$$

where:

ω_m = Mechanical speed [rad/s]

n = Rotational speed of rotor [rpm]

The sensors $Isen10$ and $Isen11$ measures the current in two of the three phases in the input of the motor. Note that only two-phase currents are necessary to measure at this point. The controller calculates the third phase current.

4.4.2 Reference Frame Transformation

The transformation blocks in Figure 26 make it easier to control of the current signals Isa and Isb. The Clarke transformation and Park transformation aligns the reference frames. The PI controller in the design only needs to consider the current values Iq and Id because of the transformations.

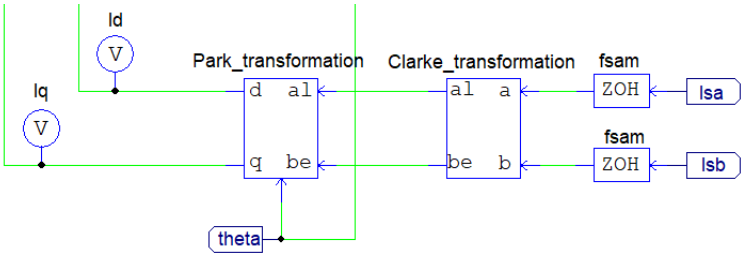


Figure 26: Transformation Blocks

As shown in (12), the Clarke transformation transforms the three-phase reference frame into a two-phase reference frame. Furthermore, the Park transformation obtains a rotating reference frame. Implementing the rotor angle *theta* into the Park transformation block makes it possible to align the reference frames. The sampling blocks $fsam$ adjusts the sample frequency.

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \rightarrow \begin{bmatrix} I_\alpha \\ I_\beta \\ 0 \end{bmatrix} \rightarrow \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{12}$$

where:

$I_a,\ I_b,\ I_c$ = Three-phase reference frame current $[A]$

$I_\alpha,\ I_\beta$ = Two-phase reference frame current $[A]$

$I_d,\ I_q$ = Two-phase rotating reference frame current $[A]$

Figure 27 shows an overview of the three reference frames with its corresponding graph beneath. The graph to the left, middle, and right shows the three-phase reference frame, Clarke transformation, and Park transformation respectively. Note the reduction of current phase movement by each of the transformation.

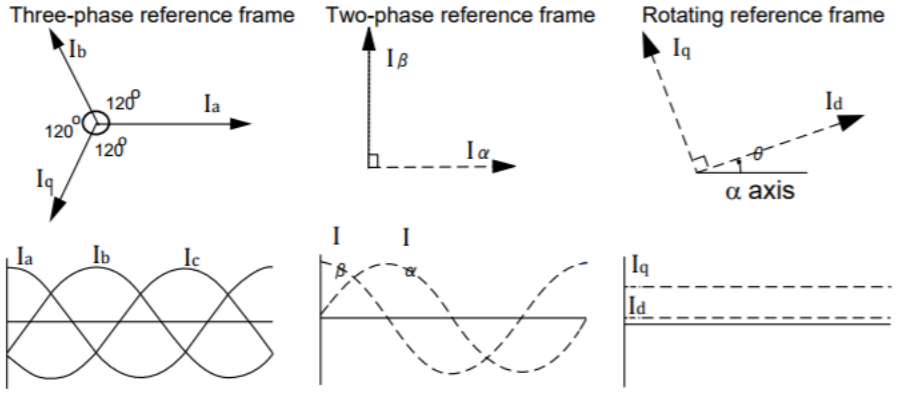


Figure 27: Reference Frames [30]

Figure 28 illustrates the change in the reference frame during a Clarke transformation. The reference frame to the left shows the initial three-phase coordination of Ia, Ib, and Ic. The coordination system to the right shows the two axis stationary reference frame generated by the Clarke transformation with I_α and I_β distributed across the α and β axis.

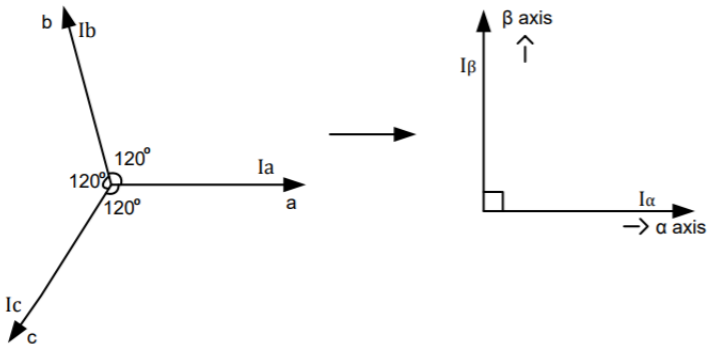


Figure 28: Clarke Transformation Reference Frame

The mathematical expression of the Clarke transformation is shown in (13).

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} I_a \\ I_b \end{bmatrix} \tag{13}$$

where:

$I_\alpha,\ I_\beta$ = Two-phase reference frame current $[A]$

$I_a,\ I_b$ = Three-phase reference frame current $[A]$

The torque produced in the synchronous motor is equal to the cross product of the magnetic fields of the stator and rotor. The motor reaches maximum torque generation when the stator and rotor magnetic fields are orthogonal. In addition, keeping the magnetic fields constantly orthogonal will reduce torque ripple and improve the dynamic response [31]. The two axis $\alpha - \beta$ reference frame from the Clarke transformation are stationary and attached to the stator [32]. Simultaneously, the reference frame of the rotor is rotating, making the task of keeping the magnetic field orthogonal challenging. The Park transformation aligns these two reference frames with each other.

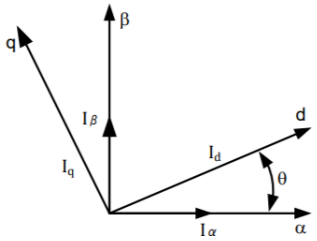


Figure 29: Park Transformation

Figure 29 shows the Park transformation in principle. The transformation aligns the stator flux reference frame $\alpha - \beta$ with the rotor torque reference frame $d - q$ by obtaining the angle θ between the reference frames. The transformation makes sure that the flux current is orthogonal to the torque current at all times. Setting up the reference frame this way makes it possible to control the motor by adjusting the value of the torque current I_q and setting the direct component I_d to zero [31]. The electromagnetic torque can then be controlled with I_q as (14) shows [13].

$$T_{em} = \frac{3}{2}\frac{P}{2} \cdot \lambda_{PM} \cdot I_q \tag{14}$$

where:

T_{em} = Electromagnetic torque $[Nm]$

P = Number of poles [-]

λ_{PM} = Rotor permanent-magnet flux $[\frac{Vs}{rad}]$

I_q = Stator current in q-axis $[A]$

The mathematical representation of the Park transformation is shown in (15).

$$\begin{bmatrix} I_d \\ I_q \end{bmatrix} = \begin{bmatrix} cos\ \theta & sin\ \theta \\ -sin\ \theta & cos\ \theta \end{bmatrix} \cdot \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \tag{15}$$

where:

$I_d,\ I_q$ = Two-phase rotating reference frame current $[A]$

θ = Rotor flux position [rad]

$I_\alpha,\ I_\beta$ = Two-phase reference frame current $[A]$

4.4.3 Retrieving Electrical Angle

The design shown in Figure 30 converts the motor speed wm to its corresponding electric angle $theta$. The electrical angle is needed for the Park transformation and for the Inverse Park transformation. $P1$ converts the mechanical speed into the electrical speed. P is the number of poles in the PMSM and Wmb is the base mechanical speed in *per unit*. The integration block and gain block $P1$ obtains the electrical angle as shown in (17). Furthermore, $fsam\_w$ sets a new sampling frequency for the speed Wm_sim for further use.

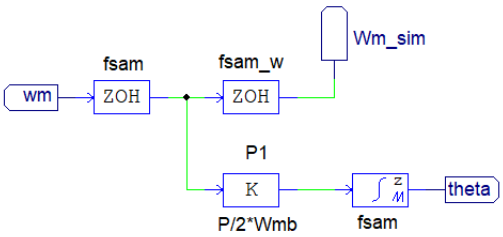


Figure 30: Electrical Angle

The correlation between the electrical speed and mechanical speed is shown in (16).

$$\omega_e = \frac{p \cdot \omega_m}{2} \tag{16}$$

where:

ω_e = Electrical speed [rad/s]

ω_m = Motor speed [rad/s]

p = Number of poles [-]

$$\theta_e = \int \omega_e \, dt \tag{17}$$

where:

θ_e = Electrical angle [rad]

ω_e = Electrical speed [rad/s]

4.4.4 Speed Controller

Figure 31 shows the input and output signals of the speed controller. The constant block $C3$ converts the reference speed from rpm to $\frac{rad}{s}$. The voltage probe Wm_ref measures the desired speed in the converted unit. The summation block compares the converted motor speed to the real (re-sampled) motor speed Wm_sim. The Speed Controller block converts the summarised motor speed signal into an equivalent current Iq_ref (sampled to the same frequency as Iq) for further use.

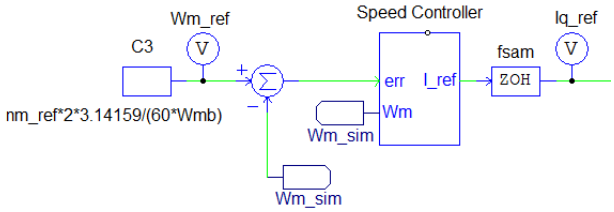


Figure 31: Reference Speed

The speed controller in Figure 32 converts the reference speed to its equivalent current. The gain in the PI controller $S1$ converts the error signal err into torque. In addition, it limits output torque to the rated torque of the motor.

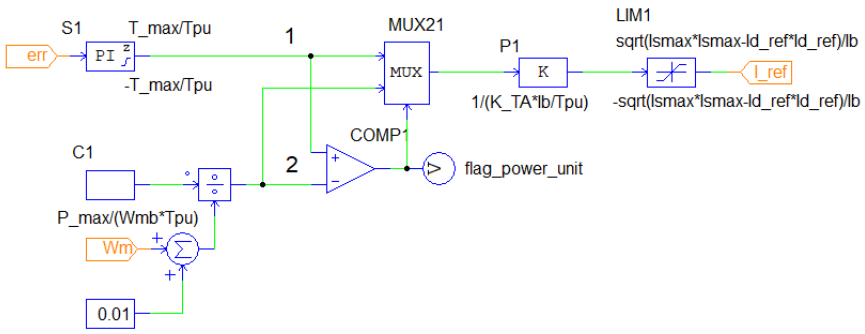


Figure 32: Speed Controller

Dividing the maximum power $C1$ with the actual motor speed Wm obtains the maximum torque. The correlation between the electromagnetic torque, maximum motor power, and mechanical speed is shown in (18).

$$T_{em} = \frac{P_{em,max}}{\omega_m} \tag{18}$$

where:

T_{em} = Electromagnetic torque [Nm]

$P_{em,max}$ = Maximum motor power [W]

ω_m = Mechanical speed [rad/s]

The comparator $COMP1$ compares the limited torque (marked with 1) and the actual torque (marked with 2). The MUX function $MUX21$ will send only one of the two input signals through. The output signal of $MUX21$ depends on the output signal of the comparator. If $1 > 2$ then signal 2 will pass through. If $2 > 1$ then signal 1 will pass through the MUX function. In other words, the signal with lowest value will be the output signal of $MUX21$. The gain $P1$ converts the torque output signal of $MUX21$ into a current signal, based on (19). The signal is then limited by the $LIM1$ (maximum current) and sent as the output signal of the speed controller (I_ref in Figure 31).

$$\hat{I}_s = \frac{T_{em}}{k_T} \tag{19}$$

where:

$\hat{I}_s$ = Magnitude of stator-current space vector [A]

T_{em} = Electromagnetic torque [Nm]

K_T = Torque constant [Nm/A]

4.4.5 Current Controller and Inverse Transformations

Figure 33 shows the current controller which consists of two PI controllers. Id is set to 0 for this application, but it should be set to a value other than zero for higher torques and for field weakening [33]. This makes it possible to control the speed of the motor by controlling Iq. $Idref$ and $Iqref$ are summed with the measured Id and Iq respectively. The PI controllers $S2$ and $S3$ adjust the signals.

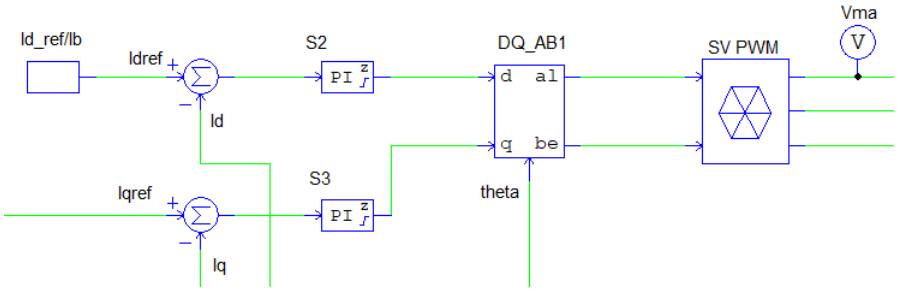


Figure 33: Current Controller, Inverse Park, and SV PWM

The processed signals and the electrical angle *theta* are sent into the Inverse Park transformation DQ_AB1. The transformation function is shown in (20). Furthermore, the Space Vector PWM ($SV\ PWM$) transforms the two-phase orthogonal α/β input signal back to a three-phase signal.

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \begin{bmatrix} cos\ \theta & -sin\ \theta \\ sin\ \theta & cos\ \theta \end{bmatrix} \cdot \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{20}$$

where:

$I_\alpha,\ I_\beta$ = Two-phase reference frame current $[A]$

θ = Rotor flux position [rad]

$I_d,\ I_q$ = Two-phase rotating reference frame current $[A]$

4.4.6 Controller Output

Figure 34 shows the output signals of the control design. The unit delay blocks ($\frac{1}{Z}$) introduces a digital delay to a, b, and c which is inherent in all digital systems. The comparators $COMP1 - COMP3$ processing the signals further. The pulse signal $VTRI1$ is sending a triangular-wave signal with switching frequency fsw, to compare the signals with the three-phase signals. This generates the pulse signals $Q1$, $Q3$, and $Q5$ in addition to the inverted signals $Q2$, $Q4$, and $Q6$.

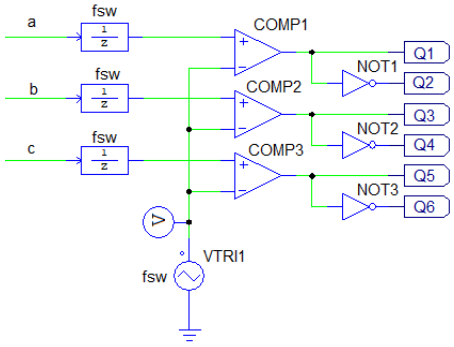


Figure 34: Output Control Signal

Figure 35 shows the $Q1$ PWM signal to demonstrate its behaviour. A high signal from the current controller will give a wide pulse. A low signal will give narrow pulse signal. these signals (Q1-Q6) will determine the switching frequency of the IGBTs. Furthermore, the switching frequency of the IGBTs in the inverter will determine the speed of the PMSM motor.

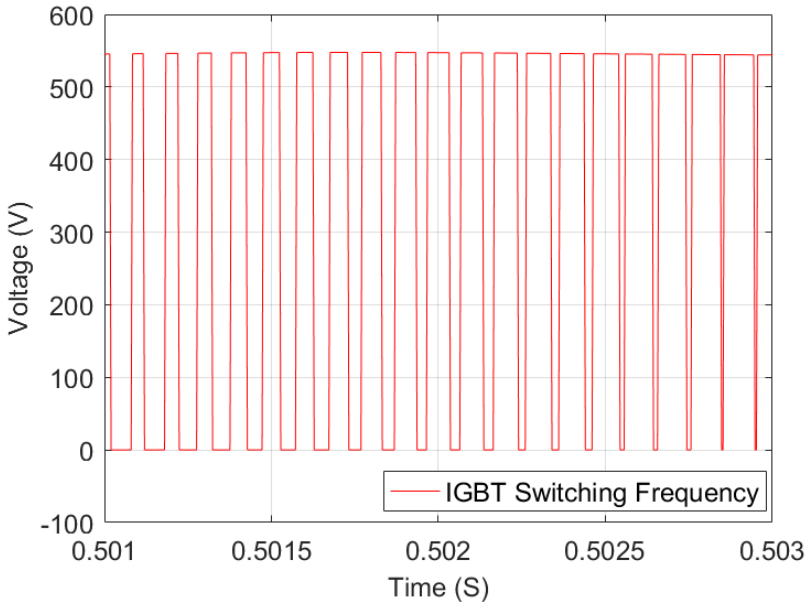


Figure 35: Switching Frequency of an IGBT

5 SimCoder

The simulation design described in Section 4 makes it possible to test different scenarios before running the PMSM. However, PSIM provides SimCoder in addition to the simulation software. This module enables automatic code generation. The generated code can be imported into the DSP to run the frequency converter. However, generating the code requires some adjustments. This chapter describes these design adjustments.

5.1 Encoder Conversion

Figure 36 shows the speed measurement of the simulation design. Furthermore, Figure 37 shows the the SimCoder design. The incremental encoder attached to the available PMSM indicates the motion of the motor shaft. Implementing a corresponding encoder $PMSM\_Encoder$ makes it possible to estimate the angle and speed of the system. The *Encoder Counter* in the simcoder design specifies the input pins on the DSP, as well as counting the $PMSM\_Encoder$ output signals.

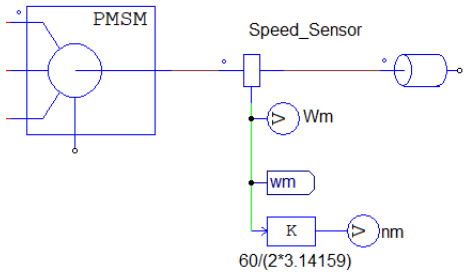


Figure 36: Speed Measurement Simulation

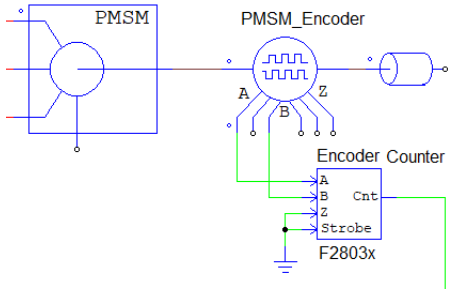


Figure 37: Encoder and Counter for SimCoder

5.1.1 Angle Calculation

The output value of the encoder counter value needs further calculations to retrieve the speed and angle of the motor. Figure 38 shows the SimCoder design for the angle conversion.

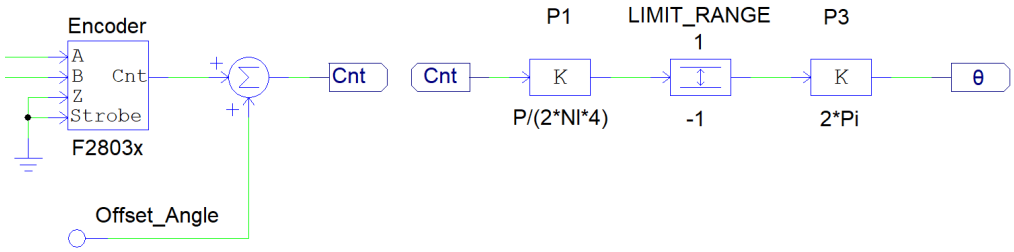


Figure 38: SimCoder Angle Calculation

The encoder counter value is an indicator of the mechanical angle of the motor. The proportional gain $P1$ calculates the electrical angle. The relation between the electrical and mechanical angle is shown in (21).

$$\theta_e = \frac{P}{2} \cdot \theta_m \tag{21}$$

where:

θ_e = Electrical angle [rad]

P = Number of poles[-]

θ_m = Mechanical angle [rad]

An important parameter of the encoder is the number of lines Nl which specifies the number of electrical pulses registered during one revolution. The Nl alternatives to select from are $X1$, $X2$, and $X4$. The incremental encoder sends quadrature digital signals. This means that the two output waveforms are 90 degrees out of phase. The Nl of the encoder is set to $X4$. As a result, the corresponding resolution of the encoder counter value will be four times the number of lines from the encoder. Figure 39 shows an example of quadrature encoder pulses A-B and the index signal which sends one pulse per revolution. The numbering 1-4 in the figure illustrates the counting frequency when the Nl is set to X4 in an encoder.

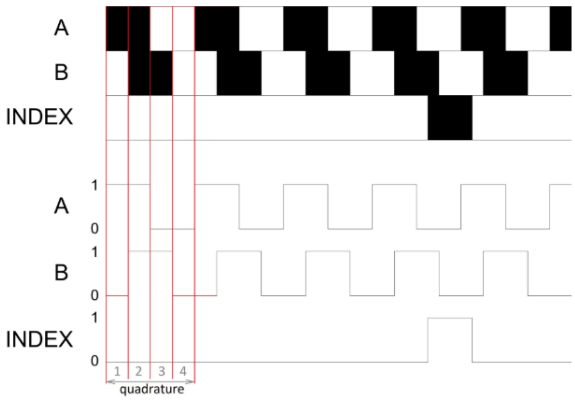


Figure 39: Quadrature Encoder Pulses [34]

The encoder counter value is divided by its resolution to obtain the per unit value. The $limit\_range$ limits the output value of $P1$ from -1 to 1, for per unit conversion. Finally, $P3$ multiplies the per unit value by 2π, converting the value into radians. Note the summation of the offset angle and the encoder counter value. The encoder angle calculation and the ideal angle deviates to some extent. The offset angle adjusts the deviation.

5.1.2 Speed Calculation

The formula for encoder speed calculation is shown in (22) [35].

$$v(k) = \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T} = \Delta X \cdot f \tag{22}$$

where:

$v(k)$ = Velocity at time instant k $[\frac{rad}{s}]$

$x(k)$ = Position at time instant k $[rad]$

$x(k-1)$ = Position at time instant k-1 $[rad]$

T = Fixed unit time or inverse of velocity calculation rate $[s]$

f = Sampling frequency $[Hz]$

The speed calculation in Figure 40 is the corresponding formula in SimCoder. $ZOH7$ sets a sampling frequency. The summation of $ZOH7$ and $UDELAY$ results in retrieving ΔX. However, the summation of the delay signal leads to a negative peak in the output signal when the counter resets. The comparator along with $P12$ compensates for this peak. Whenever the peak occurs, $P12$ sends a gain opposite to the peak signal. The value of the peak signal is equal to the resolution of the encoder En_res. The proportional block $omega\_m$ implements the remaining calculations. The signal is divided by the resolution and multiplied with 2π to get the output value in $\frac{rad}{s}$. The multiplication of the sampling frequency $fsam\_e$ finalises the encoder speed calculation. The 1. order low pass filter $S1$ smoothens the output signal. The output signal Wm_sim is the mechanical speed of the motor shaft.

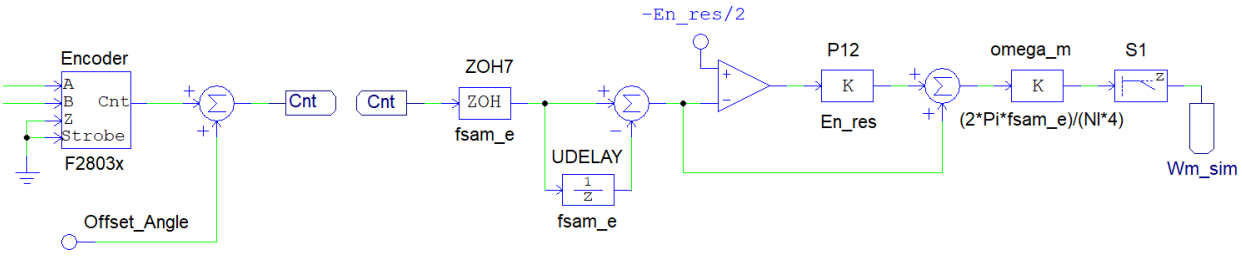


Figure 40: SimCoder Speed Calculation

Figure 41 shows the peak compensation.

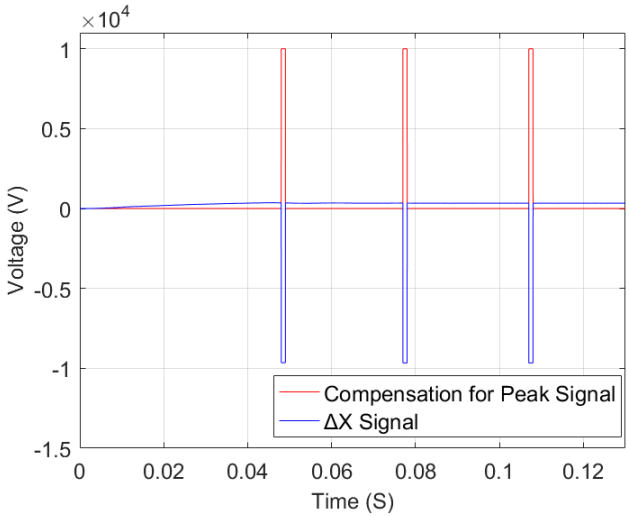


Figure 41: ΔX Pulse Compensation

A low-pass filter attenuates the signal. However, the delay is increasing as the cut-off frequency is decreasing. The low-pass filter is tested with different cut-of frequency to get a steady and fast enough speed estimation. Figure 42 shows some of the test frequencies. At the highest frequency (800 Hz) the signal is unstable. However, the low frequency of 100 Hz shows a big delay. The 300 Hz test results show a good balance between the delay and stability. As a result, the cut-of frequency is set to 300 Hz.

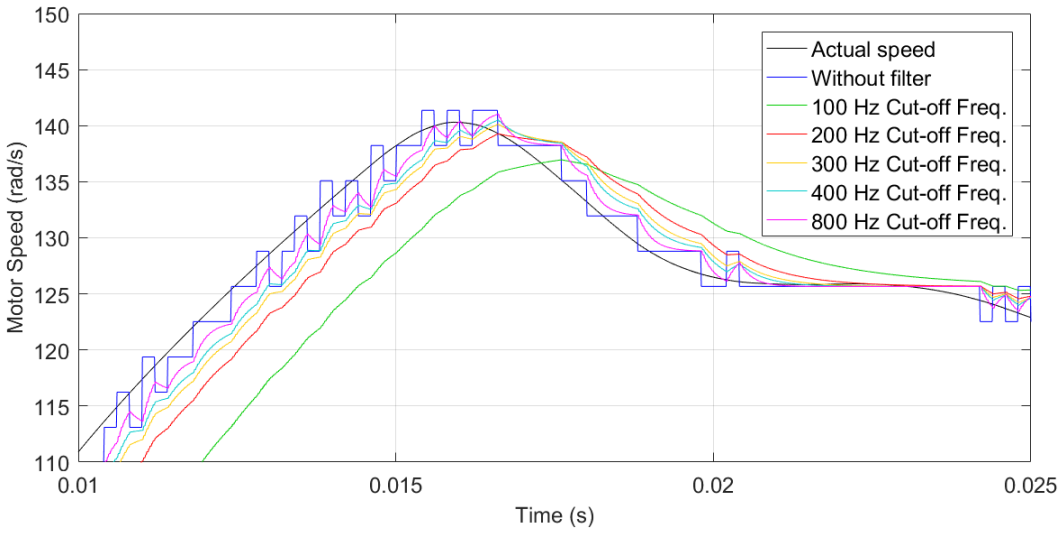


Figure 42: Speed Estimation with Low-Pass Filter

5.2 Analog / Digital Converter

Figure 43 shows the input current of the simulation design which consists of two current inputs (Isa and Isb), a frequency sampling block, and a Clarke transformation block *Clarke_ Transformation*. Converting the input signals into digital signals makes the design compatible with SimCoder.

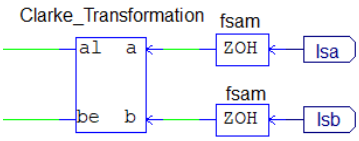


Figure 43: Simulation Input Current

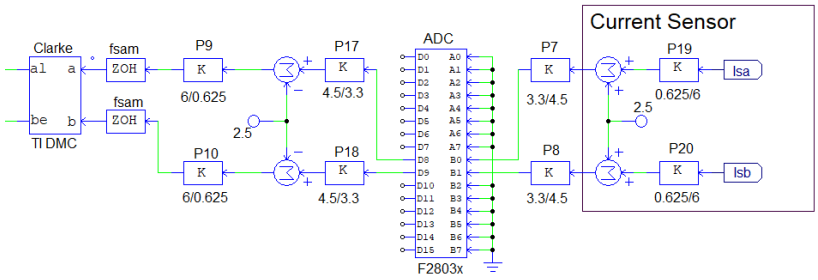


Figure 44: SimCoder Input Current

Figure 44 shows the SimCoder design with the A/D converter ADC. The proportional gains $P19$-$P20$ and the summation of + 2.5 V represents the output signal of the hardware current sensors. The output voltage equation for the current sensor (given in [A.9]) is shown in (23).

$$V_{out} = 2.5 \pm \frac{0.625 \cdot I_P}{I_{PN}} \tag{23}$$

where:

V_{out} = Output voltage of the current sensor [V]

I_P = Primary current [A]

I_{PN} = Primary nominal current [A]

The input signal range of the A/D converter is from 0 V to 3.3 V. The proportional blocks $P7$ and $P8$ are implemented to manipulate the input values so that they are within the range of the converter. The gain of the proportional blocks is set to $\frac{3.3}{4.5}$. Furthermore, $P17$ and $P18$ are set to $\frac{4.5}{3.3}$ to get the correct values in the software control system. The signals are subtracted by 2.5 for further use in the control system. $P9$ and $P10$ are implemented to retrieve the primary current I_P. The mathematical expression of the subtraction and gain adjustment are shown in (24).

$$V_{out} = 2.5 - 2.5 \pm \frac{0.625 \cdot I_P}{I_{PN}} \cdot \frac{I_{PN}}{0.625} = I_P \tag{24}$$

5.3 Pulse Width Modulation

Figure 45 shows the simulation design of the PWM signal. Figure 46 shows the design compatible for code generation. The PWM block $3 - ph\ PWM$ includes all the PWM parameters. The implemented space vector generator $SV\ Gen$ is compatible with SimCoder.

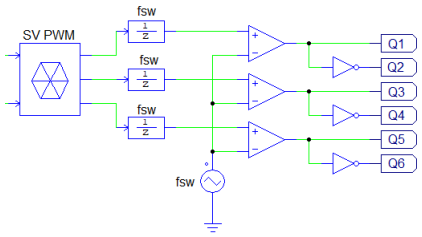


Figure 45: PWM Simulation Design

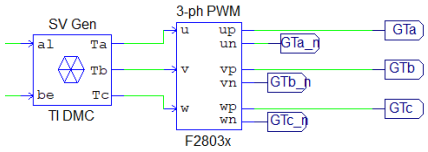


Figure 46: PWM SimCoder Design

5.4 Motor Controller Overview

Figure 47 shows an overview of the controller after the conversion. The changes in the speed controller and the transformations is minimal. Implementing a ramp for the reference speed in the speed controller makes it possible to control the acceleration of the reference speed. The PI controllers are simplified by implementing the block designed by Texas Instruments (TI). The Clarke and Park transformation in the design are from TI. The start/stop section is designed to start and stop the PWM generator as desired.

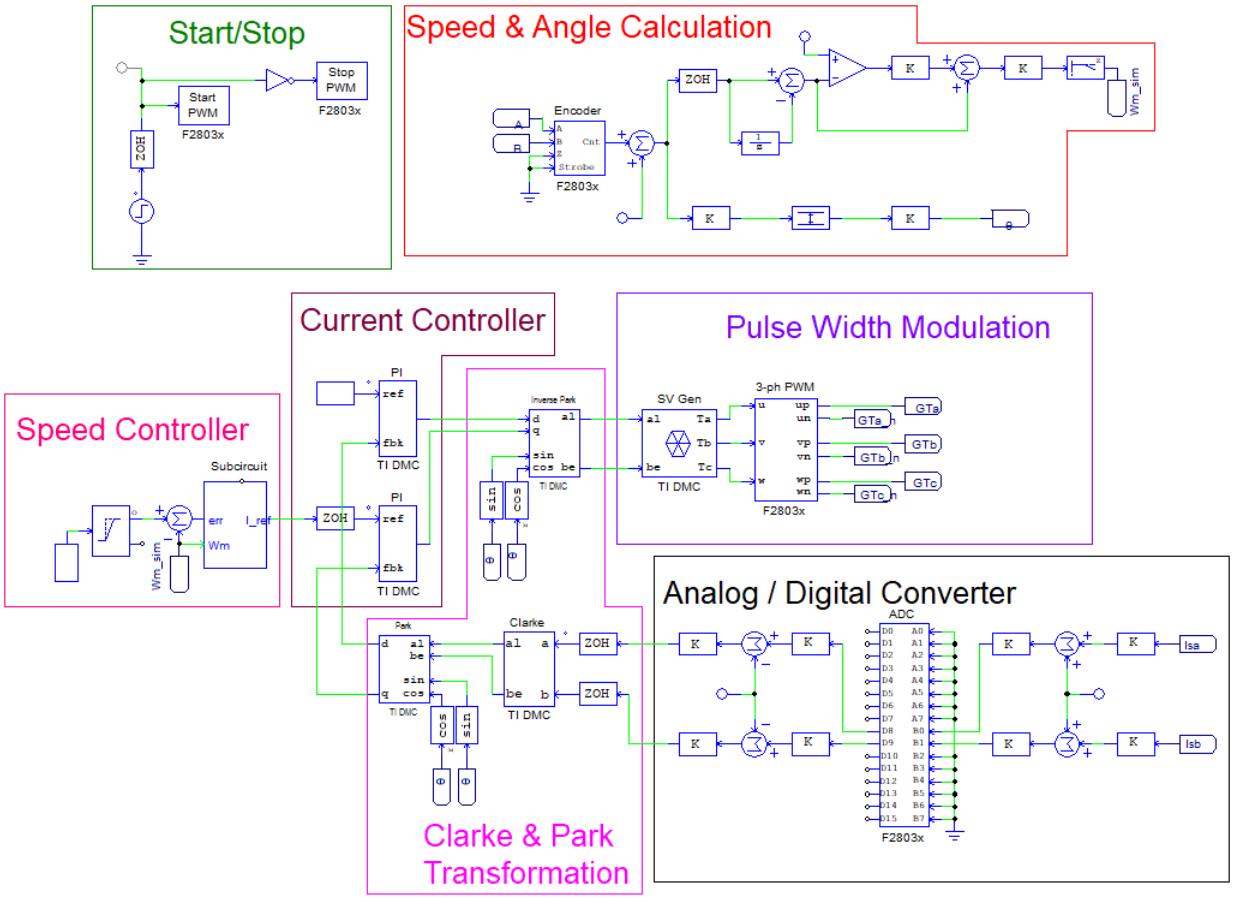


Figure 47: SimCoder Design Overview

5.5 Hardware Configuration

Figure 48 shows the hardware configuration, Serial Communication Interface (SCI) configuration, and the Digital Signal Processor (DSP) clock. The hardware configuration defines the input and output ports in a specific hardware setting. The SCI configuration defines the port selection, speed, and output buffer size of the DSP oscilloscope. The DSP clock defines the clock speed of the oscilloscope. Configuring the DSP oscilloscope makes it possible to read the values of the control system on the computer while running the code. The hardware configuration, SCI configuration, and DSP clock specification are available in [B.1].

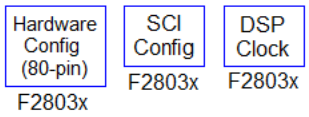


Figure 48: Hardware Configuration, SCI Configuration and DSP Clock

Figure 49 shows the DSP oscilloscope while running a test PSIM design. The speed and parity check of the SCI configuration needs to be identical to that of the DSP oscilloscope. The signals SCIOut1 to SCIOut3 are the signals chosen to read in the given design. A convenient feature of the DSP oscilloscope is to start and stop the program and change variables such as speed reference while running the code. The DSP oscilloscope can be used to monitor and change the variables of the control circuit. In addition, it is able to monitor encoder output signals and thus the speed of the motor.

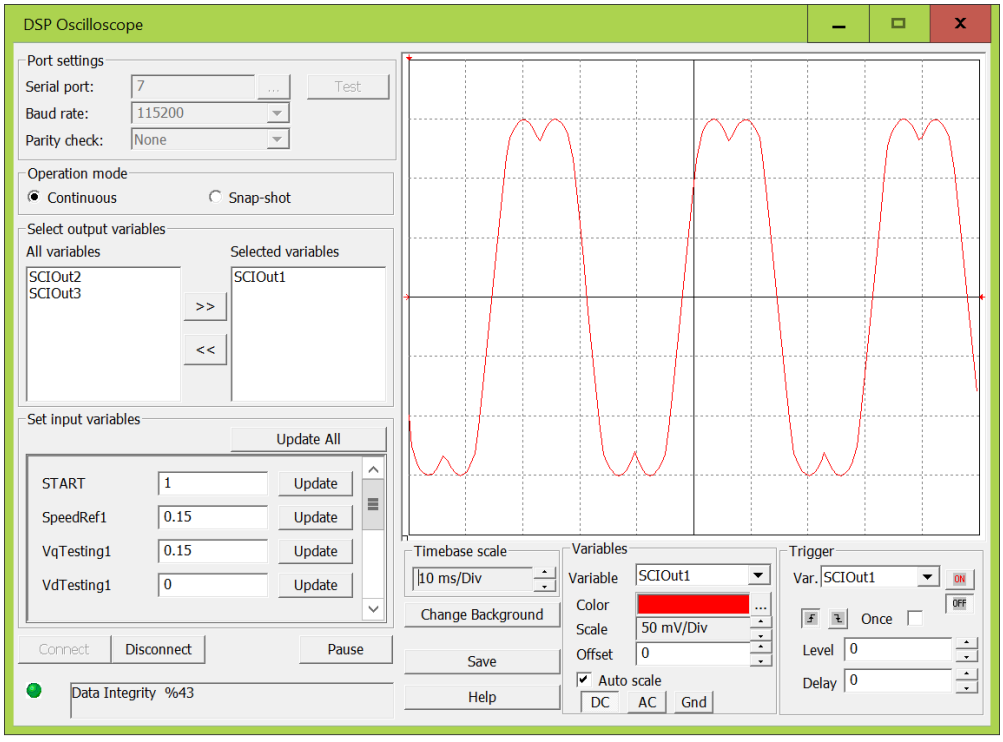


Figure 49: DSP Oscilloscope

6 Digital Signal Processing

This section describes the components and software needed for digital signal processing. The hardware for signal processing is a Digital Signal Processing (DSP) development board. Code Composer Studio (CCS) is needed to import the generated code into the development board. The section describes the configuration of CCS. Furthermore, a brief explanation of the current sensor calibration is given.

6.1 Development Board

A DSP development board processes the signals generated from the SimCoder design. Figure 50 shows the DSP board used in the design. Powesim Inc. provides the DSP development board as a package. The package includes both a DSP control board and a TI controlCARD. The DSP controlCARD used in this design is the F28035 Piccolo^{TM} Family. The pins mounted on the board registers both the output and input signals.

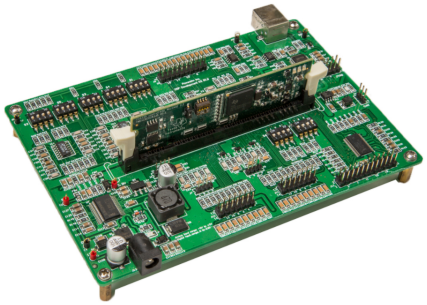


Figure 50: DSP Development Board [36]

Figure 51 shows an overview of the pins. When running the code, the analog input connector $J8$ registers the motor current signals $J7$ and $J9$ registers the encoder signals. The SCI connector $J6$ sends an enable signal to the gate driver. Furthermore, the gate driver interface $J12$ sends the output PWM signals to the gate driver.

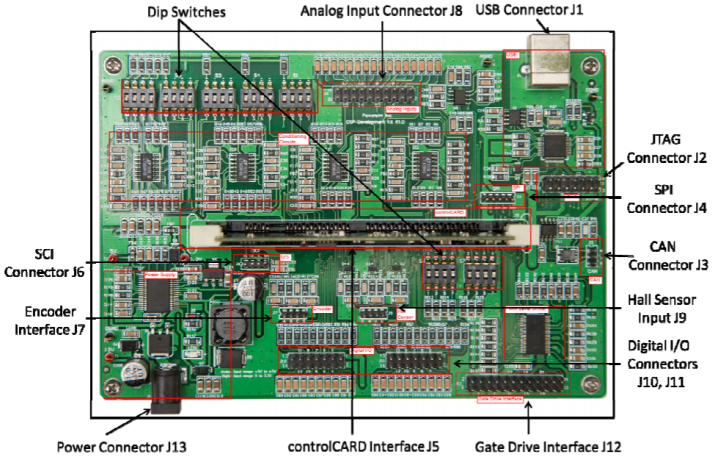


Figure 51: Development Board Connector Overview

Figure 52 shows the input connector $J8$ which contains the pins for the measured motor current. Pin number 11 and 13 ($Iain$ and $Ibin$) corresponds to the SimCoder A/D converter input ports $B0$ and $B1$ shown in Figure 44. Furthermore, pin number 1 and 2 supplies the current sensors with 5 V.

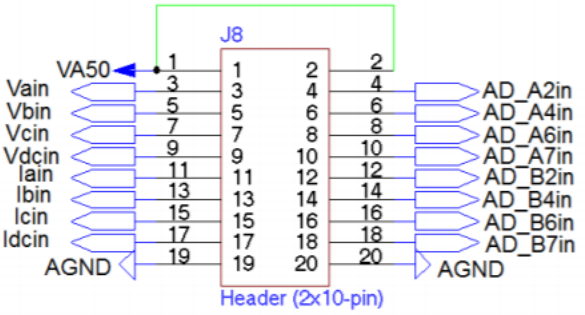


Figure 52: Current Sensor Input Connector $J8$

The input connectors $J7$ and $J9$ shown in Figure 53 and Figure 54 respectively are used to register the encoder signals.

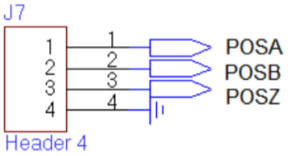


Figure 53: Encoder Connector $J7$

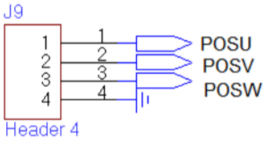


Figure 54: Encoder Connector $J9$

Figure 55 shows how $J7$ and $J9$ are connected with the encoder. Pin $POSV(EQEP1A)$ and $POSW(EQEP1B)$ corresponds to port A and port B in the encoder. The Z signal, which provides one count per revolution, is connected to ground together with $POSA(EQEP1S)$, $POSB(EQEP1I)$, and encoder ground G. The ports of the F28035 piccolo microcontroller (EQEP1X ports) are shown in [A.13].

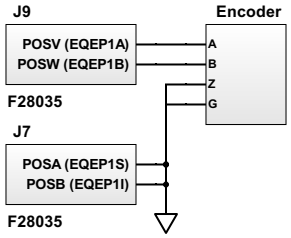


Figure 55: Encoder Connections

Figure 56 shows the PWM output connector $J12$. Furthermore, Table 4 describes the applied pins. Phase A, B, and C all have a top switch (high) signal and a bottom switch (low) signal which acts opposite to each other. The digital ground is connected to the common ground of the design, and the voltage supply KL_30 in pin 1 supplies the gate driver.

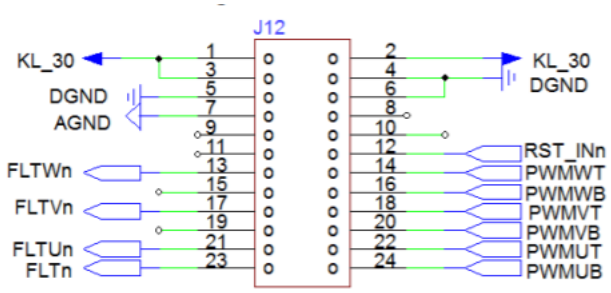


Figure 56: PWM Signal Output Connector

Pin Number	Parameter	Description
1	KL_30	12 V Power Supply
4	DGND	Digital Ground
14	PWMWT	PWM Gate High Phase C
16	PWMWB	PWM Gate Low Phase C
18	PWMVT	PWM Gate High Phase B
20	PWMVB	PWM Gate Low Phase B
22	PWMUT	PWM Gate High Phase A
24	PWMUB	PWM Gate Low Phase A

Table 4: PWM Connector Signals

6.2 Code Composer Studio

CCS processes the generated code from SimCoder. When generating the code, a .pjt file (among other files) is saved in a folder by PSIM. The .pjt file is used to import the code into CCS. The target needs to be configured when the project is imported. The configuration defines the control hardware available. Table 5 shows the configuration parameters.

Configuration	Description
Experiment's Kit - Piccolo F28035	ControlCARD and DSP Development Board
Digital Texas Intruments XDS100v1 USB Debug Probe	Internal Debug Probe on the ControlCARD
C2000Ware	Product Family

Table 5: CCS Configuration

After the target configuration, the project is ready to be built and run. By doing so, the imported code will appear. The time stamp on the code needs to be checked continuously when adjusting the design in PSIM

to verify the connection between PSIM and CCS. Figure 57 shows the CCS display when running the code. The "Debug", "Expressions", and "System_v1_3.c" tabs show the debug probe, variable expressions, and the imported code respectively. The time stamp is printed at the top of the code. The DSP oscilloscope in Figure 49 is used to change the value of the expressions while running the program in CCS.

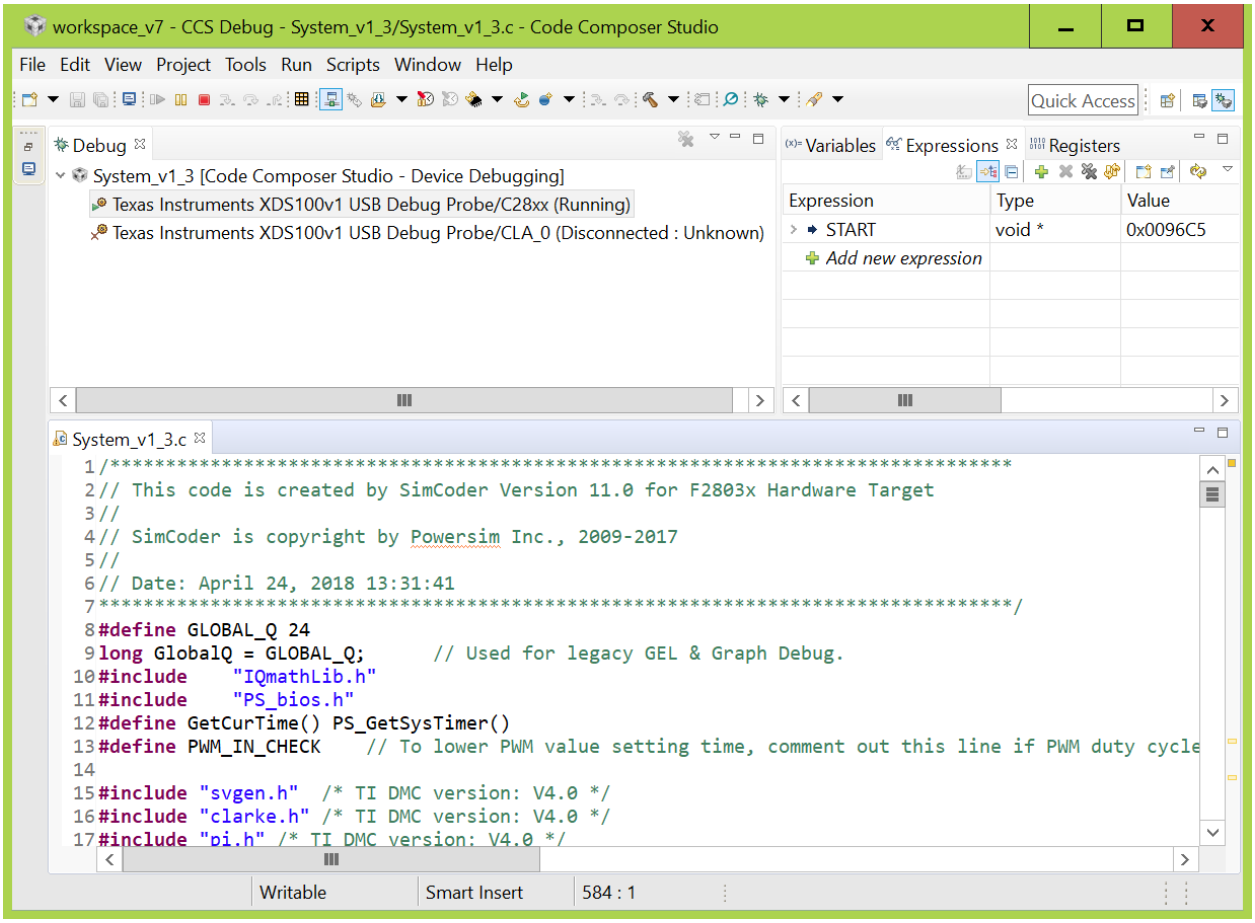


Figure 57: CCS Display

6.3 Current Sensor Calibration

The DSP board converts the received input current by default. The current conversion is shown in Table 6. The conversion for the three phases I_a, I_b, and I_c is the same.

Input	Description
AC	When $I_{in} = 5 \cdot sin(\omega t)$, $I_{DSP} = 1.5 + 1.5 \cdot sin(\omega t)$
DC	When $I_{in} = 3.5 + 3.5 \cdot sin(\omega t)$, $I_{DSP} = 1.5 + 1.5 \cdot sin(\omega t)$

Table 6: DSP Board Current Conversion [A.11]

The input value of the current sensors needs to be calibrated in SimCoder due to the DSP conversion.

Figure 58 shows the proportional gains $P9$ and $P10$ which converts the DSP value to the actual current value. Furthermore, the $Zero\_Adjust$ adjusts the zero point. The SCI output blocks I_D8 and I_D9 monitors the current before the calibration. Ia and Ib monitors the results after the calibration. Note that the SimCoder design in Figure 44 has different proportional gains compared to the one in Figure 58. The prior is for simulating the design and does not take the DSP conversion into account. The latter takes the DSP conversion into account. This makes it able to run the hardware design.

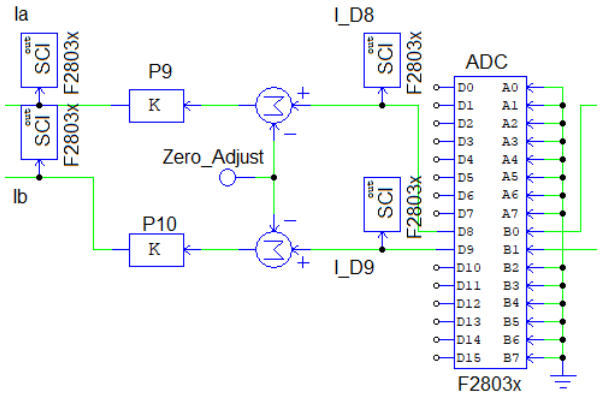


Figure 58: Current Calibration

First, the $Zero\_Adjust$ is adjusted. The value is obtained by monitoring I_D8 and I_D9 with no current flowing through the hardware sensors. This value is then subtracted to get the zero point in the design. Monitoring I_D8 and I_D9 while measuring 1 A with the current sensors makes it possible to calculate the calibration gain with (25).

$$V_{1A} \cdot K_{1A} = 1 \tag{25}$$

where:

V_{1A} = Value measured in SimCoder with 1 A going through the sensor [V]

K_{1A} = Proportional gain needed to get 1 A in the SimCoder design [-]

The calibration gain K_{1A} of $P9$ and $P10$ is calculated to be 21.62274825 and 21.04230583 respectively. The calculated proportional gain is tested with currents ranging from $0 - 4$ A, which is the maximum current of the resistances in the test design ($R1 - R3$ in Figure 60). Table 7 shows the calibration results. The maximum deviation is 1.275 % on I_b when testing with 4 A. The accuracy is considered sufficient.

Test Current [A]	**Current Measured in SimCoder [A]**	**Deviation [%]**
1	$Ia = 0.9997$, $Ib = 1.0024$	$Ia = 0.03$, $Ib = -0.24$
2	$Ia = 2.0034$, $Ib = 1.9892$	$Ia = -0.17$, $Ib = 0.54$
3	$Ia = 3.0062$, $Ib = 2.9736$	$Ia = -0.207$, $Ib = 0.88$
4	$Ia = 4.0094$, $Ib = 3.9490$	$Ia = -0.235$, $Ib = 1.275$

Table 7: Current Calibration Results

7 Hardware Configuration

This section describes the hardware configuration, the circuit design, and its associated calculation. In addition, it presents the designed setups for the tests in detail.

7.1 Circuit Design

Figure 59 shows an overview of the electrical system and its setup. The additional resistances and capacitors are implemented as recommended by the provider. The specifications of the components and the recommended circuit design are available [A].

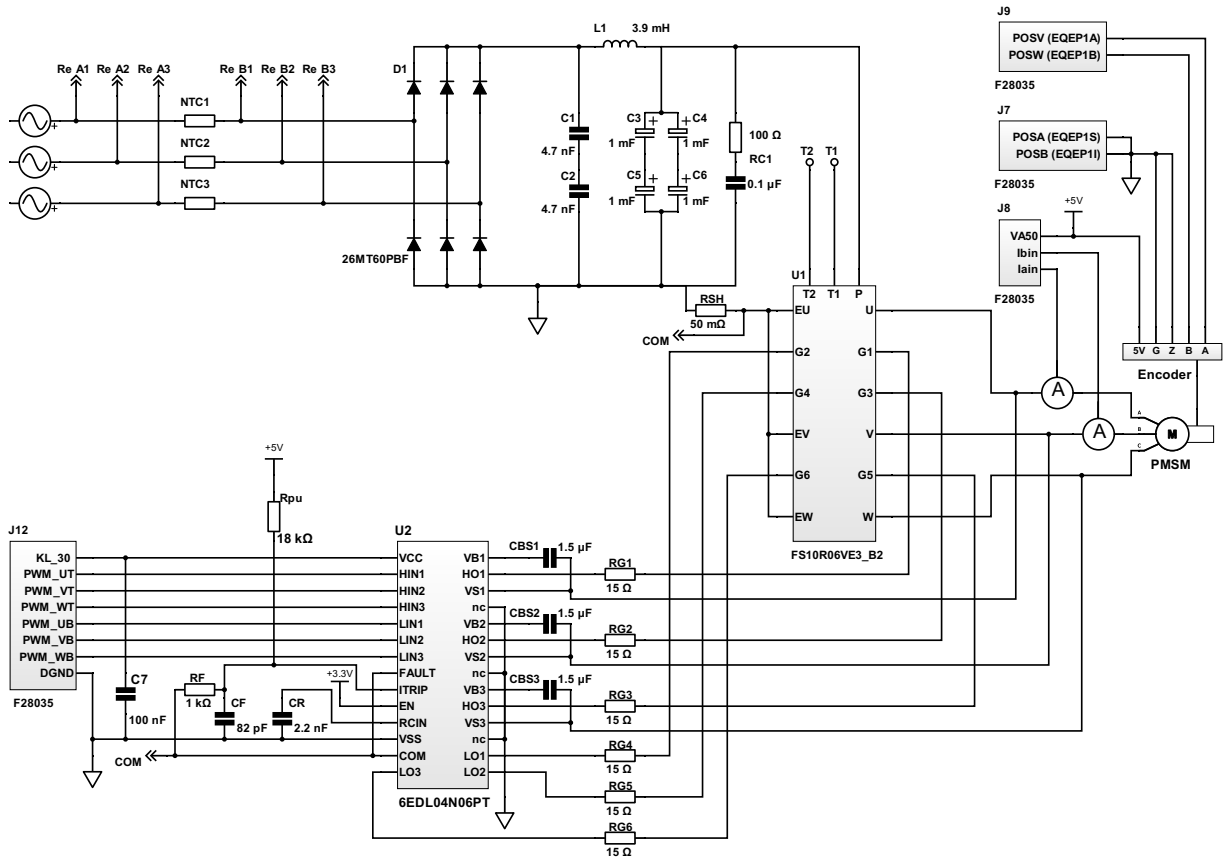


Figure 59: System Diagram

The three-phase power goes through the NTC thermistors and to the rectifier ($26MT60PBF$). The rectifier sends out the rectified power to the inverter $FS10R06VE3\_B2$ via a RC snubber and a filter. T1 and T2 are for temperature measurement of the inverter. The inverter receives gate signals from the gate driver $6EDL04N06PT$ and delivers three-phase power with a desired frequency to the motor. The high side inverter outputs U, V, and W are connected to the gate driver for power supply and the bootstrap function of the gate driver. Two current sensors deliver the measured signals to the current sensing input of the DSP $F28035$. The low side inverter output going back to the negative side of the rectifier via gate driver connections COM, ITRIP, RCIN, and VCC. The DSP (J12) delivers the PWM gate signal and a 5 V supply

signal to the gate driver. The shunt resistor R_{SH} is calculated with (26) which is based on equation 3 in [A.6].

$$R_{SH} = \frac{V_{IT,TH+}}{I_{ITRIP}} \tag{26}$$

where:

R_{SH} = Shunt resistor [Ω]

$V_{IT,TH+}$ = ITRIP positive going threshold [V]

I_{ITRIP} = Over-current for gate driver shutdown [A]

The over-current is set to minimum 8 A and maximum 10.2 A depending on the threshold of $ITRIP$. $ITRIP$ resistor R_F and pull-up resistor R_{pu} are calculated with the equations shown in [A.7]. Bootstrap capacitors C_{BS} are calculated with (27) derived from [A.6]. The voltage ripple is set to 0.1 V.

$$C_{BS} = \frac{i_{QBS} \cdot t_P + Q_G}{\Delta V_{BS}} \cdot 1.2 \tag{27}$$

where:

C_{BS} = Bootstrap capacitor [F]

i_{QBS} = Quiescent current VBS supply [A]

t_P = Swithing period [s]

Q_G = Total gate charge [C]

ΔV_{BS} = Bootstrap voltage ripple [V]

The purpose of the gate resistor R_G is to reduce overshoot and oscillating current waveform. The current oscillation will be underdamped and the switching time will be extended if the resistor value is to high [37]. The minimum resistor is calculated in (28). The value calculated is rounded up to a standard resistor value.

$$R_{G,min} = 2 \cdot \sqrt{\frac{L_S}{C_{ISS}}} \tag{28}$$

where:

$R_{G,min}$ = Minimum gate resistor to retain a non-oscillating gate current waveform [Ω]

L_S = Stray inductance of the inverter [H]

C_{ISS} = Input capacitance of the inverter [F]

Full calculations for R_{SH}, C_{BS} and $R_{G,min}$ are in [D.2]. The rest of the capacitors are selected with reasonable values and modified after testing.

7.2 Gate Driver and Inverter Test Design

Figure 60 shows the simulation design used to verify the behaviour of the hardware. In addition, a similar test circuit is set up to measure the signals of the hardware components. The simulation results and hardware measurements are then compared for verification. Three identical gate drivers are implemented in the system. The selected gate driver ($6EDL04N06PT$) for the hardware design is not available in PSIM. As a result, a similar gate driver $IRS21867$ is selected for the simulation. A 15 V (VCC) supply is connected to the gate driver. A 40 V supply is connected to the IGBTs.

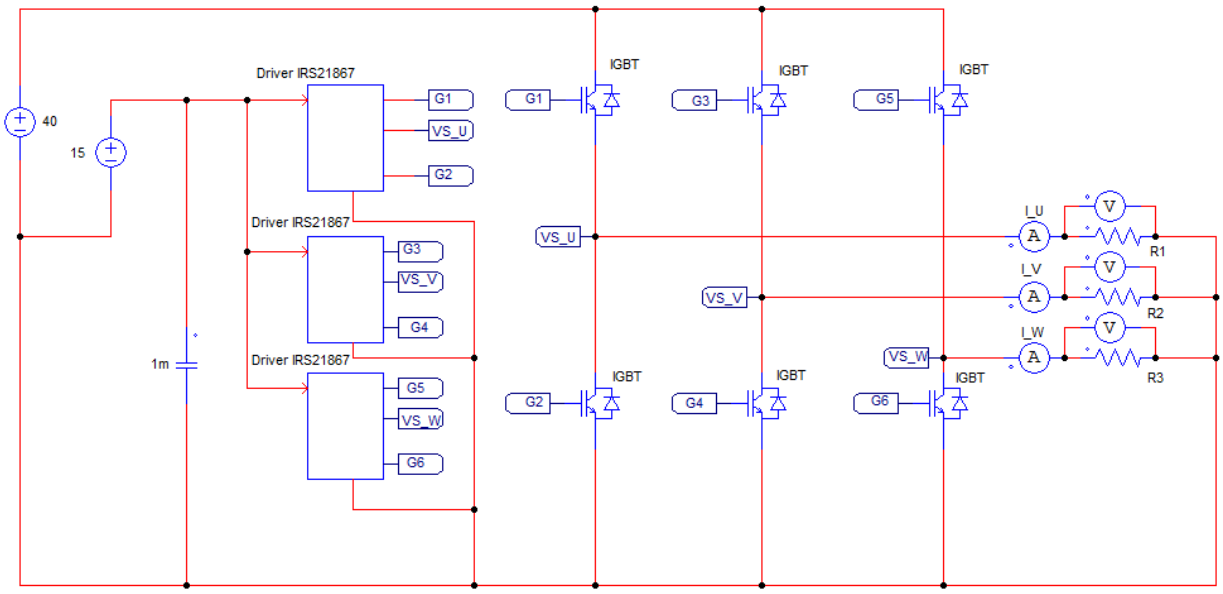


Figure 60: Test Design of Gate Driver and Inverter

Figure 61 shows the gate driver and its connections. The gate driver $IRS21867$ is able to run two IGBTs, as opposed to six IGBTs for the selected hardware gate driver. Furthermore, the hardware gate driver has an internal diode, and simulation gate driver has an external diode. The diode $D1$ and capacitor $C1$ represents the bootstrap circuit of the gate driver. The pulse signals $Vp*$ and Vp represent the DSP board in the simulation design. The probes VBs, VHO, and VLO measures the output signals.

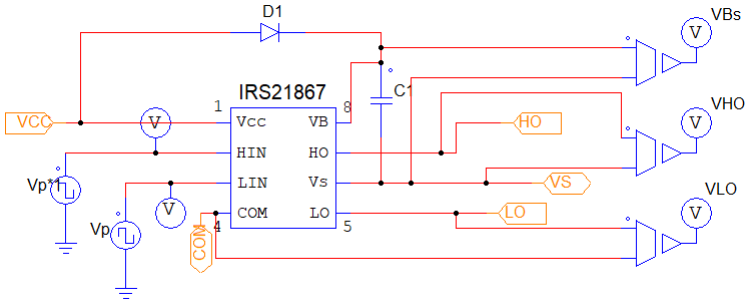


Figure 61: Subcircuit of Gate Driver

Table 8 shows the inputs and outputs of the gate driver. Note that the reference point of the listed parameter

varies. The measurement of the simulation and the hardware needs to have the same reference point to get comparable results. All measurements done when testing the gate driver and IGBT are referenced as listed below unless otherwise is specified.

Parameter	Description	Reference	Operating Range
VCC	Low Side Power Supply	VCC *vs.* VSS (Ground)	$10 - 17.5\ V$
VBS	High Side Positive Power Supply	VB *vs.* VS	$10 - 17.5\ V$
HIN	High Side Logic Input	VHIN *vs.* VSS	$0 - 5\ V$
HO	High Side Gate Driver Output	VHO *vs.* VS	$0 - VBS$
LIN	Low Side Logic Input	VLIN *vs.* VS	$0 - 5\ V$
VS	High Side Negative Power Supply	VS *vs.* VSS	$V_{cc} - V_{BS} - 1$ to $500\ V$
LO	Low Side Gate Driver Output	VLO *vs.* VCOM	$0 - VCC$
COM	Low Side Gate Driver Reference	VCOM *vs.* VSS	$-2.5 - 2.5\ V$

Table 8: Parameters Simulation Gate Driver [A.5]

7.3 Rectifier and Filter Test Design

Figure 62 shows the PSIM model for the rectifier and filter test setup. Two separate systems are simulated for the test. Initially, the system without a filter is simulated. The filter is then implemented into the same system and simulated. The results are then compared to analyse the filter and its function. The resistances $R1$ and $R2$ are implemented to make the input rectifier current similar to the one in the hardware test setup. The forward voltage and resistor of the rectifier diodes are set to 1.26 V and 7.9 mΩ respectively. The specifications of the rectifier are shown in [A.1]. The implemented filter have a 3.9 mH inductor L and four 1 mF capacitors C which is the same values as the hardware components. The resistances $R3$ and $R4$ are implemented as a load.

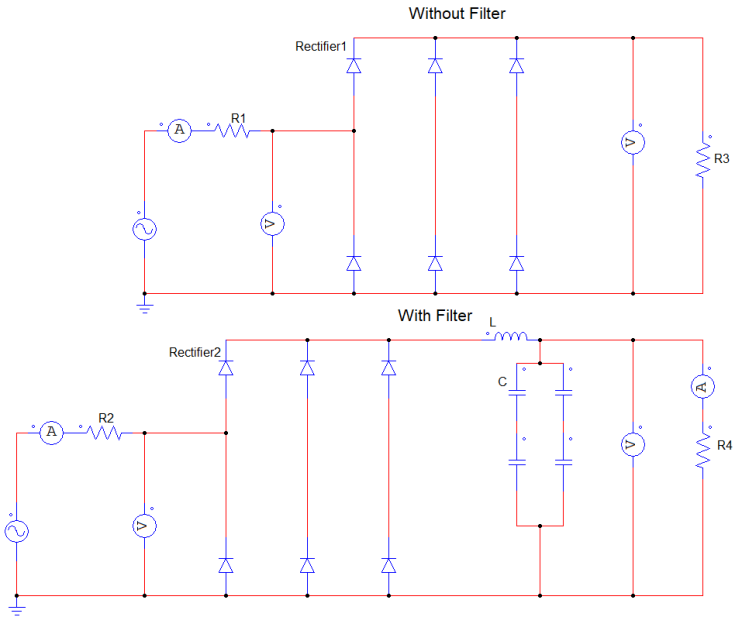


Figure 62: Rectifier and Filter Test Design

8 Results

This section presents the results. The hardware results is compared to test design simulations results in Section 8.1. Section 8.2 presents the simulations of the motor while running with the designed software controller.

8.1 Hardware Setup

Figure 63 shows the designed PMSM controller. The PMSM is removed and replaced with one resistance per phase during the individual component tests. The DSP, gate driver circuit and inverter are tested separately to verify the control part of the design. Furthermore, the rectifier and filter tests are carried out to verify the filter function. The test setup uses external power supplies. This makes it possible to monitor the current flowing through the components.

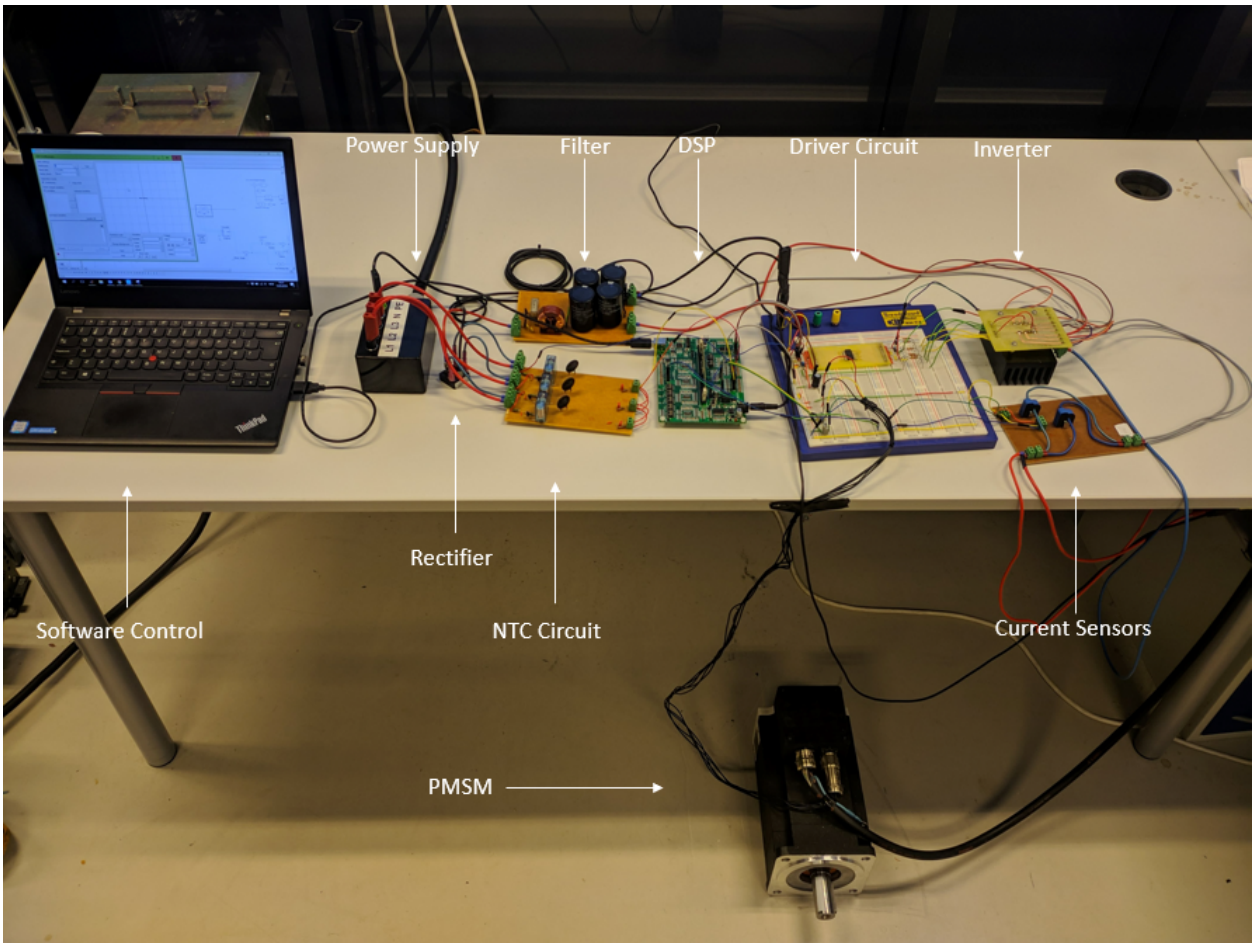


Figure 63: Hardware Setup

The simulation designs presented in Section 7 is compared to the hardware measurements to verify the components. The model presented in Section 7.2 is used to test the DSP, gate driver, and inverter. The setup from Section 7.3 is used for the rectifier and filter test. The hardware components are set up and run the same way as the simulation tests in the tests described below.

8.1.1 DSP and Gate Driver Test

Figure 64 shows the simulation results of the high input HIN and low input LIN gate driver signals. As expected, the simulation shows a high and low input 5 V PWM signal acting opposite to each other. The input signal of the hardware gate driver is shown in Figure 65. The DSP Development board sends the PWM signals. The yellow signal is HIN and the blue signal is LIN. Opposite behaviours are observed while running the gate driver. Note that a slightly higher peak signal Vpp is measured Figure 65. However, the signals of 5.6 V and 5.52 V are well within the maximum limits (-1 to 10 V) of HIN and LIN [A.5]. The comparison of the two figures shows that the signal from the DSP into the gate driver runs as expected. All measured values from the figures below are referenced to COM.

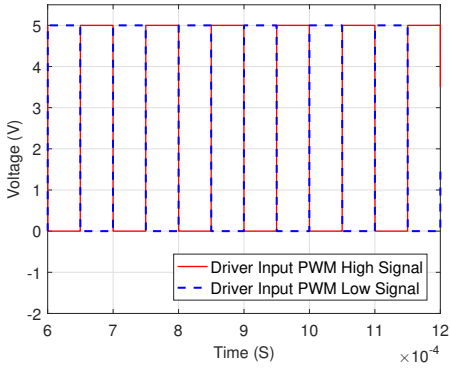


Figure 64: Gate Driver Input PWM Signals HIN and LIN Simulation (Phase A)

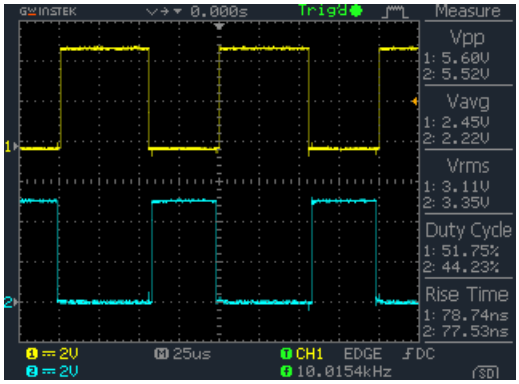


Figure 65: Gate Driver Input PWM Signals HIN and LIN Hardware (Phase A)

Figure 66 shows the simulation results of the output PWM gate driver signals HO. The results show a 13.64 V output gate driver pulse signal. Figure 67 shows the hardware high output pulse signal HO. The simulation results and hardware results show a similar behaviour. However, the hardware voltage shows a higher amplitude than the simulated voltage. In the simulation, the pulse signal has an amplitude of 13.02 V and the amplitude of the hardware voltage is 15.4 V for HO. Considering that a different gate driver is used for the simulation and that all components and values are considered ideal, some deviation of amplitude is expected.

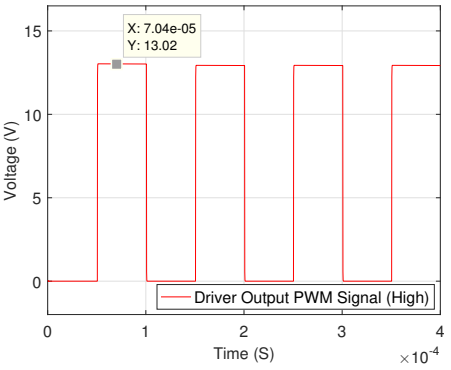


Figure 66: Simulated Output Gate Driver Signal HO Referenced to VS (Phase A)

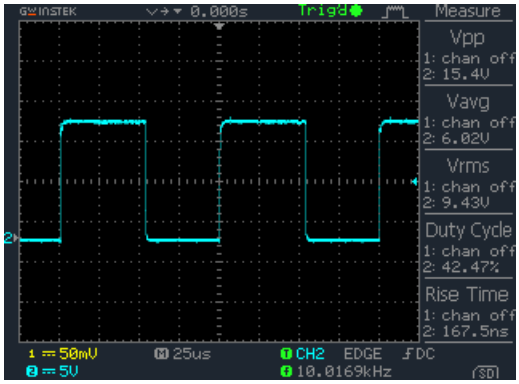


Figure 67: Hardware Output Gate Driver Signal HO Referenced to VS (Phase A)

Both high output HO and and low output LO gate driver signals are referenced to COM and measured simultaneously to illustrate the behaviour of the hardware system. Figure 68 shows the results. Channel 1 (yellow) is HO and channel 2 (blue) is LO. The figure illustrates that the high and low output gate driver signal act opposite to each other, which is expected. HO reaches a peak voltage of 76 V. The software *WebPlotDigitizer* made it possible to approximate amplitude of the PWM signals (excluding the peak). The amplitude was approximately 53 V. The PWM signal of LO referenced to COM reached an amplitude of 16.0 V. The LO signal corresponds to the values specified in the data sheet, but the value of HO referenced to COM is not specified. Simulations was used to verify this behaviour. The results from the simulation in Figure 69 shows an amplitude of 52.07 V on the PWM signal.

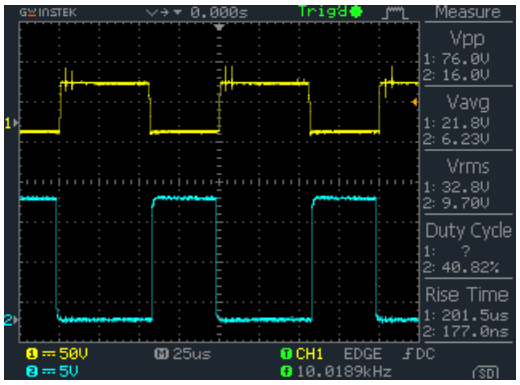


Figure 68: HO and LO Referenced to COM (Phase A)

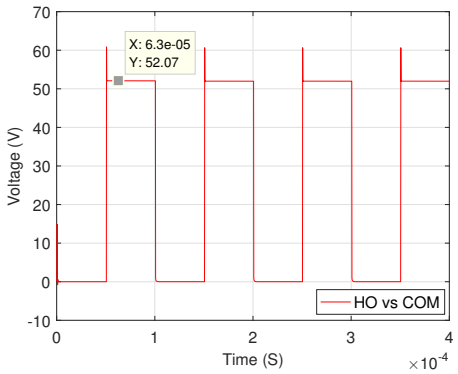


Figure 69: Simulated HO Referenced to COM

8.1.2 Inverter Test

Figure 70 shows the IGBT measurements. For verification, all the IGBT were probed individually to analyse their behaviour.

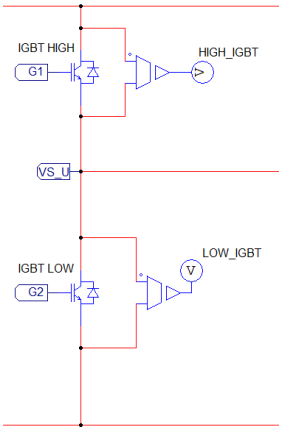


Figure 70: IGBT Measurement

Figure 71 shows the simulation result of the high IGBT signal. The PWM signal reaches an amplitude of 40 V when running the test simulation. As shown in Figure 72, the measured IGBT signal has an amplitude of 44.8 V. As expected, the simulation and hardware measurement deviates moderately. However, the results show similar behaviour.

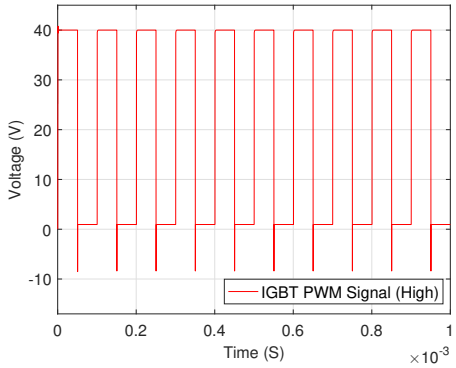


Figure 71: Simulated High IGBT Signals

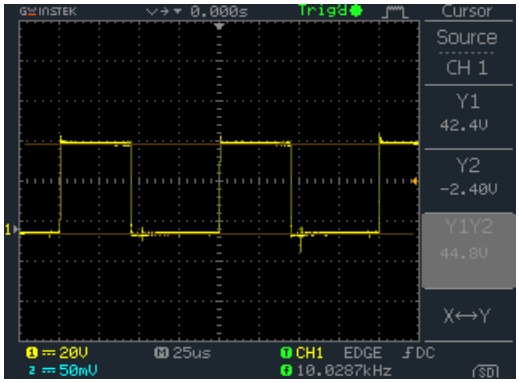


Figure 72: Hardware High IGBT Signal

8.1.3 Rectifier and Filter Test

Figure 73 shows simulation results from the rectifier and filter test. The results show the waveforms of the output voltage with and without a filter implemented into the system. The the peak and rms of the waveforms without a filter shows 6.768 V and 3.276 V respectively. Furthermore, the results with a filter show a 3.503 V peak and 3.274 V rms.

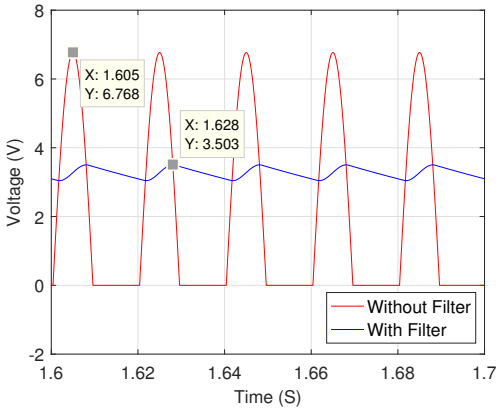


Figure 73: Simulation Results Rectifier and Filter

The hardware rectifier and filter were tested simultaneously to verify its function. Figure 74 and 75 shows the results without and with a filter respectively.

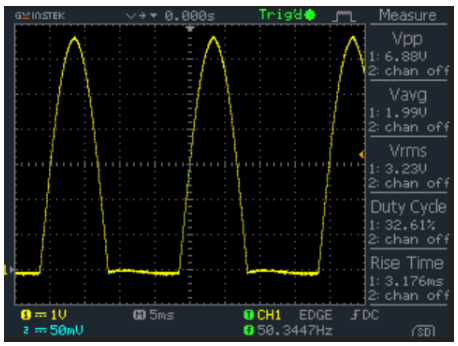


Figure 74: Output Voltage Signal without Filter

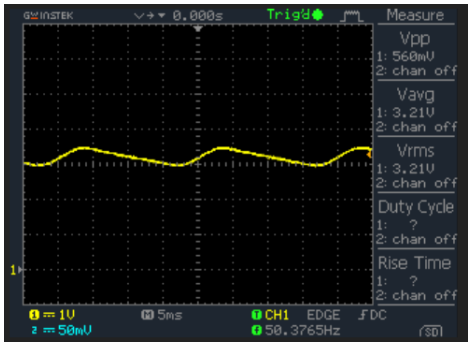


Figure 75: Output Voltage Signal with Filter

Setup	**Simulation [V]**	**Hardware [V]**	**Deviation [%]**
Without Filter	$V_p = 6.768$, $V_{rms} = 3.276$	$V_p = 6.88$, $V_{rms} = 3.23$	$V_p = 1.63$, $V_{rms} = -1.424$
With Filter	$V_p = 3.503$, $V_{rms} = 3.274$	$V_p = 3.56$, $V_{rms} = 3.21$	$V_p = 1.601$, $V_{rms} = -1.994$

Table 9: Simulation and Hardware Comparison

Table 9 shows the values of both the simulation and hardware results. The comparison of the values shows a deviation below 2 % in both cases. This is considered sufficient for this test.

8.1.4 NTC Bypass Circuit Test

To test the NTC bypass circuit, 2.56 V is sent through the thermistor. Simultaneously, a pulse signal is applied to activate the relay and provide a bypass path around the thermistor. When the bypass is activated, the alternative path is connected directly to the ground. As a result, 0 V is measured. Figure 76 shows the voltage measurements in this test. The results show that the bypass circuit works as expected.

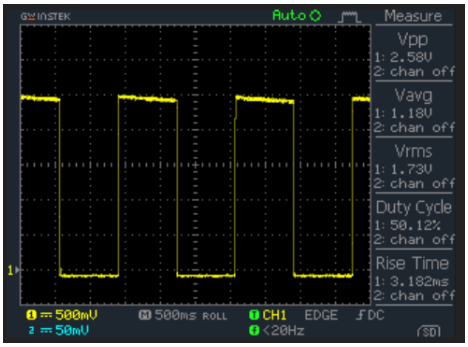


Figure 76: NTC Signal Results

8.2 Modelling of FOC-Based-PMSM

Three different simulation cases are created to test the motor and the controller. The model consists of the frequency converter from Figure 18 and the motor controller from Figure 47. A speed ramp with 1000 $\frac{rpm}{s}$ rise are used in all three cases. A tachometer which only measures rpm is available for the speed measurement in future tests. In addition, the speed specifications in the data sheets are given in rpm. As a result, the cases are defined with rpm values. However, the results are presented in $\frac{rad}{s}$.

- **Case 1 (No-Load):** Motor speed from 0 rpm to 2426 rpm. 0 Nm motor load.
- **Case 2 (Variable Speed):** Motor speed 800 rpm, 1600 rpm and 2489 rpm. 0 Nm motor load.
- **Case 3 (Full-Load):** Motor speed from 0 rpm to 2426 rpm. 9.18 Nm motor load (rated torque).

8.2.1 Case 1 (No-Load)

Case 1 is created to test the motor's ability to stabilise at one constant speed, after a speed ramp. This test is without any motor load. Figure 77 shows a 3.5 s simulation of Case 1. The results show that the motor speed stabilises at 254.05 $\frac{rad}{s}$ (2426 rpm) after 2.426 s.

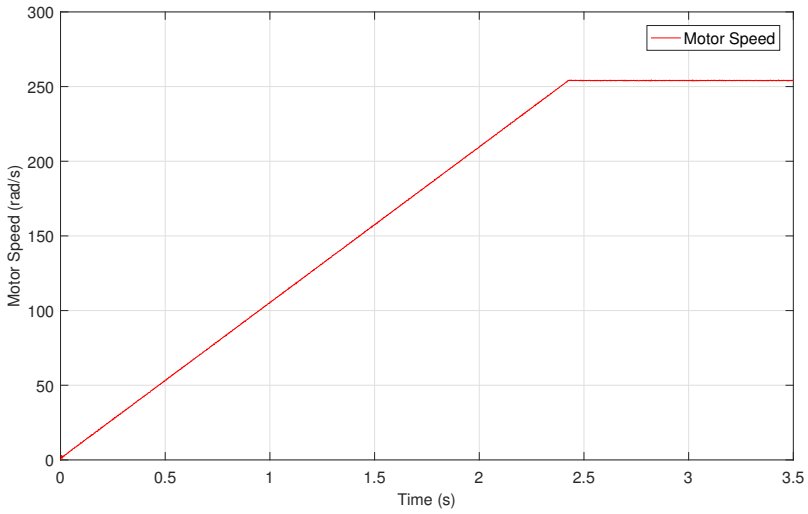


Figure 77: Motor Speed at Case 1

Figure 78 shows a closer look at constant motor speed. The figure shows two error lines which is a percentage of the reference motor speed. The lines visualises the area of deviation. The deviation of the speed in Case 1 is at highest 0.11 %. The motor phase currents I_{adc} have an average rms of 0.24 A from 0 $\frac{rad}{s}$ to 254.05 $\frac{rad}{s}$ and 0.28 A at constant speed.

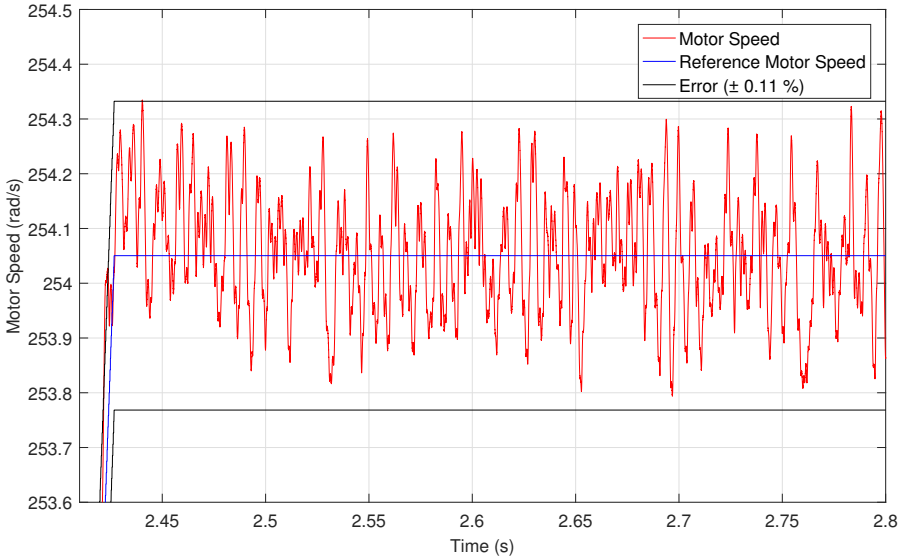


Figure 78: Deviation of Motor Speed at Case 1

8.2.2 Case 2 (Variable Speed)

In Case 2, a no-load test with variable speeds are completed to test if the motor can run at all speeds and change the speeds smoothly. Figure 79 shows the results from the test. Three different ramp characteristics are implemented on the motor. The speed is increased up to 83.78 $\frac{rad}{s}$, 167.55 $\frac{rad}{s}$ and 260.65 $\frac{rad}{s}$. Between each step, the speed stabilises. The speed is then decreased with the same characteristics.

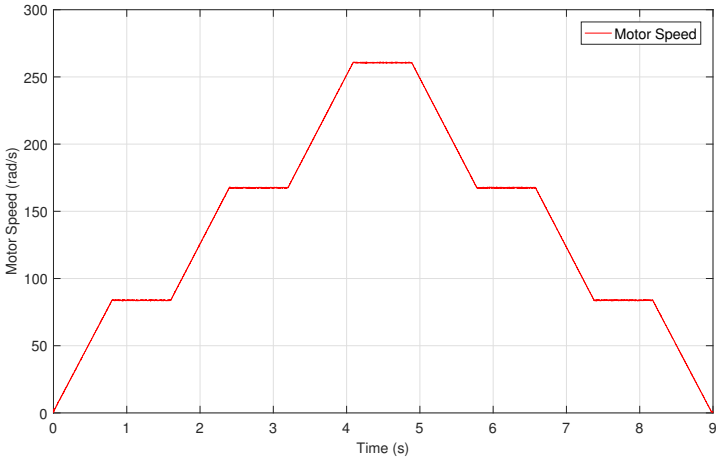


Figure 79: Motor Speed at Case 2

The accuracy of the different speeds is highlighted below. Figure 80 shows a deviation of 0.42 %. Figure 81 shows a 0.27 % deviation at stabilised speed. Figure 82 shows a deviation 0.155 %. The motor phase currents of the speeds 83.78 $\frac{rad}{s}$, 167.55 $\frac{rad}{s}$, and 260.65 $\frac{rad}{s}$ are 0.20 A, 0.26 A, and 0.30 A respectively.

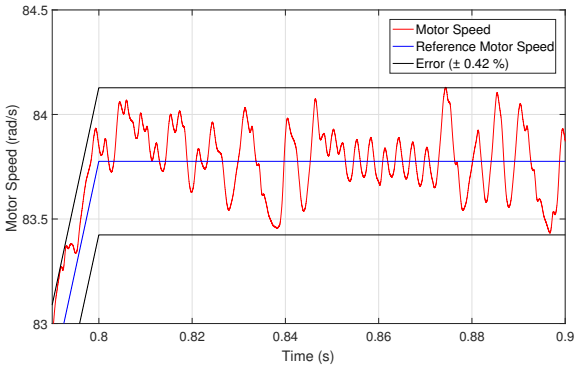


Figure 80: Motor Speed at 83.78 $\frac{rad}{s}$

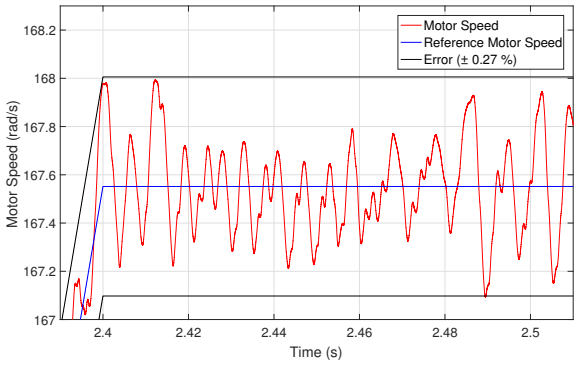


Figure 81: Motor Speed at 167.55 $\frac{rad}{s}$

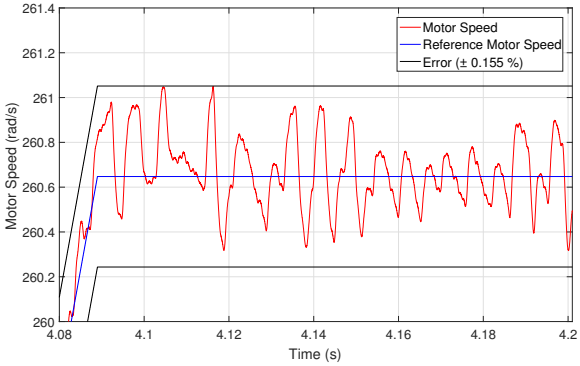


Figure 82: Motor Speed at 260.65 $\frac{rad}{s}$

8.2.3 Case 3 (Full-Load)

Case 3 is completed to verify that the motor can run at rated power, which is 2.332 kW at 545 VDC according to Section 4.3. As shown in Figure 83 the torque is set to 9.18 Nm with a speed ramp from 0 to 254.05 $\frac{rad}{s}$ in 2.426 s. The speed is then set to be constant.

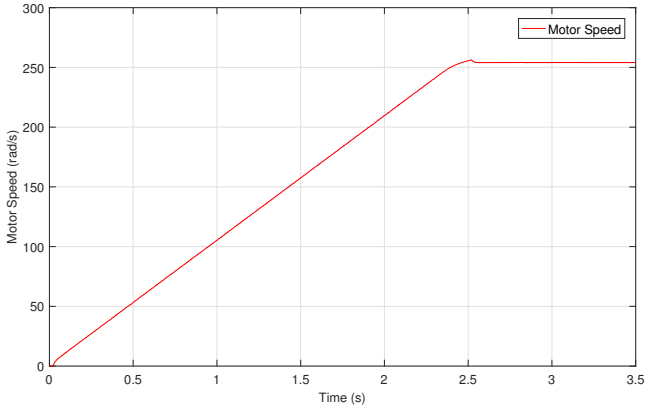


Figure 83: Motor Speed at Case 3

Figure 84 shows a close-up of the motor speed when stabilised. The speed has an overshoot of 0.84 % before stabilising with an error of ± 0.05 %. The average motor phase currents with full-load are 3.71 A at the ramp segment and 3.60 A at constant speed.

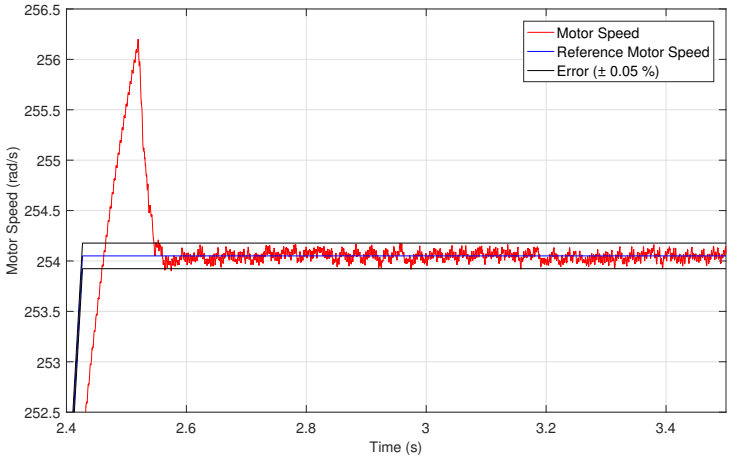


Figure 84: Deviation of Motor Speed at Case 3

9 Discussion

Using PSIM based software and hardware resulted in a stable communication between the DSP and software while running the tests. Adjusting the control design and generating the code led to an immediate update in the code imported into CCS. The DSP development board made the system flexible and easy to use. However, initially the PSIM environment had a relatively steep learning curve. Converting the simulation into SimCoder and learning how to use CCS proved to be a time consuming process.

Case 1, Case 2, and Case 3 was designed to test the PMSM with the designed controller and compare the test and simulation results. However, the fully assembled controller which includes the PMSM was not tested due to the time limit. That said, the designed controller was imported into the DSP when testing the gate driver and inverter. The hardware and simulation results are discussed separately below.

9.1 Hardware Setup

Mounting the components on veroboards when possible made the design more flexible. The filter, NTC circuit and current sensors are all mounted on veroboards. The gate driver is a surface mount component. Furthermore, the ports of the inverter make it challenging to mount it on veroboards. As a result, the gate driver and inverter were mounted on PCBs. The rectifier did not require a veroboard or PCB. The resistances and capacitors needed for the gate driver circuit were either provided in the data sheets or calculated.

Different tests were carried out to verify the controller to get a better understanding of the individual behaviour of the components. However, there are some limitations for the results. Only one phase were tested at a time with a function generator in the rectifier and filter test. As a result, the ripple value is not comparable with the ripple calculation shown in Section 3.2. However, the results verifies the functionality and behaviour of the filter. In general, there are some amplitude differences observed when comparing the simulation and hardware results. This is expected since the parameters of the hardware and software components are not identical. Note that the purpose of the test setups was to verify the behaviour of the components. Running the PMSM while measuring the controller components will give a proper comparison of the measured values and the motor simulation results presented in Section 8.2.

Note that the transients observed in Figure 69 and 71 have an arbitrary amplitude. All the necessary parameters for the IGBT elements were not available in the data sheets. This includes the emitter-collector voltage V_{ec} which affects the transient in the simulation. As a result, V_{ec} was set to 15 V to illustrate the presence of transients in the simulation results. Obtaining the missing parameters through tests is required to analyse the transient behaviour further.

The measured output gate driver signals HO and LO was close to identical. Furthermore, the signals was measured separately with the oscilloscope due to their different reference point. Considering the similarity of the signals, only HO is presented in the results, while the LO measurement is available in [C]. This also applies to the inverter test.

The inverter, rectifier, filter and NTC bypass tests were carried out under controlled environments. Using external power supplies made it possible to monitor all currents going through the components. The downside of this setup is that the components might act differently when applying rated voltage to the design. The

behaviour matches the simulations, but further tests with rated values need to carried out to fully verify the components. The DSP and gate driver tests, however, was tested with rated values and the results show expected behaviour.

9.2 Modelling Discussion

The correlation between the speed and torque was kept in the continuous operation area which was introduced in Section 4.3. The results and observation are discussed below.

The results from the motor simulation shows that the motor reaches its reference speed in all the introduced cases. Cases 1 and 3 shows a low deviation. However, Case 2 shows a higher deviation. The results indicate that the percentage of error decreases as the speed approaches its rated value. This is particularly evident in Case 2 where the deviation of the lowest and highest speed differs by 0.265 %. The controller was tuned to be as precise as possible at rated speed. As a result, a higher deviation was observed when running the motor at lower speeds.

The results from Case 3 shows a speed overshoot of 0.84 %. Initially, running the motor on no-load conditions was a prioritised over full-load conditions. As a result, the controller was tuned to be as efficient as possible under no-load conditions. The overshoot observed in Case 3 may be a result of the no-load conditions priority in the tuning process. The overshoot can be reduced by running and adjusting the controller under full-load conditions. However, this affects the no-load conditions results which is the first priority at this stage of the project. That said, the deviation of ± 0.05 % in Case 3 is about half of the deviation of ± 0.11 % observed in case one, and the speed overshoot is for a brief time period.

9.3 Future Work

Running the motor with PSIM is the main objective in future work. Considering the results from the individual tests, it is expected that the controller will be able to run the PMSM.

PMSMs reaches the rated torque independently of its speed when they run below rated speed. However, exceeding the rated speed introduces some challenges. The available torque will be reduced when the motor exceeds its rated speed. In addition, the terminal voltage (imposed by the inverter constraints) exceeds its maximum allowable value. Introducing a negative d-axis current on the controller will reduce the terminal voltage. The resulting voltage drop will counterbalance the electromotive force generated by the rotor flux [38]. This operation is called field weakening control and makes it possible to obtain the maximum torque available at speeds above its rated value [39]. In future research, the introduction of field weakening control in will lead to additional experiments and research.

10 Conclusion

In this thesis, a PSIM-based controller for an inverter-fed PMSM was dimensioned and designed. The majority of the report addresses the software design needed to implement the controller to the PMSM. The project outputs and requirements were listed in the problem statement. The progress of the research is summarised below.

1. The frequency converter was dimensioned for a 2.332 kW PMSM. The simulation model proved to be efficient when dimensioning the inductor, capacitor, NTC element, and the snubber. The data sheets provided sufficient information to dimension the rectifier, inverter, gate driver, cooling elements, and current sensors.

2. The PSIM based simulation model was presented in two parts. The first part was the frequency converter and motor. The second part was the control algorithm that controls the speed of the motor. The dimensioned components was implemented to get as realistic results as possible. Creating the model introduced the opportunity of analysing the behaviour of the entire frequency converter by simulations. Tuning the controller to get adequate results proved to be a comprehensive process.

3. Converting the PSIM model into SimCoder made it possible to run the frequency converter through the PSIM model. The conversion included swapping out the PSIM components that were incompatible with the code generation with compatible ones. Generally, the conversion process was straightforward. However, implementing the encoder and tuning it was challenging.

4. The filter, NTC circuit, and current sensors were soldered on veroboards. PCB designs were the best solution for the gate driver and inverter. The rectifier did not need any board design. Designing the gate driver circuit on a prototype breadboard made the system more flexible and made it possible to test different resistances.

5. Importing the code into CCS required much testing with PSIM example designs to make it work as expected. The current sensors were calibrated to match the DSP measurements.

6. The components of the frequency converter were tested individually. The measured hardware signals and the test simulation results show similar behaviour. The amplitudes of the components can be verified by running additional tests in rated conditions.

Using PSIM to design and run the frequency converter was an educational process although the software had a steep learning curve. Running the individual components with PSIM through the DSP development board was easy and intuitive ones the system was designed. The low cost and open system design of the software make it a good alternative in future research.

A full-scale test of the frequency converter with all the rated value can be conducted to fully verify the design. Comparing the measured values with the full-scale simulation results presented in Section 8.2 may verify the design functionality further. The design introduces research opportunities for the control algorithm. The controller can be improved by implementing field weakening control into the design to run the PMSM at higher than rated value speeds.

References

[1] J. F. Gieras, *Permanent magnet motor technology: design and applications*. CRC press, 2002, pp. iii–16.

[2] W. Li, C. Abbey, and G. Joós, "Control and performance of wind turbine generators based on permanent magnet synchronous machines feeding a diode rectifier," in *IEEE Power Electronics Specialists Conference*, vol. 2, 2006, pp. 1–6.

[3] Z. Jian, W. Xuhui, and Z. Lili, "Optimal system efficiency operation of dual pmsm motor drive for fuel cell vehicles propulsion," in *Power Electronics and Motion Control Conference, 2009. IPEMC'09. IEEE 6th International*, IEEE, 2009, pp. 1889–1892.

[4] *Certification summary information report*, JTSLV00.0L13-002, epa certificate tesla model 3, epa, Dec. 2017.

[5] M. T. Elsayed, O. A. Mahgoub, and S. A. Zaid, "Simulation study of a new approach for field weakening control of pmsm," *Journal of power electronics*, vol. 12, no. 1, pp. 136–144, 2012.

[6] N. Mohan, *Electric Machines and Drives*, 1st ed. 2012, ISBN: 9781118074817.

[7] B. K. Bose, "Energy, environment, and advances in power electronics," *IEEE Transactions on Power Electronics*, vol. 15, no. 4, pp. 688–701, 2000.

[8] J. Bocker and S. Mathapati, "State of the art of induction motor control," in *Electric Machines & Drives Conference, 2007. IEMDC'07. IEEE International*, IEEE, vol. 2, 2007, pp. 1459–1464.

[9] H. Sira-Ramírez, J. Linares-Flores, C. García-Rodríguez, and M. A. Contreras-Ordaz, "On the control of the permanent magnet synchronous motor: An active disturbance rejection control approach," *IEEE Transactions on Control Systems Technology*, vol. 22, no. 5, pp. 2056–2063, 2014.

[10] M. Donsión, "Parameters influence on the control of a pmsm," in *ISEF 2007-XIII International Symposium on Electromagnetic Fields in Mechatronics, Electrical and Electronic Engineering*, 2007, pp. 13–15.

[11] C. Morkoç, Y. Önal, and M. Kesler, "Dsp based embedded code generation for pmsm using sliding mode controller," in *Power Electronics and Motion Control Conference and Exposition (PEMC), 2014 16th International*, IEEE, 2014, pp. 472–476.

[12] N. Instruments. (2013). Supported motor types, [Online]. Available: `http://zone.ni.com/reference/en-XX/help/374169A-01/lvemsimshared/motor_type/` (visited on 09/27/2017).

[13] P. C. Perera, *Sensorless control of permanent-magnet synchronous motor drives*. Institute of Energy Technology, Aalborg University, 2002.

[14] T. M. Jahns, G. B. Kliman, and T. W. Neumann, "Interior permanent-magnet synchronous motors for adjustable-speed drives," *IEEE Transactions on Industry Applications*, no. 4, pp. 738–747, 1986.

[15] K. Akatsu, K. Narita, Y. Sakashita, and T. Yamada, "Characteristics comparison between spmsm and ipmsm under high flux density condition by both experimental and analysis results," in *Electrical Machines and Systems, 2008. ICEMS 2008. International Conference on*, IEEE, 2008, pp. 2848–2853.

[16] L. He, J. Ma, Y. Fang, and S. Liang, "An improved method to estimate initial rotor position for surface-mounted permanent magnet synchronous motors," in *Electrical Machines and Systems (ICEMS), 2014 17th International Conference on*, IEEE, 2014, pp. 2050–2054.

[17] W. T. Thomson and M. Fenger, "Current signature analysis to detect induction motor faults," *IEEE Industry Applications Magazine*, vol. 7, no. 4, pp. 26–34, 2001.

[18] E. PUMPS. (2017). Ac induction motors vs. permanent magnet synchronous motors, [Online]. Available: http://empoweringpumps.com/ac-induction-motors-versus-permanent-magnet-synchronous-motors-fuji/ (visited on 11/13/2017).

[19] G. Kohlrusz and D. Fodor, "Comparison of scalar and vector control strategies of induction motors," *Hungarian Journal of Industry and Chemistry*, vol. 39, no. 2, pp. 265–270, 2011.

[20] D. Jee and N. Patel, "V/f control of induction motor drive," PhD thesis, 2013.

[21] E. DISTRELEC. (2017). Brolikeretter, trefaset 600 v 25 a 26mt60pbf, vishay, [Online]. Available: https://www.elfadistrelec.no/no/brolikeretter-trefaset-600-25-vishay-26mt60pbf/p/17036205?q=brolikeretter&page=4&origPos=4&origPageSize=50&simi=95.97 (visited on 10/04/2017).

[22] D. Tardiff and T. Barton, "A summary of resonant snubber circuits for transistors and gtos," in *Industry Applications Society Annual Meeting, 1989., Conference Record of the 1989 IEEE*, IEEE, 1989, pp. 1176–1180.

[23] N. Mohan, *Power electronics: a first course*. Wiley, 2011, pp. 113–114.

[24] S. Pyakuryal and M. Matin, "Filter design for ac to dc converter," *International Refereed Journal of Engineering and Science (IRJES)*, vol. 2, no. 6, pp. 42–49, 2013.

[25] infineon. (2017). Easypack 750 600v sixpack igbt module with igbt3 and ntc, [Online]. Available: https://www.infineon.com/cms/en/product/power/igbt/igbt-module/igbt-module-600v-650v/FS10R06VE3_B2/productType.html?productType=ff80808112ab681d0112ab6eb4921d7c (visited on 10/10/2017).

[26] ——, (2017). Eicedriver compact - full bridge 3 phase gate driver ic with ls-soi technology to control power devices like mos-transistors or 600v igbts, [Online]. Available: https://www.infineon.com/cms/en/product/power/gate-driver-ics/level-shift-gate-drivers/three-phase-drivers/6edl04n06pt/?productType=db3a30443004528501306 43e046d300b# (visited on 11/07/2017).

[27] M. H. Rashid, *Power electronics handbook*. Butterworth-Heinemann, 2017, p. 546.

[28] Elfadistrelect. (2017). Kjoleelement 100 mm 1.5 k/w svart anodisert, sk 100/100 sa, fischer elektronik, [Online]. Available: https://www.elfadistrelec.no/no/kjoleelement-100-mm-svart-anodisert-fischer-elektronik-sk-100-100-sa/p/17560430?q=kj%5C%C3%5C%B8leelement&page=4&origPos=119&origPageSize=50&simi=95.88 (visited on 10/10/2017).

[29] R. Components. (2018). Lem lts series closed loop current sensor, 0 → ±19.2a, [Online]. Available: https://uk.rs-online.com/web/p/current-transducers/4362330/ (visited on 04/22/2017).

[30] Microsemi. (2013). Park, inverse park and clarke, inverse clarke transformations mss software implementation, [Online]. Available: https://www.microsemi.com/document-portal/doc_view/132799-park-inverse-park-and-clarke-inverse-clarke-transformations-mss-software-implementation-user-guide (visited on 11/01/2017).

[31] B. Akin, M. Bhardwaj, and J. Warriner, "Sensorless field oriented control of 3-phase permanent magnet synchronous motors," *Texas Instruments, Application Notes*, 2013.

[32] I. Freescale Semiconductor. (2016). Sensorless pmsm field-oriented control, [Online]. Available: https://cache.nxp.com/docs/en/reference-manual/DRM148.pdf (visited on 11/01/2017).

[33] POWERSIM. (2016). Tutorial:motor control design suite, [Online]. Available: https://powersimtech.com/drive/uploads/2017/11/Tutorial-Motor-Control-Design-Suite-11.1.pdf (visited on 11/20/2017).

[34] N. Instruments. (2018). Reading encoders, [Online]. Available: https://learn.ni.com/teach/resources/117/reading-encoders (visited on 05/10/2018).

[35] *Tms320x280x, 2801x, 2804x enhanced quadrature encoder pulse (eqep) module*, SPRU790D, Revised 2008, Texas Instruments, Dec. 2008.

[36] *Dsp development board user's manual*, Version 1, POWERSIM INC., Nov. 2016.

[37] T. Instruments. (2017). Fundamentals of mosfet and igbt gate driver circuits, [Online]. Available: http://www.ti.com/lit/ml/slua618/slua618.pdf (visited on 05/23/2018).

[38] M. Preindl and S. Bolognani, "Model predictive direct torque control with finite control set for pmsm drive systems, part 2: Field weakening operation," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 648–657, 2013.

[39] M. Zordan, P. Vas, M. Rashed, S. Bolognani, and M. Zigliotto, "Field-weakening in high-performance pmsm drives: A comparative analysis," vol. 3, pp. 1718–1724, 2000.

Appendix A Data Sheets

A.1 Rectifier

Three Phase Bridge (Power Modules), 25/35 A

D-63

FEATURES

- Universal, 3 way terminals: push-on, wrap around or solder
- High thermal conductivity package, electrically insulated case
- Center hole fixing
- Excellent power/volume ratio
- UL E300359 approved
- Gold plated terminals solderable using lead (Pb)-free solder; solder alloy Sn/Ag/Cu (SAC305); solder temperature 260 to 275 °C
- RoHS compliant
- Designed and qualified for industrial and consumer level

RoHS COMPLIANT

DESCRIPTION

A range of extremely compact, encapsulated three phase bridge rectifiers offering efficient and reliable operation. They are intended for use in general purpose and instrumentation applications.

PRODUCT SUMMARY	
I_O	25/35 A

MAJOR RATINGS AND CHARACTERISTICS				
SYMBOL	CHARACTERISTICS	26MT	36MT	UNITS
I_O		25	35	A
	T_C	70	60	°C
I_{FSM}	50 Hz	360	475	A
	60 Hz	375	500	
I^2t	50 Hz	635	1130	A^2s
	60 Hz	580	1030	
V_{RRM}		100 to 1600		V
T_J		- 55 to 150		°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM} MAXIMUM AT T_J MAXIMUM mA
26MT../36MT..	10	100	150	2
	20	200	275	
	40	400	500	
	60	600	725	
	80	800	900	
	100	1000	1100	
	120	1200	1300	
	140	1400	1500	
	160	1600	1700	

FORWARD CONDUCTION

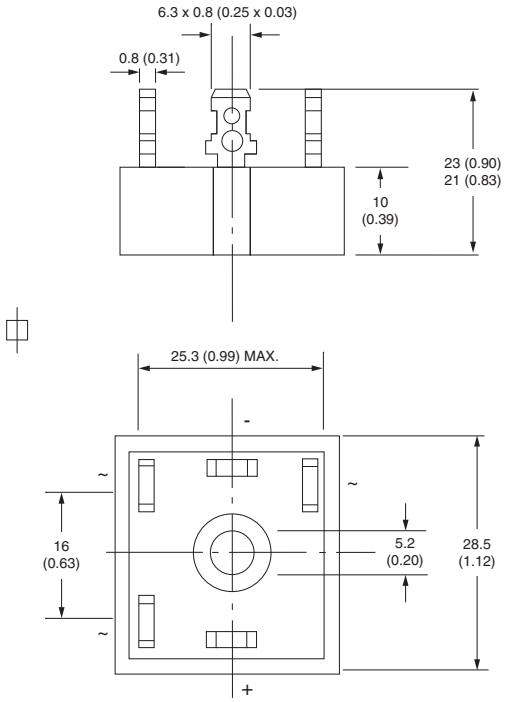
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES 26MT	VALUES 36MT	UNITS
Maximum DC output current at T_C	I_O	120° rect. conduction angle			25	35	A
					70	60	°C
Maximum peak, one-cycle non-repetitive forward current	I_{FSM}	t = 10 ms	No voltage reapplied	Initial $T_J = T_J$ maximum	360	475	A
		t = 8.3 ms			375	500	
		t = 10 ms	100 % V_{RRM} reapplied		300	400	
		t = 8.3 ms			314	420	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		635	1130	A^2s
		t = 8.3 ms			580	1030	
		t = 10 ms	100 % V_{RRM} reapplied		450	800	
		t = 8.3 ms			410	730	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	I^2t for time $t_x = I^2\sqrt{t} \times \sqrt{t_x}$; $0.1 \le t_x \le 10$ ms, V_{RRM} = 0 V			6360	11 300	$A^2\sqrt{s}$
Low level of threshold voltage	$V_{F(TO)1}$	(16.7 % x π x $I_{F(AV)}$ < I < π x $I_{F(AV)}$), T_J maximum			0.88	0.86	V
High level of threshold voltage	$V_{F(TO)2}$	(I > π x $I_{F(AV)}$), T_J maximum			1.13	1.03	
Low level forward slope resistance	r_{t1}	(16.7 % x π x $I_{F(AV)}$ < I < π x $I_{F(AV)}$), T_J maximum			7.9	6.3	mΩ
High level forward slope resistance	r_{t2}	(I > π x $I_{F(AV)}$), T_J maximum			5.2	5.0	
Maximum forward voltage drop	V_{FM}	T_J = 25 °C, I_{FM} = 40 Apk - per single junction			1.26	1.19	V
Maximum DC reverse current	I_{RRM}	T_J = 25 °C, per junction at rated V_{RRM}			100		µA
RMS isolation voltage	V_{INS}	T_J = 25 °C, all terminal shorted; f = 50 Hz, t = 1 s			2700		V

THERMAL - MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES 26MT	VALUES 36MT	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		- 55 to 150		°C
Maximum thermal resistance, junction to case	R_{thJC}	DC operation per bridge (based on total power loss of bridge)	1.42	1.35	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.2	0.2	
Approximate weight			20		g
Mounting torque ± 10 %		Bridge to heatsink with screw M4	2.0		Nm

D-63

DIMENSIONS in millimeters (inches)



Suggested plugging force:
400 N maximum;
axially applied to fast on terminals

Not to scale

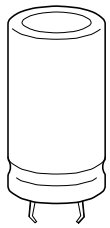
A.2 Capacitor

Aluminum electrolytic capacitors

Snap-in capacitors

Series/Type: **B43305**
Date: November 2008

General-purpose grade capacitors



Applications

- Switch-mode power supplies in industrial and entertainment electronics
- Uninterruptiple power supplies

Features

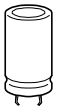
- Voltage derating (0.93 · V_R) enables 105 °C operation, more details available upon request
- Extremely high CV product, ultra compact
- High ripple current capability
- Different case sizes available for each capacitance value
- RoHS-compatible

Construction

- Charge/discharge-proof, polar
- Aluminum case, fully insulated with PVC
- Version with PET insulation available
- Version with additional PET insulation cap on terminal side available for insulating the capacitor from the PCB
- Snap-in solder pins to hold component in place on PC-board
- Minus pole marking on case surface
- Minus pole not insulated from case
- Overload protection by safety vent on the base

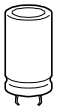
Terminals

- Standard version with 2 terminals, 2 lengths available: 6.3 and 4.5 mm
- 3 terminals to ensure correct insertion: length 4.5 mm



Specifications and characteristics in brief

Rated voltage V_R Surge voltage V_S	200 ... 450 V DC 1.15 · V_R (for $V_R \leq 250$ V DC) 1.10 · V_R (for $V_R \geq 400$ V DC)	
Rated capacitance C_R Capacitance tolerance	68 ... 3300 µF ±20% ≙ M	
Dissipation factor tan δ (20 °C, 120 Hz)	$V_R \leq 250$ V DC: tan δ ≤ 0.15 $V_R \geq 400$ V DC: tan δ ≤ 0.20	
Leakage current I_{leak} (5 min, 20 °C)	$I_{leak} \leq 0.3\ \mu A \cdot \left(\frac{C_R}{\mu F} \cdot \frac{V_R}{V}\right)^{0.7} + 4\ \mu A$	
Self-inductance ESL	Approx. 20 nH	
Useful life 85 °C; V_R; $I_{AC,R}$ 40 °C; V_R; 1.1 · $I_{AC,R}$	 > 2000 h > 100000 h	Requirements: ΔC/C ≤ ±30% of initial value tan δ ≤ 3 times initial specified limit I_{leak} ≤ initial specified limit
Voltage endurance test 85 °C; V_R	2000 h	Post test requirements: ΔC/C ≤ ±10% of initial value tan δ ≤ 1.3 times initial specified limit I_{leak} ≤ initial specified limit
Vibration resistance test	To IEC 60068-2-6, test Fc: Displacement amplitude 0.35 mm, frequency range 10 Hz ... 55 Hz, acceleration max. 5 *g*, duration 3 × 2 h. Capacitor mounted by its body which is rigidly clamped to the work surface.	
Characteristics at low temperature	Max. impedance ratio at 100 Hz	V_R ≤ 250 V; ≥ 400 V $Z_{-25\,°C} / Z_{20\,°C}$: 3; 7 $Z_{-40\,°C} / Z_{20\,°C}$: 7; 14
IEC climatic category	To IEC 60068-1: ■ $V_R \leq 250$ V DC: 40/085/56 (−40 °C/+85 °C/56 days damp heat test) ■ $V_R \geq 400$ V DC: 25/085/56 (−25 °C/+85 °C/56 days damp heat test) The capacitors can be operated in the temperature range of −40 °C to +85 °C but the impedance at −40 °C should be taken into consideration.	
Detail specification Sectional specification	Similar to CECC 30301-806 IEC 60384-4	



Technical data and ordering codes

C_R 100 Hz 20 °C µF	Case dimensions d × l mm	ESR_{typ} 100 Hz 20 °C mΩ	Z_{max} 10 kHz 20 °C mΩ	$I_{AC,max}$ 100 Hz 60 °C A	$I_{AC,R}$ [3] 100 Hz 85 °C A	Ordering code (composition see below)
V_R = 400 V DC						
68	22 × 25	1990	2690	1.28	0.65	B43305A9686M0*#
82	22 × 25	1650	2230	1.41	0.72	B43305A9826M0*#
100	22 × 25	1360	1830	1.55	0.79	B43305A9107M0*#
120	22 × 25	1130	1530	1.70	0.87	B43305A9127M0*#
150	22 × 30	900	1220	1.98	1.01	B43305A9157M0*#
180	22 × 30	750	1020	2.17	1.11	B43305A9187M0*#
180	25 × 25	750	1020	2.18	1.11	B43305B9187M0*#
220	22 × 35	620	830	2.49	1.27	B43305A9227M0*#
220	25 × 30	620	830	2.51	1.28	B43305B9227M0*#
270	22 × 45	500	680	2.92	1.49	B43305A9277M0*#
270	25 × 35	500	680	2.89	1.47	B43305B9277M0*#
270	30 × 25	500	680	2.79	1.42	B43305C9277M0*#
330	22 × 50	410	560	3.31	1.69	B43305A9337M0*#
330	25 × 40	410	560	3.29	1.68	B43305B9337M0*#
330	30 × 30	410	560	3.22	1.64	B43305C9337M0*#
330	35 × 25	410	560	3.04	1.55	B43305D9337M0*#
390	25 × 45	350	470	3.68	1.87	B43305A9397M0*#
390	30 × 35	350	470	3.62	1.85	B43305B9397M0*#
390	35 × 30	350	470	3.67	1.87	B43305C9397M0*#
470	25 × 50	290	390	4.14	2.11	B43305A9477M0*#
470	30 × 40	290	390	4.37	2.23	B43305B9477M0*#
470	35 × 30	290	390	4.03	2.05	B43305C9477M0*#
560	30 × 45	240	330	4.91	2.50	B43305A9567M0*#
560	35 × 35	240	330	4.56	2.32	B43305B9567M0*#
680	30 × 50	200	270	5.55	2.83	B43305A9687M0*#
680	35 × 40	200	270	5.18	2.64	B43305B9687M0*#
820	30 × 55	170	230	6.23	3.18	B43305A9827M0*#
820	35 × 45	170	230	5.85	2.98	B43305B9827M0*#
1000	35 × 50	140	190	6.63	3.38	B43305A9108M0*#

Composition of ordering code

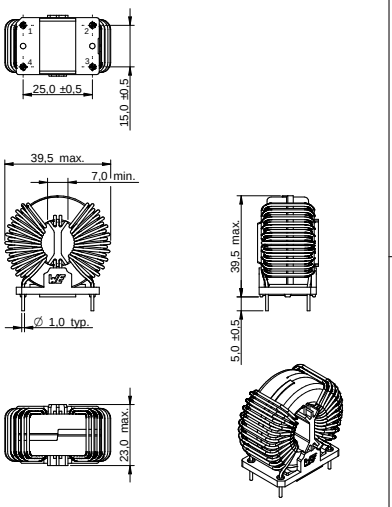
* = Insulation feature
- 0 = PVC insulation
- 6 = PET insulation
- 8 = PVC insulation with additional PET insulation cap on terminal side

\# = Terminal style
- 0 = snap-in standard terminals (6.3 mm)
- 2 = snap-in 3 terminals (4.5 mm)
- 7 = snap-in short terminals (4.5 mm)

3) 120-Hz conversion factor of ripple current: I_{AC} (120 Hz) = 1.03 · I_{AC} (100 Hz)

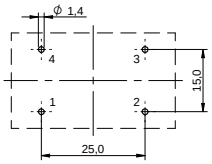
A.3 Inductor

Dimensions: [mm]



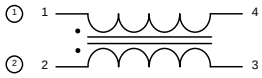
Scale - 1:1,5

Recommended Hole Pattern: [mm]



Scale - 1:1

Schematic:



Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance	10 kHz/ 0.1 mA	L	3.9	mH	±30
Rated Current	@ 70 °C	I_R	8	A	max.
DC Resistance	@ 20 °C	R_{DC}	31	mΩ	max.
Rated Voltage	50 Hz	U_R	760	V (AC)	max.
Insulation Test Voltage	50 Hz/ 5 mA/ 2 sec.	U_T	3000	V (AC)	

General Information:

It is recommeded that the temperature of the component does not exceed +125°C under worst case conditions	
Storage Temperature (in original packaging)	-20 °C up to +60 °C
Operating Temperature	-40 °C up to +125 °C
Temperature Rise < 55K	
Test conditions of Electrical Properties: +20°C, 33% RH if not specified differently	

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Germany
Tel. +49 (0) 79 42 945 - 0

www.we-online.com
eiSos@we-online.com

WÜRTH ELEKTRONIK

CREATED	CHECKED	GENERAL TOLERANCE	PROJECTION METHOD
KaS	HasA	DIN ISO 2768-1m	

DESCRIPTION: **WE-CMB HV Common Mode Power Line Choke**

ORDER CODE: **744830039080**

SIZE	REVISION	STATUS	DATE	BUSINESS UNIT	PAGE
XL	001.000	Valid	2015-11-10	eiSos	1/5

A.4 Inverter

Technische Information / Technical Information

IGBT-Module
IGBT-modules

FS10R06VE3_B2

Vorläufige Daten
Preliminary Data

IGBT,Wechselrichter / IGBT,Inverter

Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 25°C	V_{CES}	600	V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 80°C, $T_{vj\,max}$ = 175°C T_C = 25°C, $T_{vj\,max}$ = 175°C	$I_{C\,nom}$ I_C	10 16	A A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	20	A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, $T_{vj\,max}$ = 175	P_{tot}	50,0	W
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage		V_{GES}	+/-20	V

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	I_C = 10 A, V_{GE} = 15 V I_C = 10 A, V_{GE} = 15 V I_C = 10 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$V_{CE\,sat}$		1,55 1,70 1,80	2,00	V V V
Gate-Schwellenspannung Gate threshold voltage	I_C = 0,30 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	4,9	5,8	6,5	V
Gateladung Gate charge	V_{GE} = -15 V ... +15 V		Q_G		0,10		µC
Interner Gatewiderstand Internal gate resistor	T_{vj} = 25°C		R_{Gint}		0,0		Ω
Eingangskapazität Input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		0,55		nF
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		0,017		nF
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V_{CE} = 600 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			1,0	mA
Gate-Emitter-Reststrom Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	I_C = 10 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Gon} = 27 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,on}$		0,012 0,012 0,012		µs µs µs
Anstiegszeit, induktive Last Rise time, inductive load	I_C = 10 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Gon} = 27 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r		0,009 0,013 0,014		µs µs µs
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	I_C = 10 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Goff} = 27 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,off}$		0,10 0,12 0,125		µs µs µs
Fallzeit, induktive Last Fall time, inductive load	I_C = 10 A, V_{CE} = 300 V V_{GE} = ±15 V R_{Goff} = 27 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_f		0,085 0,13 0,135		µs µs µs
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 10 A, V_{CE} = 300 V, L_S = 60 nH V_{GE} = ±15 V R_{Gon} = 27 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}		0,14 0,20 0,22		mJ mJ mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 10 A, V_{CE} = 300 V, L_S = 60 nH V_{GE} = ±15 V R_{Goff} = 27 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}		0,24 0,30 0,32		mJ mJ mJ
Kurzschlußverhalten SC data	V_{GE} ≤ 15 V, V_{CC} = 360 V V_{CEmax} = V_{CES} -L_{sCE} ·di/dt	t_P ≤ 6 µs, T_{vj} = 150°C	I_{SC}		50		A
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}		2,70	3,00	K/W
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		1,00		K/W
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		150	°C

prepared by: DPK	date of publication: 2013-10-03
approved by: RK	revision: 2.0

Vorläufige Daten
Preliminary Data

Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	600	V
Dauergleichstrom Continuous DC forward current		I_F	10	A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	20	A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C V_R = 0 V, t_P = 10 ms, T_{vj} = 150°C	I²t	12,5 9,50	A²s A²s

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Durchlassspannung Forward voltage	I_F = 10 A, V_{GE} = 0 V I_F = 10 A, V_{GE} = 0 V I_F = 10 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	V_F		1,60 1,55 1,50	2,05	V V V
Rückstromspitze Peak reverse recovery current	I_F = 10 A, - di_F/dt = 1500 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	I_{RM}		18,0 19,0 21,0		A A A
Sperrverzögerungsladung Recovered charge	I_F = 10 A, - di_F/dt = 1500 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	Q_r		0,50 0,85 1,10		µC µC µC
Abschaltenergie pro Puls Reverse recovery energy	I_F = 10 A, - di_F/dt = 1500 A/µs (T_{vj}=150°C) V_R = 300 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}		0,11 0,20 0,26		mJ mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode		R_{thJC}		3,70	4,10	K/W
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		1,90		K/W
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		150	°C

NTC-Widerstand / NTC-Thermistor

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Nennwiderstand Rated resistance	T_C = 25°C	R_{25}		5,00		kΩ
Abweichung von R100 Deviation of R100	T_C = 100°C, R_{100} = 493 Ω	ΔR/R	-5		5	%
Verlustleistung Power dissipation	T_C = 25°C	P_{25}			20,0	mW
B-Wert B-value	$R_2 = R_{25}$ exp [$B_{25/50}(1/T_2 - 1/(298,15\ K))$]	$B_{25/50}$		3375		K
B-Wert B-value	$R_2 = R_{25}$ exp [$B_{25/80}(1/T_2 - 1/(298,15\ K))$]	$B_{25/80}$		t.b.d.		K
B-Wert B-value	$R_2 = R_{25}$ exp [$B_{25/100}(1/T_2 - 1/(298,15\ K))$]	$B_{25/100}$		t.b.d.		K

Angaben gemäß gültiger Application Note.
Specification according to the valid application note.

prepared by: DPK	date of publication: 2013-10-03
approved by: RK	revision: 2.0

Vorläufige Daten
Preliminary Data

Modul / Module

Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		2,5		kV
Innere Isolation Internal isolation	Basisisolierung (Schutzklasse 1, EN61140) basic insulation (class 1, IEC 61140)			Al_2O_3		
Kriechstrecke Creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			5,0 5,0		mm
Luftstrecke Clearance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			3,2 3,2		mm
Vergleichszahl der Kriechwegbildung Comperative tracking index		CTI		> 225		
			min.	typ.	max.	
Modulstreuinduktivität Stray inductance module		L_{sCE}		25		nH
Modulleitungswiderstand, Anschlüsse - Chip Module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		9,50		mΩ
Lagertemperatur Storage temperature		T_{stg}	-40		125	°C
Anpresskraft für mech. Bef. pro Feder mountig force per clamp		F	30	-	50	N
Gewicht Weight		G		10		g

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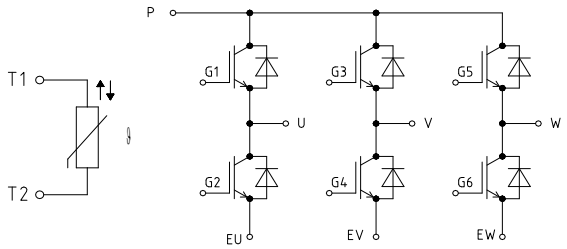
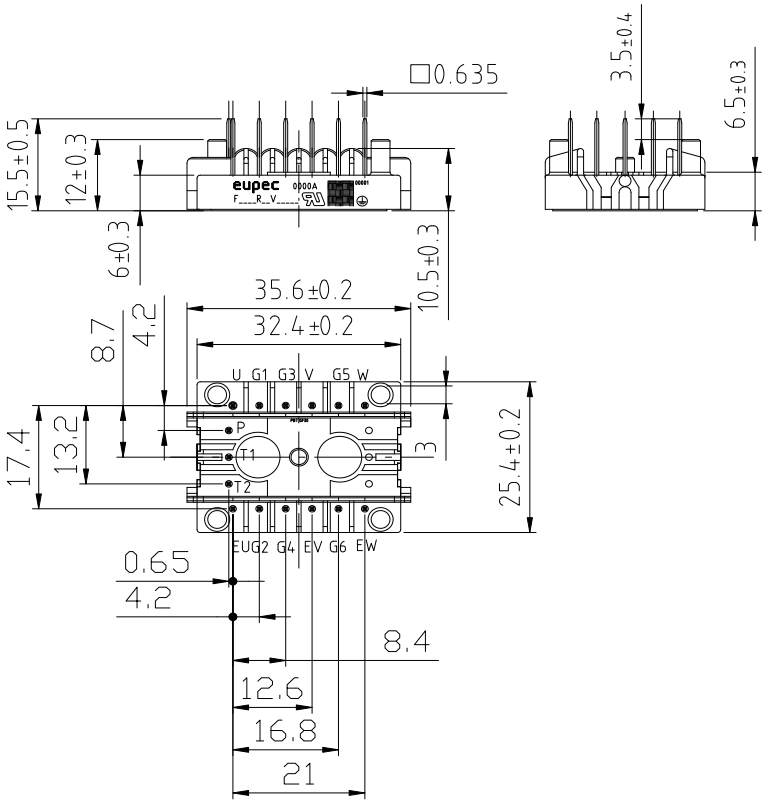
approved by: RK	revision: 2.0

Vorläufige Daten
Preliminary Data

Schaltplan / circuit_diagram_headline



Gehäuseabmessungen / package outlines



Pinpositions with tolerance ⌖ ø0.4

prepared by: DPK	date of publication: 2013-10-03
approved by: RK	revision: 2.0

A.5 Gate Driver

EiceDRIVER™
3 phase 200 V and 600 V gate drive IC

1 Overview

Main features

- Thin-film-SOI-technology
- Maximum blocking voltage +600V
- Separate control circuits for all six drivers
- CMOS and LSTTL compatible input (negative logic)
- Signal interlocking of every phase to prevent cross-conduction
- Detection of over current and under voltage supply
- externally programmable delay for fault clear after over current detection

Product highlights

- Insensitivity of the bridge output to negative transient voltages up to -50V given by SOI-technology
- Ultra fast bootstrap diodes
- 'shut down' of all switches during error conditions

Typical applications

- Home appliances
- Fans, pumps
- General purpose drives

Product family

Table 1 Members of 6ED family – 2nd generation

Sales Name	high side control input HIN1,2,3 and LIN1,2,3	typ. UVLO-Thresholds	Bootstrap diode	Package
6EDL04I06NT	negative logic	11.7 V / 9.8 V	Yes	DSO28
6EDL04I06PT	positive logic	11.7 V / 9.8 V	Yes	DSO28
6EDL04N06PT / 6EDL04N02PR	positive logic	9 V / 8.1 V	Yes	DSO28 / TSSOP28

Description

The device 6ED family – 2nd generation is a full bridge driver to control power devices like MOS-transistors or IGBTs in 3-phase systems with a maximum blocking voltage of +600 V. Based on the used SOI-technology there is an excellent ruggedness on transient voltages. No parasitic thyristor structures are present in the device. Hence, no parasitic latch-up may occur at all temperatures and voltage conditions.

The six independent drivers are controlled at the low-side using CMOS resp. LSTTL compatible signals, down to 3.3 V logic. The device includes an under-voltage detection unit with hysteresis characteristic and an over-current detection. The over-current level is adjusted by choosing the resistor value and the threshold level at pin ITRIP. Both error conditions (under-voltage and over-current) lead to a definite shut down off all six switches. An error signal is provided at the FAULT open drain output pin. The blocking time after over-current can be adjusted with an RC-network at pin RCIN. The input RCIN owns an internal current source of 2.8 µA. Therefore, the resistor R_{RCIN} is optional. The typical output current can be given with 165 mA for pull-up and 375 mA for pull down. Because of system safety reasons a 310 ns interlocking time has been realised. The function of input EN can optionally be extended with an over-temperature detection, using an external NTC-resistor (see Fig.1). The

monolithic integrated bootstrap diode structures between pins VCC and VBx can be used for power supply of the high side.

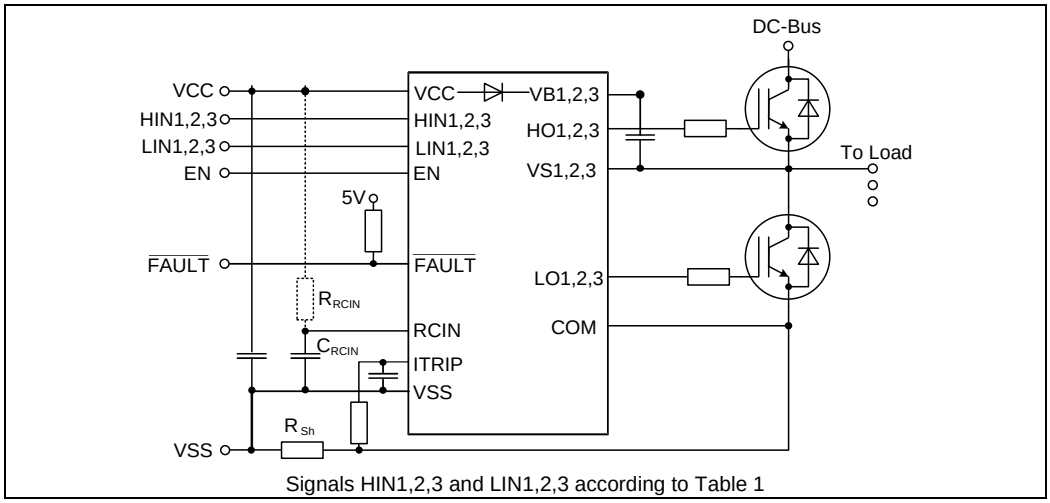


Figure 1 Typical Application

3 Pin configuration, description, and functionality

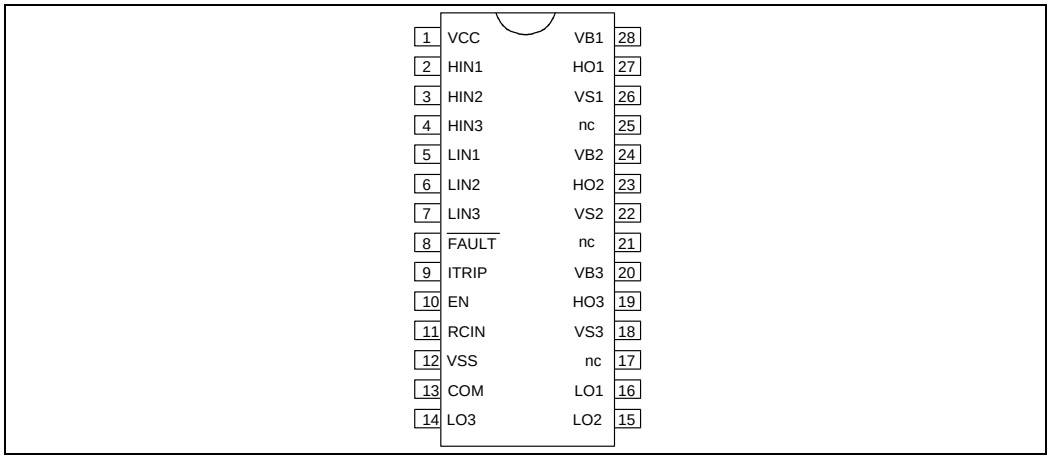


Figure 4 Pin Configuration of 6ED family (signals HIN1,2,3 and LIN1,2,3 according to Table 1)

Table 2 xPin Description

Symbol	Description
VCC	Low side power supply
VSS	Logic ground
HIN1,2,3	High side logic input (positive or negative logic according to Table 1)
LIN1,2,3	Low side logic input (positive or negative logic according to Table 1)
/FAULT	Indicates over-current and under-voltage (negative logic, open-drain output)
EN	Enable I/O functionality (positive logic)
ITRIP	Analog input for over-current shut down, activates FAULT and RCIN to VSS
RCIN	External RC-network to define FAULT clear delay after FAULT-Signal (T_{FLTCLR})
COM	Low side gate driver reference
VB1,2,3	High side positive power supply
HO1,2,3	High side gate driver output
VS1,2,3	High side negative power supply
LO1,2,3	Low side gate driver output
nc	Not connected

3.1 Low Side and High Side Control Pins (Pin 2, 3, 4, 5, 6, 7)

The Schmitt trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. Input Schmitt trigger and noise filter provide beneficial noise rejection to short input pulses according to Figure 5 and Figure 6.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 3 Abs. maximum ratings

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage(Note 1)	DSO28 TSSOP28	V_S	V_{CC}-V_{BS}-6	600 180	V
High side offset voltage (t_p<500ns, Note 1)			V_{CC} -V_{BS} – 50	–	
High side offset voltage(Note 1)	DSO28 TSSOP28	V_B	V_{CC} – 6	620 200	
High side offset voltage (t_p<500ns, Note 1)			V_{CC} – 50	–	
High side floating supply voltage (V_B vs. V_S) (internally clamped)		V_{BS}	-1	20	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	-0.5	V_B + 0.5	
Low side supply voltage (internally clamped)		V_{CC}	-1	20	
Low side supply voltage (V_{CC} vs. V_{COM})		V_{CCOM}	-0.5	25	
Gate driver ground		V_{COM}	-5.7	5.7	
Low side output voltage (V_{LO} vs. V_{COM})		V_{LO}	-0.5	V_{CCOM} + 0.5	
Input voltage LIN,HIN,EN,ITRIP		V_{IN}	-1	10	
FAULT output voltage		V_{FLT}	-0.5	V_{CC} + 0.5	
RCIN output voltage		V_{RCIN}	-0.5	V_{CC} + 0.5	
Power dissipation (to package) Note 2	DSO28 TSSOP28	P_D	– –	1.3 0.6	W
Thermal resistance (junction to ambient, see section 6)	DSO28 TSSOP28	$R_{th(j-a)}$	– –	75 165	K/W
Junction temperature		T_J	–	125	°C
Storage temperature		T_S	- 40	150	
offset voltage slew rate (Note 3)		dV_S/dt		50	V/ns

Note :The minimum value for ESD immunity is 1.0kV (Human Body Model). ESD immunity inside pins connected to the low side (VCC, HINx, LINx, FAULT, EN, RCIN, ITRIP, VSS, COM, LOx) and pins connected inside each high side itself (VBx, HOx, VSx) is guaranteed up to 1.5kV (Human Body Model).

Note 1 : In case $V_{CC} > V_B$ there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx. Insensitivity of bridge output to negative transient voltage up to –50V is not subject to production test – verified by design / characterization.

Note 2: Consistent power dissipation of all outputs. All parameters inside operating range.

Note 3: Not subject of production test, verified by characterisation

4.2 Required operation conditions

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 4 Required Operation Conditions

Parameter		Symbol	Min.	Max.	Unit
High side offset voltage (Note 1)	DSO28 TSSOP28	V_B	7	620 200	V
Low side supply voltage (V_{CC} vs. V_{COM})	DSO28 TSSOP28	V_{CCOM}	10	25	

4.3 Operating Range

All voltages are absolute voltages referenced to V_{SS} -potential unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 5 Operating range

Parameter		Symbol	Min.	Max.	Unit
High side floating supply offset voltage		V_S	V_{CC} - V_{BS} -1	500	V
High side floating supply offset voltage (V_B vs. V_{CC}, statically)		V_{BCC}	-1.0	500	
High side floating supply voltage (V_B vs. V_S, Note 1)	6EDL04I06NT 6EDL04I06PT	V_{BS}	13	17.5	
	6EDL04N06PT 6EDL04N02PR		10	17.5	
High side output voltage (V_{HO} vs. V_S)		V_{HO}	0	V_{BS}	
Low side output voltage (V_{LO} vs. V_{COM})		V_{LO}	0	V_{CC}	
Low side supply voltage	6EDL04I06NT 6EDL04I06PT	V_{CC}	13	17.5	
	6EDL04N06PT 6EDL04N02PR		10	17.5	
Low side ground voltage		V_{COM}	-2.5	2.5	
Logic input voltages LIN,HIN,EN,ITRIP (Note 2)		V_{IN}	0	5	
FAULT output voltage		V_{FLT}	0	V_{CC}	
RCIN input voltage		V_{RCIN}	0	V_{CC}	
Pulse width for ON or OFF (Note 3)		t_{IN}	1	–	µs
Ambient temperature		T_a	-40	105	°C

Note 1 : Logic operational for V_B (V_B vs. V_S) > 7,0V

Note 2 : All input pins (HINx, LINx) and EN, ITRIP pin are internally clamped (see abs. maximum ratings)

Note 3 : In case of input pulse width at LINx and HINx below 1µ the input pulse may not be transmitted properly

4.4 Static logic function table

VCC	VBS	RCIN	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
$<V_{CCUV-}$	X	X	X	X	0	0	0
15V	$<V_{BSUV-}$	X	0	3.3 V	High imp	LIN1,2,3*	0
15V	15V	<3.2 V ↓	0	3.3 V	0	0	0
15V	15V	X	$> V_{IT,TH+}$	3.3 V	0	0	0
15V	15V	$> V_{RCIN,TH}$	0	3.3 V	High imp	LIN1,2,3*	HIN1,2,3*
15V	15V	$> V_{RCIN,TH}$	0	0	High imp	0	0

* according to Table 1

4.5 Static parameters

V_{CC} = V_{BS} = 15V unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
High level input voltage		V_{IH}	1.7	2.1	2.4	V	
Low level input voltage		V_{IL}	0.7	0.9	1.1		
EN positive going threshold		$V_{EN,TH+}$	1.9	2.1	2.3		
EN negative going threshold		$V_{EN,TH-}$	1.1	1.3	1.5		
ITRIP positive going threshold		$V_{IT,TH+}$	380	445	510	mV	
ITRIP input hysteresis		$V_{IT,HYS}$	45	70			
RCIN positive going threshold		$V_{RCIN,TH}$	-	5.2	6.4	V	
RCIN input hysteresis		$V_{RCIN,HYS}$	-	2.0	-		
Input clamp voltage (HIN and LIN acc. Table 1, EN, ITRIP)		$V_{IN,CLMAP}$	9	10.3	12		I_{IN} = 4mA
Input clamp voltage at high impedance (/HIN, /LIN negative logic only)		$V_{IN,FLOAT}$	-	5.3	5.8		controller output pin floating
High level output voltage	LO1,2,3	V_{OH}	-	V_{CC} -0.7	V_{CC} -1.4		I_O = 20mA
	HO1,2,3		-	V_B -0.7	V_B -1.4		
Low level output voltage	LO1,2,3	V_{OL}	-	V_{COM}+ 0.2	V_{COM}+ 0.6		I_O = -20mA
	HO1,2,3		-	V_S+ 0.2	V_S + 0.6		
V_{CC} and V_{BS} supply undervoltage positive going threshold	6EDL04I06NT 6EDL04I06PT	V_{CCUV+} V_{BSUV+}	11	11.7	12.5		
	6EDL04N06PT 6EDL04N02PR		8.3	9	9.8		
V_{CC} and V_{BS} supply undervoltage negative going threshold	6EDL04I06NT 6EDL04I06PT	V_{CCUV-} V_{BSUV-}	9.5	9.8	10.8	V	
	6EDL04N06PT 6EDL04N02PR		7.5	8.1	8.8		

Table 6 Static parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
V_{CC} and V_{BS} supply undervoltage lockout hysteresis	6EDL04I06PT 6EDL04I06PT	V_{CCUVH} V_{BSUVH}	1.2	1.9	-	V	
	6EDL04N06PT 6EDL04N02PR		0.5	0.9	-		
High side leakage current betw. VS and VSS		I_{LVS+}		1	12.5	µA	V_S = 600V
High side leakage current betw. VS and VSS		I_{LVS+}[1]	-	10	-		T_J=125°C,V_S=600V
High side leakage current between VSx and VSy (x=1,2,3 and y=1,2,3)		I_{LVS-}[1]	-	10	-		T_J = 125°C V_{Sx} - V_{Sy} = 600V
Quiescent current V_{BS} supply (VB only)		I_{QBS1}	-	210	400		HO=low
Quiescent current V_{BS} supply (VB only)		I_{QBS2}	-	210	400		HO=high
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NT	I_{QCC1}	-	1.1	1.8	mA	V_{LIN}=float. (all) V_{VSx}=50V (only bootstrap types)
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR		-	0.75	1.5		
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NT	I_{QCC2}	-	1.3	2		V_{LIN}=0, V_{HIN}=3.3 V V_{VSx}=50V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0.75	1.5		V_{LIN}=3.3 V, V_{HIN}=0 V_{VSx}=50V
Quiescent current V_{CC} supply (VCC only)	6EDL04I06NT	I_{QCC3}	-	1.3	2		V_{LIN}=3.3 V, V_{HIN}=0 V_{VSx}=50V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0.75	1.5		V_{LIN}=3.3 V, V_{HIN}=0 V_{VSx}=50V
Input bias current	6EDL04I06NT	I_{LIN+}	-	70	100	µA	V_{LIN}=3.3 V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR		400	700	1100		
Input bias current	6EDL04I06NT	I_{LIN-}	-	110	200	µA	V_{LIN}=0
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0			
Input bias current	6EDL04I06NT	I_{HIN+}	-	70	100		V_{HIN}=3.3 V
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR		400	700	1100		
Input bias current	6EDL04I06NT	I_{HIN-}	-	110	200		V_{HIN}=0
	6EDL04I06PT 6EDL04N06PT 6EDL04N02PR			0			
Input bias current (ITRIP=high)		I_{ITRIP+}		45	120		V_{ITRIP}=3.3 V
Input bias current (EN=high)		I_{EN+}	-	45	120		V_{ENABLE}=3.3 V
Input bias current RCIN (internal current source)		I_{RCIN}		2.8			V_{RCIN} = 2 V

[1] Not subject of production test, verified by characterisation

Table 6 Static parameters

Parameter	Symbol	Values			Unit	Test condition
		Min.	Typ.	Max.		
Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%)	I_{O+}	120	165	-	mA	C_L=10 nF
Peak output current turn on (single pulse)	I_{Opk+} [1]		240			R_L = 0 Ω, t_p <10 µs
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	I_{O-}	250	375	-		C_L=10 nF
Peak output current turn off (single pulse)	I_{Opk-} [1]		420			R_L = 0 Ω, t_p <10 µs
Bootstrap diode forward voltage between VCC and VB	$V_{F,BSD}$	-	1.0	1.3	V	I_F=0.5 mA
Bootstrap diode forward current between VCC and VB	$I_{F,BSD}$	27	51	75	mA	V_F=4 V
Bootstrap diode resistance	R_{BSD}	24	40	60	Ω	V_{F1}=4 V, V_{F2}=5 V
RCIN low on resistance of the pull down transistor	$R_{on,RCIN}$	-	40	100		V_{RCIN}=0.5 V
FAULT low on resistance of the pull down transistor	$R_{on,FLT}$	-	45	100		V_{FAULT}=0.5 V

[1] Not subject of production test, verified by characterisation

4.6 Dynamic parameters

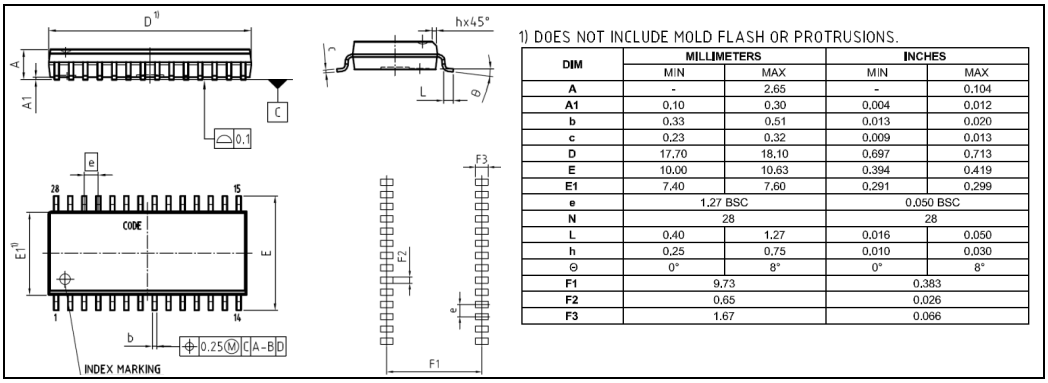
V_{CC} = V_{BS} = 15 V, V_S = V_{SS} = V_{COM} unless otherwise specified. All parameters are valid for T_a=25 °C.

Table 7 Dynamic parameters

Parameter		Symbol	Values			Unit	Test condition
			Min.	Typ.	Max.		
Turn-on propagation delay		t_{on}	400	530	800	ns	$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-off propagation delay	6EDL04I06NT 6EDL04I06PT	t_{off}	360	490	760		
	6EDL04N06PT 6EDL04N02PR		400	530	800		
Turn-on rise time		t_r	-	60	100		$V_{LIN/HIN}$ = 0 or 3.3 V
Turn-off fall time		t_f	-	26	45		C_L = 1 nF
Shutdown propagation delay ENABLE		t_{EN}	-	780	1100		V_{EN}=0
Shutdown propagation delay ITRIP		t_{ITRIP}	400	670	1000		V_{ITRIP}=1 V
Input filter time ITRIP		$t_{ITRIPMIN}$	155	230	380		
Propagation delay ITRIP to FAULT		t_{FLT}	-	420	700		
Input filter time at LIN/HIN for turn on and off		t_{FILIN}	120	300	-		$V_{LIN/HIN}$ = 0 & 3.3 V
Input filter time EN		t_{FILEN}	300	600	-		
Fault clear time at RCIN after ITRIP-fault, (C_{RCin}=1nF)		t_{FLTCLR}	1.0	1.9	3.0	ms	$V_{LIN/HIN}$ = 0 & 3.3 V V_{ITRIP} = 0
Dead time		DT	150	310	-	ns	$V_{LIN/HIN}$ = 0 & 3.3 V
Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs		MT_{ON}	-	20	100		external dead time > 500 ns
Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs		MT_{OFF}	-	40	100		external dead time >500 ns
Output pulse width matching. Pw_{in}-PW_{out}	6EDL04I06NT 6EDL04I06PT	PM		40	100		PW_{in} > 1 µs
	6EDL04N06PT 6EDL04N02PR			10	100		

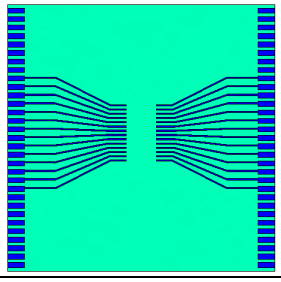
6 Package

6.1 PG-DSO-28



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	2.65	-	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	17.70	18.10	0.697	0.713
E	10.00	10.63	0.394	0.419
E1	7.40	7.60	0.291	0.299
e	1.27 BSC		0.050 BSC	
N	28		28	
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.030
Θ	0°	8°	0°	8°
F1	9.73		0.383	
F2	0.65		0.026	
F3	1.67		0.066	

Figure 19 Package drawing



Dimensions	80.0 × 80.0 × 1.5 mm³	λ_{therm} [W/m·K]
Material	FR4	0.3
Metal (Copper)	70µm	388

Figure 20 PCB reference layout

A.6 Gate Driver: Technical Description

This pin is on high potential again after transistor T2 is turned off and either T1 or D1 is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin VB and VCC. It is good engineering to choose the same blocking voltage of power transistor T1 and external bootstrap diode. The voltage of the bootstrap capacitor can now supply the highside gate drive sections.

It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual highside driver section.
The voltage of bootstrap capacitor is approximately

$$V_{CBS} \approx V_{CC} - V_{FBS} \tag{1}$$

A current limiting resistor R_{Lim} reduces the peak of the pulse current during the turn-on of transistor T2. The pulse current will occur at each turn-on of transistor T2, so that with increasing switching frequency the capacitor C_{BS} is charged more frequently. Therefore a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: The highside quiescent current and the gate charge of the transistor to be turned on. The calculation of the bootstrap capacitor results in

$$C_{BS} = \frac{i_{QBS} \cdot t_P + Q_G}{\Delta v_{BS}} \cdot 1.2 \tag{2}$$

with i_{QBS} being the quiescent current of the highside section, t_P the switching period, Q_G the total gate charge and Δv_{BS} the voltage drop at the bootstrap capacitor within a switching period. An additional margin of 20% is added for the case of tolerances for the bootstrap capacitor.

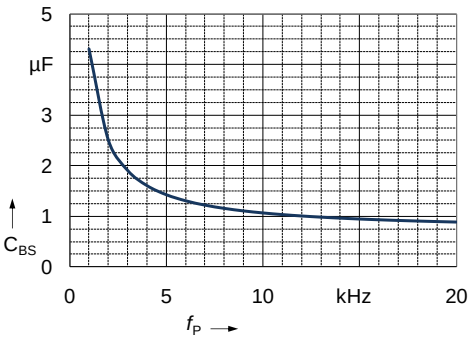


Figure 11 Size of the bootstrap capacitor as a function of the switching frequency f_P for driving IKD10N60R according to equ. (2) with a voltage ripple of 0.1 V

Figure 11 shows the curve corresponding to equ. (2) for a continuous sinusoidal modulation, if the voltage ripple Δv_{BS} = 0.1 V. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances. It is therefore not recommended to exceed a maximum capacitance of C_{BS} = 47 µF.
Please note here, that equ. (2) is valid for continuous switching operation according to the switching frequency. The use of space vector modulations can cause periods up to 60° (electrical), in which no switching of the low side transistor of a halfbridge occurs and must be considered seperately. This effects the bootstrap capacitor size, especially for low output current (motor current) frequencies. In this case the variable t_P must be set to the longest period of no switching.

3.7 Protection

3.7.1 Overcurrent protection (ITRIP)

The current signal of the DC-link reference is measured in order to recognize overcurrent or halfbridge short circuit events. A shunt resistor generates a voltage drop. A small RC-filter for attenuating voltage spikes is recommended. Such spikes may be generated by parasitic elements in the practical layout. It is highly recommended as considerations of good layout to avoid any joint PCB track of the ITRIP signal with the low side emitter track or the COM track (see also section 3.10). If the voltage drop over the shunt is higher than typically $V_{IT,TH+}$ = 0.445 V, then the internal comparator is triggered according to Figure 12. This results in a trigger current of

$$I_{ITRIP} = \frac{V_{IT,TH+}}{R_{SH}} \quad (3)$$

where R_{SH} is the value of the shunt resistor.

The output of the comparator passes a noise filter, which inhibits an overcurrent shutdown caused by parasitic voltage spikes. The typical filter time of the noise filter is $t_{ITRIPMIN}$ = 210 ns. A set-dominant latch stores the overcurrent event until it is reset by the signal provided from the RCIN circuit.

The ITRIP-comparator switches the discharging NMOS-FET at pin RCIN. The $R_{DS(on)}$ of the FET is typically 54 Ω, so that there is a characteristical discharge curve in respect of the external capacitor C_{RCin}. The time constant is defined by the external capacitor C_{RCin} and the $R_{DS(on)}$ of the FET. The dischage phase ends, when the comparator is low again. This corresponds to a voltage level at the comparator of $V_{IT,TH+}$ - $V_{IT,HYS}$ = 445 mV - 70 mV = 375 mV, where $V_{IT,HYS}$ = 70 mV is the hysteresis of the ITRIP-comparator.

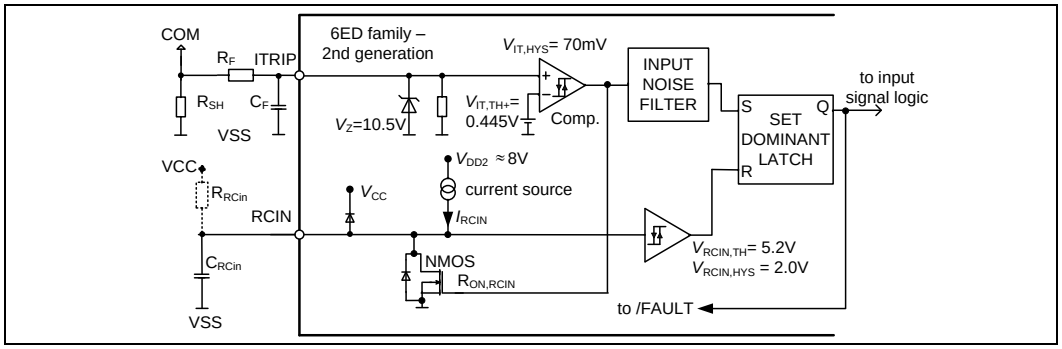


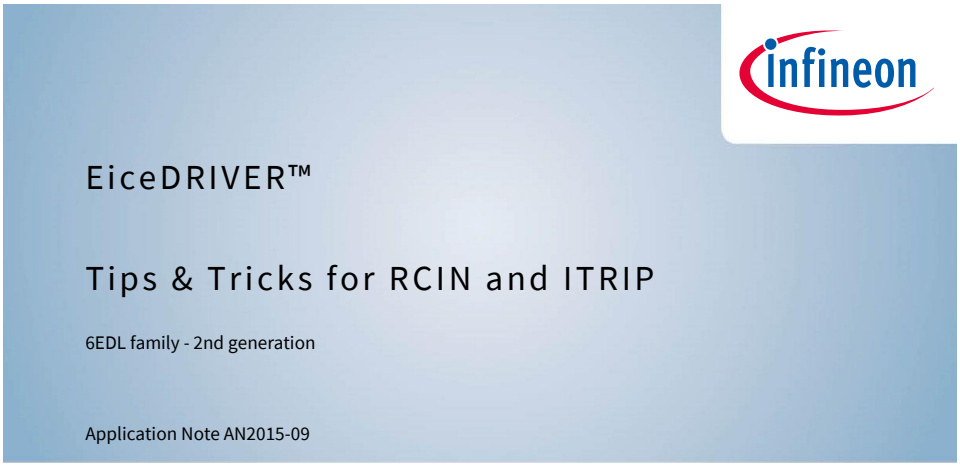
Figure 12 Internal structure of the ITRIP and RCIN sections

It is important to note here, that due to a large external capacitance at pin RCIN and rather short occurrance of overcurrent, the voltage at the capacitor C_{RCin} is not below the thereshold of the RCIN Schmitt-Trigger. The threshold of the Schmitt-Trigger $V_{RCIN,TH}$ - $V_{RCIN,HYS}$ = 5.2 V – 2 V = 3.2 V lead to the result, that the set-dominant latch is still in active reset and the IC might restart operation as soon as the voltage at pin ITRIP is in the operative range again, which is $V_{IT,TH+}$ - $V_{IT,HYS}$. If the trigger level at pin ITRIP is set closely to the maximum operative current, then this behaviour acts as a soft overcurrent limitation. As long as the voltage at pin RCIN does not hit the 3.2 V level of the Schmitt-trigger, the gate drive section restarts immediately after the overcurrent vanishes. This may be after some pulse periods.

3.7.2 Failure reset (RCin)

The external circuit at pin RCIN defines the overcurrent recovery of the drive system. This circuit can consist of a single capacitor C_{RCin} according to Figure 12. There is also the option for a path to the supply voltage V_{CC} via resistor R_{RCin}. The fault-clear time t_{FLTCLR} is dependent on the re-charging of C_{RCin}, because the system

A.7 Gate Driver: Tips and Tricks for RCIN and ITRIP



EiceDRIVER™

Tips & Tricks for RCIN and ITRIP

6EDL family - 2nd generation

Application Note AN2015-09

About this document

Scope and purpose

The RCIN and ITRIP functions strongly help to reduce the system cost. However, the functions as they are available do have limitations in some applications. This application note helps to understand the function more in detail and give application support how to overcome these limitations.

Intended audience

The application note addresses experienced hardware engineers who have already basic knowledge of the 6EDL family – 2nd generation.

Table of Contents

3 Overcome the high trigger level of the ITRIP function

This section describes how the high trigger level of the overcurrent shut down function can be adapted towards lower levels.

3.1 Application problem

The shunt, which is located in the emitter path of a low side IGBT, generates a voltage according to its bias point. This voltage is filtered by means of a R_F / C_F –combination according to Figure 5.

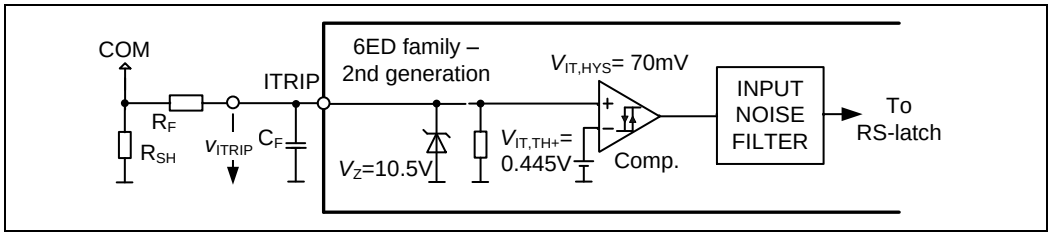


Figure 5 ITRIP function

The ITRIP trigger level of $V_{IT,th+}$ = 0.445 V is fixed for the 6EDL family – 2nd generation. The adjustment of the triggering current level is done by adjusting the shunt value, so that the shunt's voltage will trigger the ITRIP event. However, applications with high load currents will dissipate a considerable power in the shunt. For example, a current trigger level of 50 A would dissipate a power of 50 A · 0.445 V = 22.25 W. Therefore, the current trigger level should result in a low shunt voltage in the area of 100 mV to 200 mV in order to reduce the power dissipated in the shunt.

3.2 Application solution

The application solution is implemented by an additional voltage drop over the filter resistor R_F. The voltage drop is generated by a current added by a pull up-resistor R_{pu} according to Figure 6.

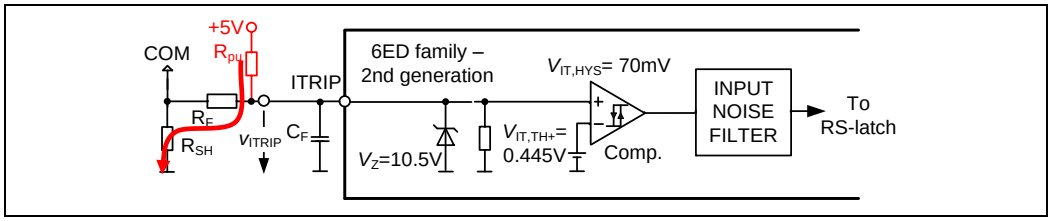


Figure 6 ITRIP function with pre-bias circuit

The required voltage drop of the resistor R_F is calculated with

$$V_{\mathrm{IT,th}} = V_{\mathrm{RF}} + V_{\mathrm{SH,max}} \implies V_{\mathrm{RF}} = V_{\mathrm{IT,th}} - V_{\mathrm{SH,max}} \tag{10}$$

This results in a required pull-up current of

$$I_{\mathrm{RF}} = \frac{V_{\mathrm{RF}}}{R_{\mathrm{F}}} \tag{11}$$

Now the pull-up resistor value which provides the current I_{RF} can be calculated

$$R_{pu} = \frac{V_{pu} - V_{IT,th}}{I_{RF}} \quad (12)$$

3.3 Application example

The example in this document is based on these conditions and assumptions:

- The triggering current of an ITRIP event should result in a shunt voltage of 200 mV
- The pull-up voltage is 5 V
- R_F = 1 kΩ ($\gg R_{SH}$)

The execution of equations (10) - (12) is

$$V_{RF} = V_{IT,th} - V_{SH,max} = 0.445\ V - 0.2\ V = 0.245\ V \quad (13)$$

The pull-up current will be

$$I_{RF} = \frac{V_{RF}}{R_F} = \frac{0.245\ V}{1\ k\Omega} = 0.245\ mA \quad (14)$$

Now the pull-up resistor value which provides the current I_{RF} can be calculated

$$R_{pu} = \frac{V_{pu} - V_{IT,th}}{I_{RF}} = \frac{5\ V - 0.445\ V}{0.245\ mA} \approx 18.6\ k\Omega \quad (15)$$

A selection of R_{pu} = 18 kΩ is possible. The design verification step executes the reworked equations (12) - (10) using the selected component values.

$$I_{RF} = \frac{V_{pu} - V_{IT,th}}{R_{pu}} = \frac{5\ V - 0.445\ V}{18\ k\Omega} = 0.253\ mA \quad (16)$$

This results in a voltage drop at the resistor R_F of

$$V_{RF} = I_{RF} \cdot R_F = 0.253\ mA \cdot 1\ k\Omega = 0.253\ V \quad (17)$$

The typical error is smaller than 5% and therefore acceptable with respect to the overall tolerance of the ITRIP function.

3.4 Limitations of the proposed solution

The most dominant limitation is the overall tolerance of the ITRIP function. It is of course possible to reduce the triggering shunt voltage of this function. However, the absolute tolerance of ± 65 mV remains. A very precise overcurrent shut down function can´t be achieved with this proposal. Nevertheless, the secure shut down of short circuit events is not jeopardized.

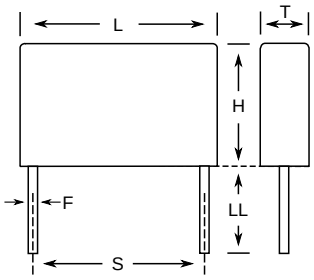
Additionally, the ITRIP hysteresis must be considered, so that the largest usable voltage drop over the resistor R_F is $V_{IT,th+,min} - V_{IT,hys,typ}$ = 380 mV – 70mV = 310 mV. Therefore, the resulting smallest shunt voltage is 65 mV + 70 mV = 135 mV. An additional margin of approximately 50 mV is recommended in order to ensure a proper power up.

A.8 Snubber

KEMET Part Number: P410EE104M300AH101

Electronic Components
KEMET
CHARGED.

Capacitor, film, Metallized Paper, 0.1 uF, +/-20% Tol, -40/+85C, Integrated Resistor (X1), 1000 VDC@85C, Lead Spacing=25.4 mm



General Information	
Supplier:	KEMET
Dielectric:	Metallized Paper
Application:	Integrated Resistor (X1)
Style:	Radial Molded
Lead Form:	Wire Leads
Features:	Pulse
RoHS:	Yes

Specifications	
Capacitance:	0.1 uF
Voltage:	1000 VDC
Tolerance:	+/-20%
Voltage AC:	300 VAC
Rated Temperature:	85C
Temperature Range:	-40/+85C
Insulation Resistance:	3 GOhm
Miscellaneous:	Resistor Tolerance: +/-30%
Miscellaneous:	Resistor= 100 Ohms

Dimensions (mm)		
Symbol	**Dimension**	**Tolerance**
L	30.5	MAX
H	16.1	MAX
T	10.6	MAX
S	25.4	+/-0.4
LL	30	+5
F	1	+/-0.05

Packaging Specifications	
Package Kind:	Bulk
Package Quantity:	150

A.9 Current Sensor

Current Transducer LTS 6-NP

I_{PN} = 6 At

For the electronic measurement of currents: DC, AC, pulsed, mixed with galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

16065

Electrical data

I_{PN}	Primary nominal current rms		6	At
I_{PM}	Primary current, measuring range		0 .. ± 19.2	At
$\hat{I}_P$	Overload capability		250	At
V_{OUT}	Output voltage (Analog) @ I_P		2.5 ± (0.625·I_P/I_{PN})V	
	I_P = 0		2.5 [1]	V
G	Sensitivity		104.16	mV/A
N_S	Number of secondary turns (± 0.1 %)		2000	
R_L	Load resistance		≥ 2	kΩ
R_{IM}	Internal measuring resistance (± 0.5 %)		208.33	Ω
TCR_{IM}	Temperature coefficient of R_{IM}		< 50	ppm/K
V_C	Supply voltage (± 5 %)		5	V
I_C	Current consumption @ V_C = 5 V	Typ	28+I_S [2]+(V_{OUT}/R_L)	mA

Accuracy - Dynamic performance data

X	Accuracy @ I_{PN}, T_A = 25°C			± 0.2	%
	Accuracy with R_{IM} @ I_{PN}, T_A = 25°C			± 0.7	%
ε_L	Linearity error			< 0.1	%
			Typ	Max	
TCV_{OUT}	Temperature coefficient of V_{OUT} @ I_P= 0	- 10°C .. + 85°C	80	200	ppm/K
		- 40°C .. - 10°C		250	ppm/K
TCG	Temperature coefficient of G	- 40°C .. + 85°C		50 [3]	ppm/K
V_{OM}	Magnetic offset voltage @ I_P = 0,				
	after an overload of 3 x I_{PN}			± 0.5	mV
	5 x I_{PN}			± 2.0	mV
	10 x I_{PN}			± 2.0	mV
t_{ra}	Reaction time @ 10 % of I_{PN}			< 100	ns
t_r	Response time to 90 % of I_{PN} step			< 400	ns
di/dt	di/dt accurately followed			> 15	A/µs
BW	Frequency bandwidth (0 .. - 0.5 dB)			DC .. 100	kHz
	(- 0.5.. 1 dB)			DC .. 200	kHz

General data

T_A	Ambient operating temperature	- 40 .. + 85 °C
T_S	Ambient storage temperature	- 40.. + 100 °C
m	Mass	10 g
	Standards	EN 50178: 1997
		IEC 60950-1: 2001

Notes: [1] Absolute value @ T_A = 25°C, 2.475 < V_{OUT} < 2.525

[2] I_S = I_P/N_S

[3] Only due to TCR_{IM}.

Features

- Closed loop (compensated) multi-range current transducer using the Hall effect
- Unipolar voltage supply
- Isolated plastic case recognized according to UL 94-V0
- Compact design for PCB mounting
- Incorporated measuring resistance
- Extended measuring range.

Advantages

- Excellent accuracy
- Very good linearity
- Very low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

Current Transducer LTS 6-NP

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16065

Electrical data

I_{PN}	Primary nominal current rms		6	At
I_{PM}	Primary current, measuring range		0 .. ± 19.2	At
$\hat{I}_P$	Overload capability		250	At
V_{OUT}	Output voltage (Analog) @ I_P		2.5 ± (0.625·I_P/I_{PN})V	
	I_P = 0		2.5 [1]	V
G	Sensitivity		104.16	mV/A
N_S	Number of secondary turns (± 0.1 %)		2000	
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	Accuracy with R_{IM} @ I_{PN}, T_A = 25°C			± 0.7	%
ε_L	Linearity error			< 0.1	%
			Typ	Max	
TCV_{OUT}	Temperature coefficient of V_{OUT} @ I_P= 0	- 10°C .. + 85°C	80	200	ppm/K
		- 40°C .. - 10°C		250	ppm/K
TCG	Temperature coefficient of G	- 40°C .. + 85°C		50 [3]	ppm/K
V_{OM}	Magnetic offset voltage @ I_P = 0,				
	after an overload of 3 x I_{PN}			± 0.5	mV
	5 x I_{PN}			± 2.0	mV
	10 x I_{PN}			± 2.0	mV
t_{ra}	Reaction time @ 10 % of I_{PN}			< 100	ns
t_r	Response time to 90 % of I_{PN} step			< 400	ns
di/dt	di/dt accurately followed			> 15	A/µs
BW	Frequency bandwidth (0 .. - 0.5 dB)			DC .. 100	kHz
	(- 0.5.. 1 dB)			DC .. 200	kHz

General data

T_A	Ambient operating temperature	- 40 .. + 85	°C
T_S	Ambient storage temperature	- 40.. + 100	°C
m	Mass	10	g
	Standards	EN 50178: 1997	
		IEC 60950-1: 2001	

Notes: [1] Absolute value @ T_A = 25°C, 2.475 < V_{OUT} < 2.525

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- Compact design for PCB mounting
- Incorporated measuring resistance
- Extended measuring range.

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- Excellent accuracy
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- Very low temperature drift
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- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

Current Transducer LTS 6-NP

Isolation characteristics

V_d	Rms voltage for AC isolation test, 50 Hz, 1 min	3	kV
$\hat{V}_w$	Impulse withstand voltage 1.2/50 µs	> 8	kV
		Min	
V_e	Rms voltage for partial discharge extinction @ 10pC	> 1.5	kV
dCp	Creepage distance [1]	15.5	mm
dCl	Clearance distance [2]	6.35	mm
CTI	Comparative Tracking Index (group IIIa)	175	

Notes: [1] On housing
[2] On PCB with soldering pattern UTEC93-703.

Applications examples

According to EN 50178 and IEC 61010-1 standards and following conditions:

- Over voltage category OV 3
- Pollution degree PD2
- Non-uniform field

	EN 50178	IEC 61010-1
dCp, **dCl**, $\hat{V}_w$	Rated insulation voltage	Nominal voltage
Single insulation	600 V	600 V
Reinforced insulation	300 V	300 V

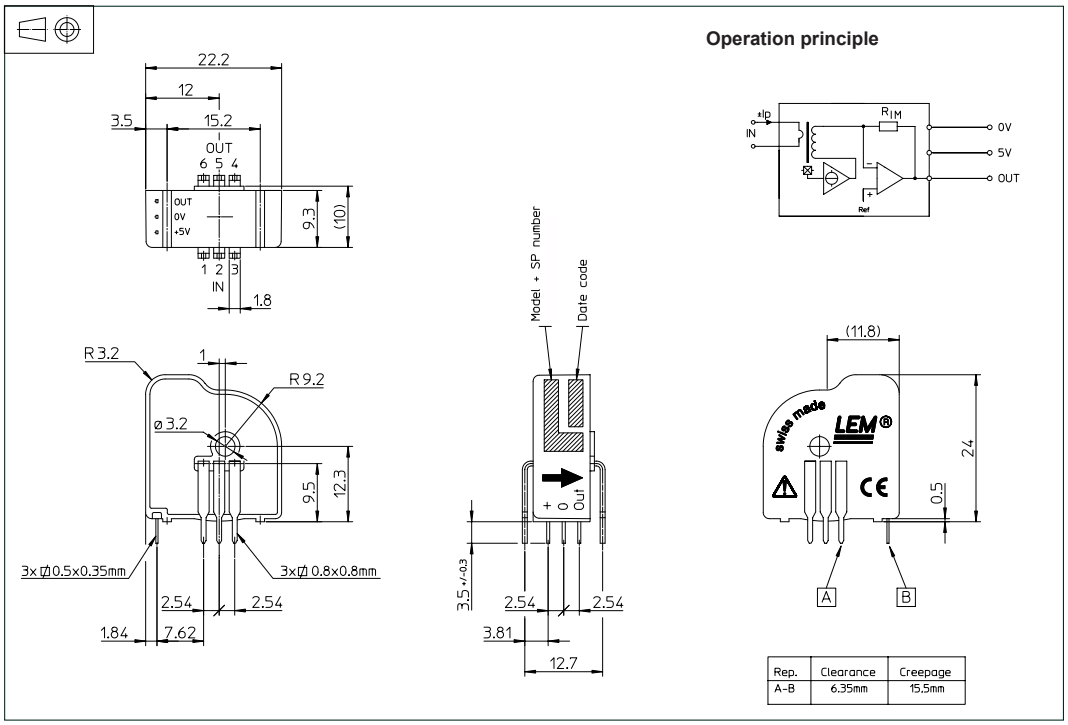
Safety

This transducer must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.

Caution, risk of electrical shock

When operating the transducer, certain parts of the module can carry hazardous voltage (eg. primary busbar, power supply).
Ignoring this warning can lead to injury and/or cause serious damage.
This transducer is a build-in device, whose conducting parts must be inaccessible after installation.
A protective housing or additional shield could be used.
Main supply must be able to be disconnected.

Dimensions LTS 6-NP (in mm.)



Number of primary turns	Primary nominal current rms I_{PN} [A]	Nominal output voltage V_{OUT} [V]	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended connections
1	± 6	2.5 ± 0.625	0.18	0.013	OUT 6 5 4 / IN 1 2 3
2	± 3	2.5 ± 0.625	0.81	0.05	OUT 6 5 4 / IN 1 2 3
3	± 2	2.5 ± 0.625	1.62	0.12	OUT 6 5 4 / IN 1 2 3

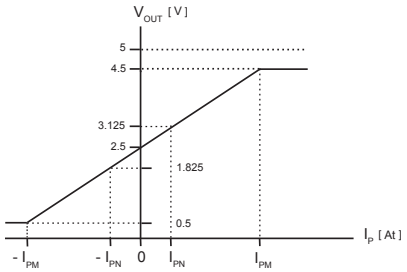
Mechanical characteristics

- General tolerance ± 0.2 mm
- Fastening & connection of primary 6 pins 0.8 x 0.8 mm
  Recommended PCB hole 1.3 mm
- Fastening & connection of secondary 3 pins 0.5 x 0.35 mm
  Recommended PCB hole 0.8 mm
- Additional primary through-hole Ø 3.2 mm

Remarks

- V_{OUT} swings above 2.5 V when I_P flows from terminals 1, 2, 3 to terminals 6, 5, 4 (with the arrow).
- Temperature of the primary jumper should not exceed 100°C.

Output Voltage - Primary Current



A.10 NTC Thermistor

NTC thermistors for inrush current limiting

Leaded and coated disks

Series/Type: **B57364S0***M0****

Date: May 2013

Applications

- Switch-mode power supplies
- Soft-start motors, e.g. in vacuum cleaners

Features

- Useable in series connections up to 265 V_{RMS}
- Coated thermistor disk
- Kinked leads of tinned copper wire
- Wide resistance range
- Manufacturer's logo, NTC and resistance value stamped on
- UL approval (E69802)

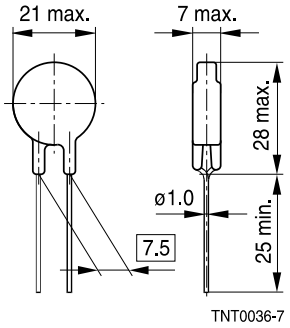
Options

Resistance tolerance <20% and alternative lead configurations available on request

Delivery mode

Bulk (standard) or with cardboard tape on 500-mm reel

Dimensional drawing



Dimensions in mm
Approx. weight 4 g

General technical data

Climatic category	(IEC 60068-1)		55/170/21	
Max. power	(at 25 °C)	P_{max}	5.1	W
Resistance tolerance		$\Delta R_R/R_R$	±20	%
Rated temperature		T_R	25	°C
Dissipation factor	(in air)	δ_{th}	approx. 24	mW/K
Thermal cooling time constant	(in air)	τ_c	approx. 100	s
Heat capacity		C_{th}	approx. 2400	mJ/K

Electrical specification and ordering codes

R_{25} Ω	I_{max} (0...65 °C) A	C_{test}[1] 230 V AC µF	C_{test}[1] 110 V AC µF	R_{min} (@ I_{max}, 25 °C) Ω	Ordering code
1	16.0	1000	4000	0.021	B57364S0109M0**
2	12.0	1000	4000	0.036	B57364S0209M0**
2.5	11.0	1000	4000	0.044	B57364S0259M0**
4	9.5	1000	4000	0.059	B57364S0409M0**
5	8.5	1000	4000	0.073	B57364S0509M0**
10	7.5	1000	4000	0.098	B57364S0100M0**

** = Delivery mode
00 = Bulk
51 = Reel packing

1) For details on the capacitance C_{test} please refer to "Application notes", chapter 1.6.

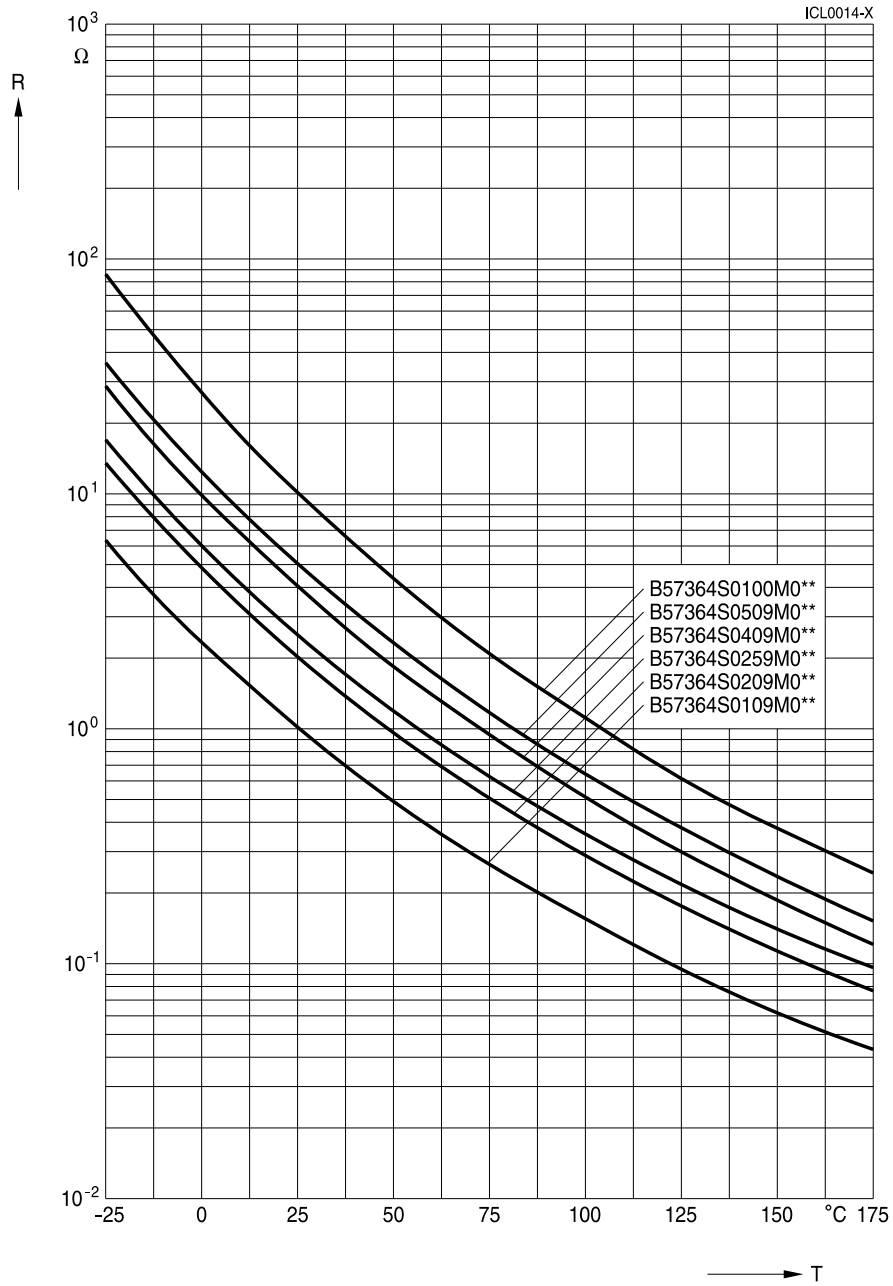
Reliability data

Test	Standard	Test conditions	$\Delta R_{25}/R_{25}$ (typical)	Remarks
Storage in dry heat	IEC 60068-2-2	Storage at upper category temperature T: 170 °C t: 1000 h	< 10%	No visible damage
Storage in damp heat, steady state	IEC 60068-2-78	Temperature of air: 40 °C Relative humidity of air: 93% Duration: 21 days	< 5%	No visible damage
Termal schock	IEC 60068-2-14	Lower test temperature: −55 °C t: 30 min Upper test temperature: 170 °C t: 30 min Time to change from lower to upper temperature: < 30 s Number of cycles: 10	< 10%	No visible damage
Endurance	IEC 60539-1	Ambient temperature: 25 ±5 °C $I = I_{max}$ t: 1000 h	< 10%	No visible damage
Cyclic endurance	IEC 60539-1	Ambient temperature: 25 ±5 °C $I = I_{max}$ On-time = 1 min Cooling time = 5 min Number of cycles: 1000	< 10%	No visible damage
Maximum permissible capacitance test	IEC 60539-1	Ambient temperature: 25 ±5 °C Capacitance = C_{test} Number of cycles: 1000	< 5%	No visible damage

Note

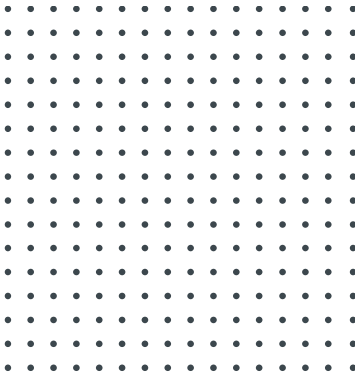
- The self-heating of a thermistor during operation depends on the load applied and the applicable dissipation factor.
- When loaded with maximum allowable current/power and the specified dissipation factor is taken as a basis, the NTC thermistor may reach a mean temperature of up to 250 °C.
- The heat developed during operation will also be dissipated through the lead wires. So the contact areas, too, may become quite hot at maximum load.
- When mounting NTC thermistors you have to ensure that there is an adequate distance between the thermistor and all parts which are sensitive to heat or combustible.

Resistance versus temperature



S364 series

A.11 DSP Board



DSP Development Board

User's Manual

POWERSIM INC.

Chapter 2 – Analog Input Interface

2.1 Analog Connector J8

The analog input connector J8 provides the interface to all analog inputs: power supply to the sensors (VA50), 3-phase voltages (Vain, Vbin, Vcin), dc voltage (Vdcin), 3-phase currents (Iain, Ibin, Icin), dc current (Idcin), 8 general-purpose ADC inputs (AD_A2in, AD_A4in, AD_A6in, AD_A7in, AD_B2in, AD_B4in, AD_B6in, AD_B7in).

Figure 2 and Table 2 show the pin assignment of the connector J8.

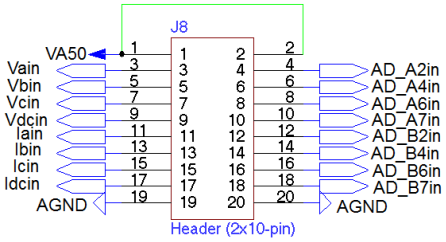


Figure 2: Analog Connector J8

Pin Number	Pin Name	Type	Description
1	VA50	Supply	+5.0V analog power supply
2	VA50	Supply	+5.0V analog power supply
3	Vain	Analog Input	AC voltage Phase A
4	AD_A2in	Analog Input	General-purpose ADC input
5	Vbin	Analog Input	AC voltage Phase B
6	AD_A4in	Analog Input	General-purpose ADC input
7	Vcin	Analog Input	AC voltage Phase C
8	AD_A6in	Analog Input	General-purpose ADC input
9	Vdcin	Analog Input	DC voltage
10	AD_A7in	Analog Input	General-purpose ADC input
11	Iain	Analog Input	AC current Phase A
12	AD_B2in	Analog Input	General-purpose ADC input
13	Ibin	Analog Input	AC current Phase B
14	AD_B4in	Analog Input	General-purpose ADC input
15	Icin	Analog Input	AC current Phase C
16	AD_B6in	Analog Input	General-purpose ADC input
17	Idcin	Analog Input	DC current
18	AD_B7in	Analog Input	General-purpose ADC input
19	AGND	Supply	Analog ground
20	AGND	Supply	Analog ground

Table 2: Analog Input Connector Pin Assignment

Chapter 3 – Motor Control Interface

3.1 Encoder Interface Connector J8

Connector J8 is used to interface with an encoder for motor position/speed sensing.

Phase A of the encoder should be connected to pin 1 ; Phase B should be connected to pin 2; and Phase Z (index or zero marker) should be connected to pin 3 as shown in figure 8.

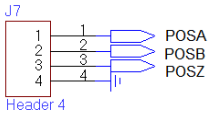


Figure 8: Encoder Interface Connector J8 Pin Assignment

3.2 Encoder Interface Circuit

The encoder interface circuit is shown in Figure 9.

The circuit uses a 1st-order low-pass filter with R=33Ω and C=100pf. Please note that input signals POSA, POSB, POSZ should be scaled to 0-3.3V because these signals are fed into DSP I/O directly.

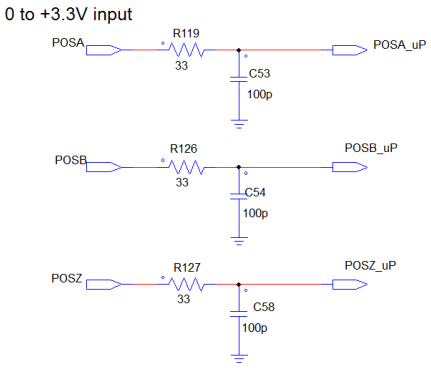


Figure 9: Encoder Interface Circuit

Chapter 4 – PWM/Digital Signals and Fault Signals

4.1 PWM Signal Connector J12

Figure 12 and Table 3 show the pin assignment of the PWM signal connector J12.

As shown in the figure, pins 1 to 8 provide the power supply.

Pins 1, 2 and 3 are connected to the external 12V dc power supply KL_30.

Pins 4, 5 and 8 provide the digital ground and pin 7 supplies the analog ground.

Pins 14 (phase W, top switch), 16 (phase W, bottom switch), 18 (phase V, top switch), 20 (phase V, bottom switch), 22 (phase U, top switch) and 24 (phase U, bottom switch) are PWM logic signals for 6 IGBT/MOSFET gate drivers. These PWM signals are generated by TI controlCARD.

Pins 12 is a reset signal to control the gate drivers 1ED020I12-F2.

Pins 13, 17, 21 and 23 are fault detection signals - one for each phase and one as logical “AND” combination of 3 phase fault detection signals.

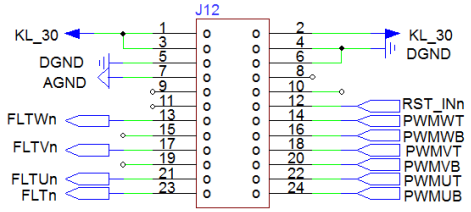


Figure 12: PWM Signal Connector J12 Pin Assignments

WARNING : When making connection or measurement to the connector J12, please handle with extreme care. DO NOT short circuit the power supply pins (Pins 1, 2, and 3) with any other pins. Short-circuit will damage the board!

Pin Number	Pin Name	Type	Description
1	KL_30	Supply	+12.0V Power Supply
2	KL_30	Supply	+12.0V Power Supply
3	KL_30	Supply	+12.0V Power Supply
4	DGND	Supply	Digital Ground
5	DGND	Supply	Digital Ground
6	DGND	Supply	Digital Ground
7	AGND	Supply	Analog Ground
8	NC		
9	NC		
10	NC		
11	NC		

12	RST_INn	Digital I/O	IGBT Gate Driver Reset
13	FLTWn	Digital I/O	IGBT Fault Phase C
14	PWM_WT	PWM I/O	PWM Gate High Phase C
15	NC		
16	PWM_WB	PWM I/O	PWM Gate Low Phase C
17	FLTVn	Digital I/O	IGBT Fault Phase B
18	PWM_VT	PWM I/O	PWM Gate High Phase B
19	NC		
20	PWM_VB	PWM I/O	PWM Gate Low Phase B
21	FLTUn	Digital I/O	IGBT Fault Phase A
22	PWM_UT	PWM I/O	PWM Gate High Phase A
23	FLTn	Digital I/O	IGBT Fault
24	PWM_UB	PWM I/O	PWM Gate Low Phase A

Table 3: PWM signal connector J12 pin assignment

4.2 Gate Drive Interface Signals

Figure 13 shows the interface circuit between DSP (0 to 3.3V) and IGBT/MOSFET gate drivers (0 to 5V). This is a level shift circuit with a 16-bit dual supply translating transceiver IC 74ALVC164245. The 0-3.3V PWM control signals G1, G2, G3, G4, G5, G6 from DSP are converted to 0-5V signals PWMUT, PWMUB, PWMVT, PWMVB, PWMWT, PWMWB for gate drivers. The 0-5V fault signals FLTUn, FLTVn, FLTWn, and FLTn are level shifted to 0-3.3V for DSP.

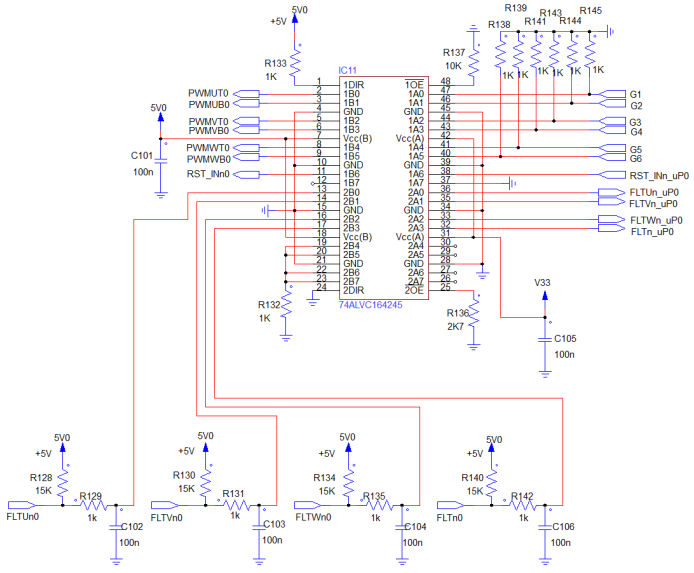


Figure 13: Gate drive interface circuit

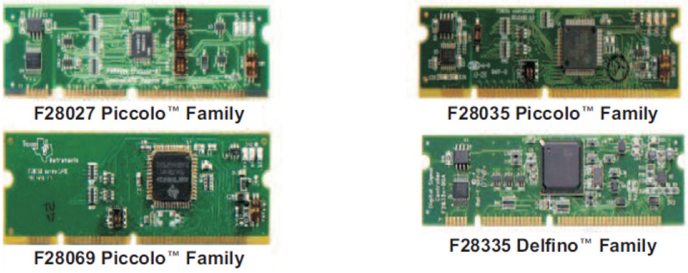


Figure 15: TI C2000 DSP Family controlCARDs

A brief description of each DSP is given below.

F28335:

The F28335 DSP has following main features:

- High-Performance floating point 32-Bit CPU (TMS320C28x) with 150 MHz (6.67-ns Cycle Time)
- On-Chip Memory (256K x 16 Flash, 34K x 16 SARAM, 8K x 16 Boot ROM)
- Six-Channel DMA Controller (for ADC, McBSP, ePWM, XINTF, and SARAM)
- Enhanced Control Peripherals
  - Up to 18 PWM Outputs
  - Up to 6 HRPWM Outputs With 150 ps MEP Resolution
  - Up to 6 Event Capture Inputs
  - Up to 2 Quadrature Encoder Interfaces
  - Up to 8 32-Bit Timers (6 for eCAPs and 2 for eQEPs)
  - Up to 9 16-Bit Timers (6 for ePWMs and 3 XINTCTRs)
- Three 32-Bit CPU Timers
- Serial Port Peripherals
  - Up to 2 CAN Modules
  - Up to 3 SCI (UART) Modules
  - Up to 2 McBSP Modules (Configurable as SPI)
  - One SPI Module
  - One Inter-Integrated-Circuit (I2C) Module
- 12-Bit ADC, 16 Channels
  - 80-ns Conversion Rate
  - x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Internal or External Reference
- Up to 88 Individually Programmable, Multiplexed GPIO Pins With Input Filtering

DSP Development Board

F28035:

The F28035 DSP has following main features:

- High-Efficiency fixed point 32-Bit CPU (TMS320C28x) with 60 MHz (16.67-ns Cycle Time)
- On-Chip Memory (64K x 16 Flash, 10K x 16 SARAM, 8K x 16 Boot ROM)
- Three 32-Bit CPU Timers
- Independent 16-Bit Timer in Each Enhanced Pulse Width Modulator (ePWM)
- Serial Port Peripherals
  - One SCI (UART) Module
  - Two SPI Modules
  - One Inter-Integrated-Circuit (I^2C) Bus
  - One Local Interconnect Network (LIN) Bus
  - One Enhanced Controller Area Network (eCAN) Bus
- Enhanced Control Peripherals
  - ePWM
  - High-Resolution PWM (HRPWM)
  - Enhanced Capture (eCAP) Module
  - High-Resolution Input Capture (HRCAP) Module
  - Enhanced Quadrature Encoder Pulse (eQEP) Module
  - On-Chip Temperature Sensor
  - Comparator
- 12-Bit ADC, 16 Channels
  - 216-ns Conversion Rate
  - x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
- Up to 45 Individually Programmable, Multiplexed GPIO Pins With Input Filtering

F28027:

The F28027 DSP has following main features:

- High-Efficiency fixed point 32-Bit CPU (TMS320C28x) with 60 MHz (16.67-ns Cycle Time)
- On-Chip Memory (Flash, SARAM, OTP, Boot ROM Available)
- Three 32-Bit CPU Timers
- Independent 16-Bit Timer in Each Enhanced Pulse Width Modulator (ePWM)
- Serial Port Peripherals
  - One Serial Communications Interface (SCI) Universal Asynchronous Receiver/Transmitter (UART) Module
  - One Serial Peripheral Interface (SPI) Module
  - One Inter-Integrated-Circuit (I2C) Module
- Enhanced Control Peripherals
  - ePWM
  - High-Resolution PWM (HRPWM)
  - Enhanced Capture (eCAP) Module

Chapter 6 – Communication Port and Computer Interface

The DSP board provides a number of communication ports for computer interface and program debugging purposes. These communication interfaces include one CAN BUS, one SCI BUS, one SPI BUS, one USB, and one JTAG.

6.1 CAN BUS Interface J3

Figure 16 shows the pin assignment of the CAN bus connector J3. Pin 1 is CAN high line and pin 2 is CAN low line. Pin 3 is digital ground.

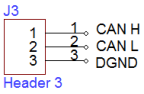


Figure 16: CAN bus connector J3 pin assignment

6.2 SCI Interface J6

Figure 17 shows the pin assignment of the SCI connector J6. Pin 1 is the RS-232 transmit output, pin 4 is the RS-232 receive input. Pin 2 is 3.3V power supply, pin 43 is ground.

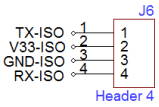


Figure 17 RS-232 Connector J6 Pin Assignment

Note that to use the SCI connector J6 for serial communication, the DIP switch S7_4 needs to be in the OFF position.

6.3 USB Interface J1

The USB connector J1 shown in Figure 18 provides the interface to a computer. The built-in DSP emulator allows users to debug DSP program with TI Code Composer Studio.

Table 5 shows the pin assignment of the connector J5. Pin 2 is data plus and pin 3 is data minus.

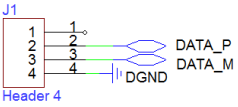
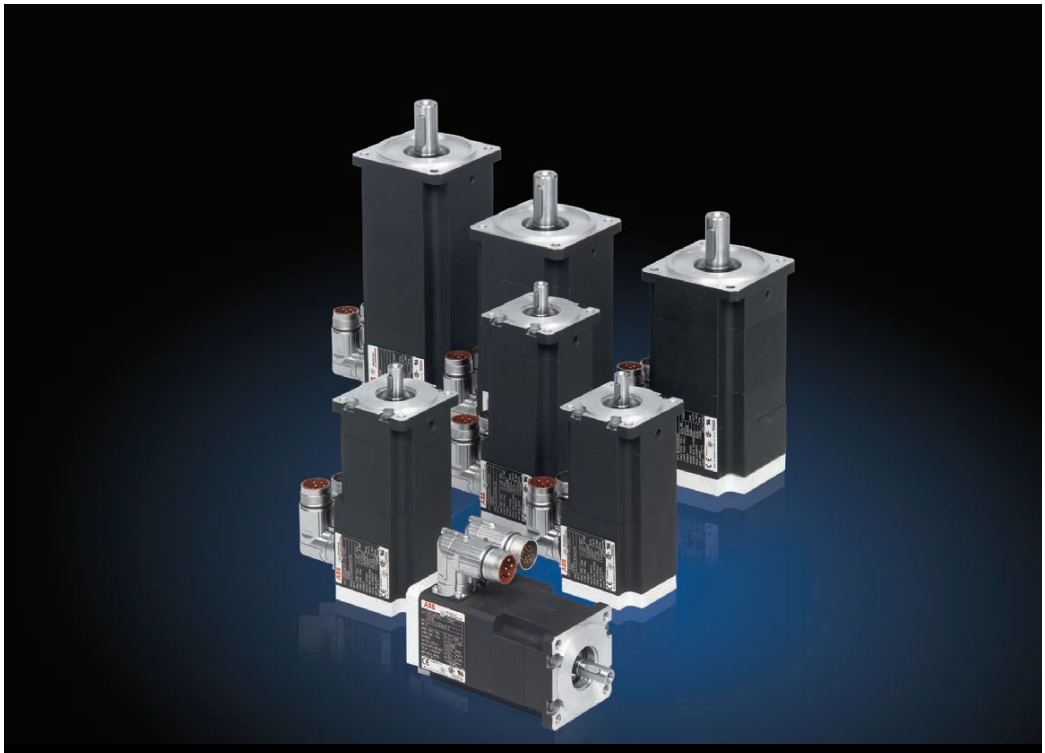


Figure 18: USB Connector J1 pin assignment

Pin Number	Pin Name	Description
1	NC	
2	DATA_P	Data plus
3	DATA_M	Data minus
4	DGND	Digital Ground

Table 5: USB Connector J1 pin assignment

A.12 ABB PMSM



Brochure

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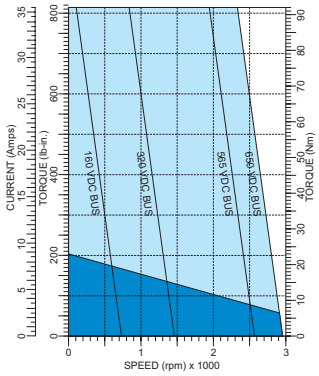
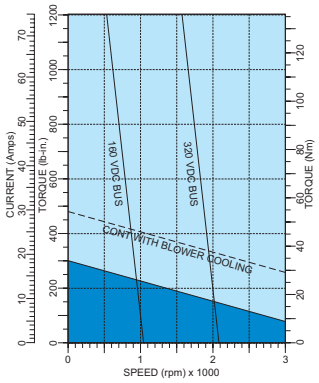
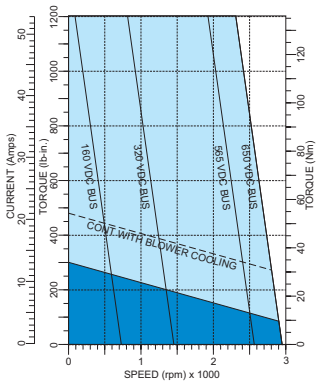


BSM100N-3150



BSM100N-3250



Model number		BSM100N-2250	BSM100N-3150[1]	BSM100N-3250[1]
General				
Continuous stall torque	lb-in	203.5	300	300
	Nm	23	34	34
Continuous current	amps	9.9	21	14.7
Peak torque	lb-in	814.2	1203.6	1203.6
	Nm	92	136	136
Peak current	amps	35.8	75.8	53.1
Thermal resistance	°C/watt	1	0.7	0.7
Thermal time constant	Min	67	76	76
Mechanical time constant	msec	0.3	0.24	0.29
Electrical time constant	msec	9.4	10.9	9.7
Rated speed @ 300 volts	rpm	1200	2000	1200
Rated speed @ 600 volts	rpm	2400		2400
Electrical				
Torque constant	lb-in/amp	22.6	15.8	22.6
	Nm/amp	2.56	1.79	2.56
Voltage constant	Vpk/krpm	219	153.1	218.8
	Vrms/krpm	154.9	108.3	154.7
Resistance	ohms	0.87	0.25	0.61
Inductance	mH	8.25	2.7	5.8
Mechanical				
Inertia	lb-in-s^2	0.0196	0.0273	0.0273
	Kg-cm^2	22.145	30.844	30.844
Maximum speed	rpm	4,000	4,000	4,000
Number of motor poles	—	8	8	8
Weight	lbs/Kg	49/22.3	63/28.6	63/28.6

[1] A blower option is available which will increase the motor's continuous stall torque by another 60%.

A.13 F28035 Piccolo Microcontroller

TMS320F28030, TMS320F28031, TMS320F28032
TMS320F28033, TMS320F28034, TMS320F28035

TEXAS INSTRUMENTS

SPRS584L – APRIL 2009 – REVISED DECEMBER 2017

TMS320F2803x Piccolo™ Microcontrollers

1 Device Overview

1.1 Features

- High-Efficiency 32-Bit CPU (TMS320C28x)
  - 60 MHz (16.67-ns Cycle Time)
  - 16 × 16 and 32 × 32 MAC Operations
  - 16 × 16 Dual MAC
  - Harvard Bus Architecture
  - Atomic Operations
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - Code-Efficient (in C/C++ and Assembly)
- Programmable Control Law Accelerator (CLA)
  - 32-Bit Floating-Point Math Accelerator
  - Executes Code Independently of the Main CPU
- Endianness: Little Endian
- JTAG Boundary Scan Support
  - IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- Low Cost for Both Device and System:
  - Single 3.3-V Supply
  - No Power Sequencing Requirement
  - Integrated Power-on Reset and Brown-out Reset
  - Low Power
  - No Analog Support Pins
- Clocking:
  - Two Internal Zero-Pin Oscillators
  - On-Chip Crystal Oscillator and External Clock Input
  - Watchdog Timer Module
  - Missing Clock Detection Circuitry
- Up to 45 Individually Programmable, Multiplexed GPIO Pins With Input Filtering
- Peripheral Interrupt Expansion (PIE) Block That Supports All Peripheral Interrupts
- Three 32-Bit CPU Timers
- Independent 16-Bit Timer in Each Enhanced Pulse Width Modulator (ePWM)
- On-Chip Memory
  - Flash, SARAM, OTP, Boot ROM Available
- Code-Security Module
- 128-Bit Security Key and Lock
  - Protects Secure Memory Blocks
  - Prevents Firmware Reverse Engineering
- Serial Port Peripherals
  - One Serial Communications Interface (SCI) Universal Asynchronous Receiver/Transmitter (UART) Module
  - Two Serial Peripheral Interface (SPI) Modules
  - One Inter-Integrated-Circuit (I2C) Module
  - One Local Interconnect Network (LIN) Module
  - One Enhanced Controller Area Network (eCAN) Module
- Enhanced Control Peripherals
  - ePWM
  - High-Resolution PWM (HRPWM)
  - Enhanced Capture (eCAP) Module
  - High-Resolution Input Capture (HRCAP) Module
  - Enhanced Quadrature Encoder Pulse (eQEP) Module
  - Analog-to-Digital Converter (ADC)
  - On-Chip Temperature Sensor
  - Comparator
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug Through Hardware
- Package Options
  - 56-Pin RSH Very Thin Quad Flatpack (No Lead) (VQFN)
  - 64-Pin PAG Thin Quad Flatpack (TQFP)
  - 80-Pin PN Low-Profile Quad Flatpack (LQFP)
- Temperature Options
  - T: –40°C to 105°C
  - S: –40°C to 125°C
  - Q: –40°C to 125°C
    (AEC Q100 Qualification for Automotive Applications)

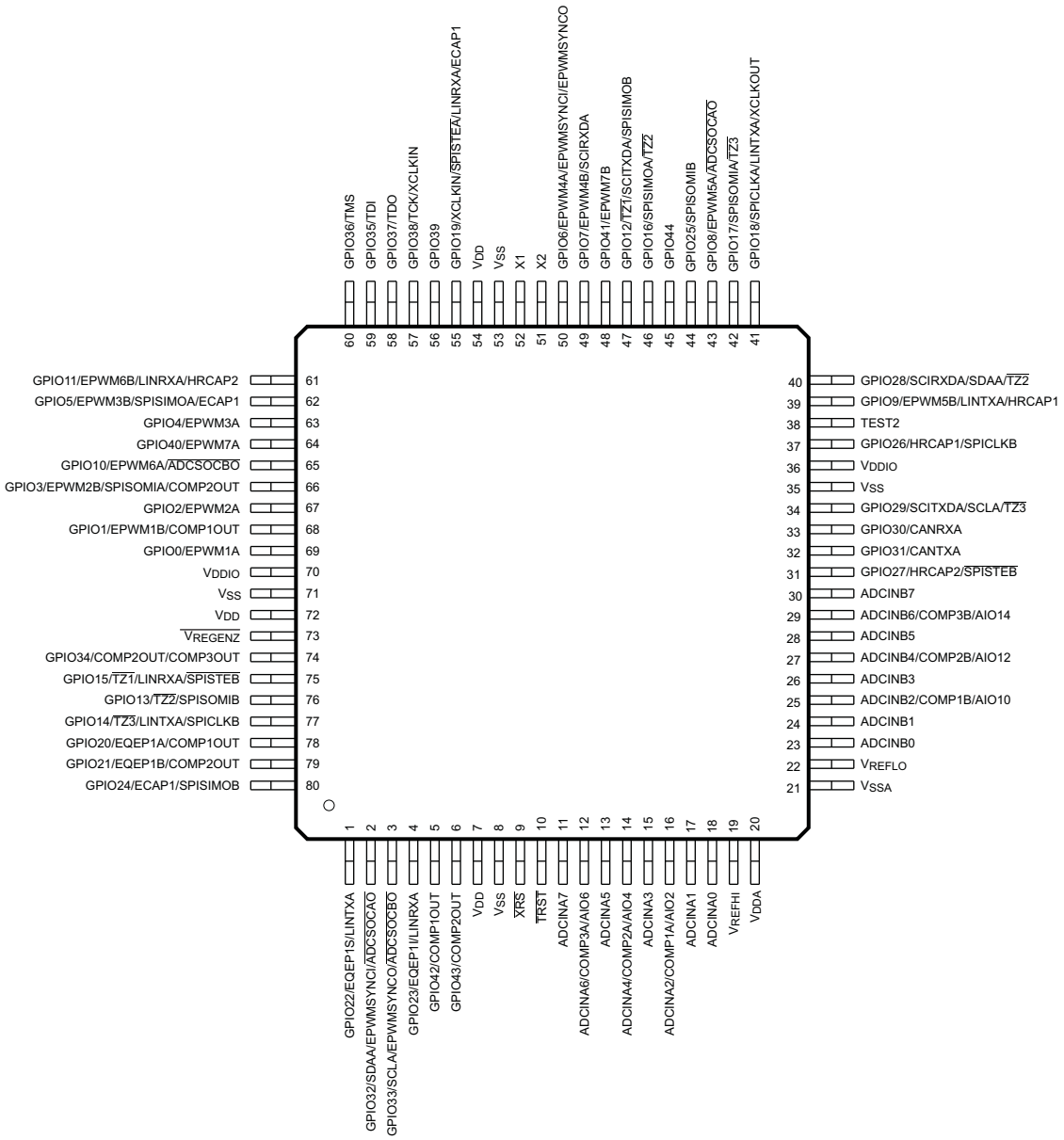


Figure 4-3. 2803x 80-Pin PN LQFP (Top View)

Appendix B Hardware Configuration

B.1 Hardware Config, SCI Config and DSP Clock

Port	Pin Name	Description
ADCB0	Iain	Current Sensor Phase A
ADCB1	Ibin	Current Sensor Phase B
GPIO0	PWM_UT	PWM Gate High Phase A
GPIO1	PWM_UB	PWM Gate Low Phase A
GPIO2	PWM_VT	PWM Gate High Phase B
GPIO3	PWM_VB	PWM Gate Low Phase B
GPIO4	PWM_WT	PWM Gate High Phase C
GPIO5	PWM_WB	PWM Gate Low Phase C
GPIO20	POSV	Hall Sensor Phase V
GPIO21	POSW	Hall Sensor Phase W
GPIO22	POSA	Encoder Phase A
GPIO23	POSB	Encoder Phase B
GPIO28	RXDA	Non-Isolated RS 232 Receive Input (SCI Input Port)
GPIO29	TXDA	Non-Isolated RS-232 Transmit Output (SCI Output Port)

Table 10: Hardware Configuration

Parameter	Configuration
SCI Port	SCIA (GPIO28,29)
Speed (bps)	115200
Parity Check	None
Output Buffer Size	64

Table 11: SCI Configuration

Parameter	Configuration
DSP Clock Source	Internal Oscillator 1
External Clock (MHz)	10
DSP Speed (MHz)	60

Table 12: DSP Clock

Appendix C Further Results

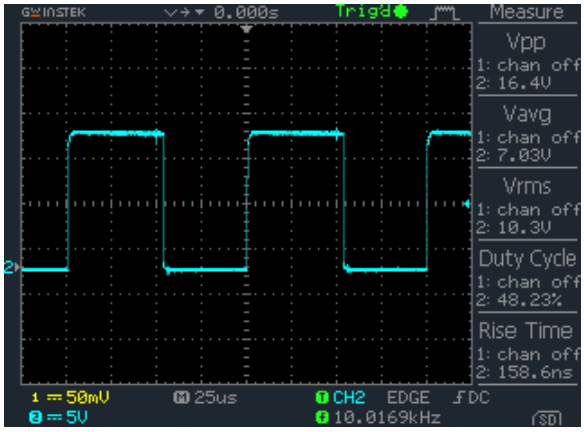


Figure 85: LO Referenced to COM (Phase A)

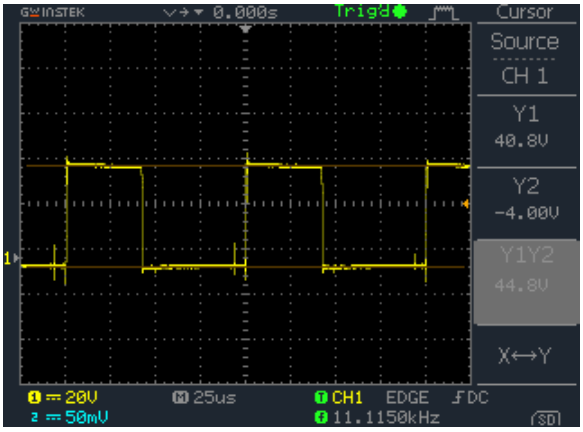


Figure 86: Hardware IGBT Low Signal

Appendix D Calculations and Excel Sheets

D.1 ABB PMSM Calculations

	A	B	C	D	E	F
1	**V_DC [V]**		**320**	**545**	**565**	**650**
2	**Min. load [Nm]**		0	0	0	0
3	**Max. load [Nm]**		92	92	92	92
4	**Speed at min. load [rpm]**	**0 Nm**	1 461	2 489	2 580	2 968
5	**Speed at max. load [rpm]**	**92 Nm**	839	1 866	1 958	2 346
6	**Δ speed(n_max-N_min) [rpm]**		622,19	622,19	622,19	622,19
7	**m [Nm/rpm]**		0,14787	0,14787	0,14787	0,14787
8						
9	**Ke [Vpk/krpm]**	**219**				
10	**Kt [Nm/A]**	**2,56**				
11						
12	**Rated power [kW]**		-	2,332	-	-
13	**Rated torque [Nm]**		-	9,18	-	-
14	**Rated current [A]**		-	3,59	-	-
15	**Rated speed [rpm]**		-	2 426	-	-
16	**Rated speed [rad/s]**		-	254,05	-	-
17	**Max speed [rpm]**		-	2 489	-	-
18	**Max speed [rad/s]**		-	260,65	-	-
19						

D.2 Calculations of Gate Driver Circuit Components

	A	B	C	D	E	F	G	H	I	J	K	L
1	**ITRIP**											
2	R_SH	0,048	*[Ω]*									
3	R_SH (Round off)	0,05	*[Ω]*									
4	I_TRIP_TH	45	*[mA]*									
5	V_IT,TH+ (MIN)	0,38	*[V]*		V_IT,TH+ (TYP)	0,445	*[V]*		V_IT,TH+ (MAX)	0,51	*[V]*	
6	I_ITRIP (MIN)	7,987	*[A]*		I_ITRIP (TYP)	8,9	*[A]*		I_ITRIP (MAX)	10,2	*[A]*	
7												
8	**C_BS**											
9	i_QBS	0,00021	210	[µA]								
10	f_s	10 000	10	kHz								
11	t_P	0,0001	0,0001	[s]								
12	Q_G	0,0000001	0,1	[µC]								
13	Δv_BS	0,1		[V]								
14												
15	C_BS	0,000001452	1,452	[µF]								
16												
17	**Gate resistor**											
18	L_S	25	*[nH]*									
19	C_ISS	0,55	*[nF]*									
20												
21	R_G (MIN)	13,48	*[Ω]*									
22	R_G (Selected)	**15**	*[Ω]*									
23												
24												

D.3 Transient Calculation

Resistance		Frequency		Overshoot		%Overshoot	Steady State Time	Parameters:		
25	Ω	1	kHz	9,6	V	44,24%	1,3 µs	Test voltage:	12,1	V
25	Ω	10	kHz	9,6	V	44,24%	1,3 µs			
25	Ω	20	kHz	8,6	V	41,55%	1,3 µs			
25	Ω	30	kHz	7,6	V	38,58%	1,3 µs			
25	Ω	50	kHz	6	V	33,15%	1,3 µs			
25	Ω	75	kHz	5	V	29,24%	1,3 µs			
25	Ω	100	kHz	4,6	V	27,54%	1,3 µs			
50	Ω	1	kHz	3,28	V	21,33%	1,12 µs			
50	Ω	10	kHz	3,04	V	20,08%	1,12 µs			
50	Ω	20	kHz	2,72	V	18,35%	1,12 µs			
50	Ω	30	kHz	2,56	V	17,46%	1,12 µs			
50	Ω	50	kHz	2,54	V	17,35%	1,12 µs			
50	Ω	75	kHz	2,48	V	17,01%	1,12 µs			
50	Ω	100	kHz	1,92	V	13,69%	1,12 µs			
100	Ω	1	kHz	1,68	V	12,19%	1,24 µs			
100	Ω	10	kHz	1,6	V	11,68%	...			
100	Ω	20	kHz	1,36	V	10,10%	...			
100	Ω	30	kHz	1,2	V	9,02%	...			
100	Ω	50	kHz	1,12	V	8,47%	...			
100	Ω	75	kHz	0,92	V	7,07%	...			
100	Ω	100	kHz	0,88	V	6,78%	1,16 µs			
150	Ω	1	kHz	1,12	V	8,47%	1,2 µs			
150	Ω	10	kHz	1	V	7,63%	.....			
150	Ω	20	kHz	0,88	V	6,78%	...			
150	Ω	30	kHz	0,76	V	5,91%	...			
150	Ω	50	kHz	0,68	V	5,32%	...			
150	Ω	75	kHz	0,6	V	4,72%	...			
150	Ω	100	kHz	0,56	V	4,42%	1,34 µs			
200	Ω	1	kHz	0,76	V	5,91%	1,32 µs			
200	Ω	10	kHz	0,68	V	5,32%	...			
200	Ω	20	kHz	0,6	V	4,72%	...			
200	Ω	30	kHz	0,56	V	4,42%	...			
200	Ω	50	kHz	0,46	V	3,66%	...			
200	Ω	75	kHz	0,42	V	3,35%	...			
200	Ω	100	kHz	0,42	V	3,35%	1,6 µs			
250	Ω	1	kHz	0,56	V	4,42%	1,48 µs			
250	Ω	10	kHz	0,52	V	4,12%	.....			
250	Ω	20	kHz	0,46	V	3,66%	.....			
250	Ω	30	kHz	0,4	V	3,20%	.....			
250	Ω	50	kHz	0,36	V	2,89%	.....			
250	Ω	75	kHz	0,34	V	2,73%	.....			
250	Ω	100	kHz	0,34	V	2,73%	1,74 µs			